McMOS
INTEGRATED CIRCUITS DATA BOOK

This book presents technical data for the broad line of McMOS integrated circuits. Complete specifications for the individual monolithic circuits are provided in the form of data sheets. Design information and family characteristic data provide the details necessary for successful use of McMOS circuits in system design. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

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DATA SHEETS

McMOS
INTEGRATED CIRCUITS

Chapter 1
TECHNOLOGY OVERVIEW

INTRODUCTION

This McMOS Data Book has been prepared as a working tool for the system, logic, and layout designer. The organization and format of the book allows the designer to select the information based upon frequency of use. General introductory information and design data are grouped in the first sections of the book and provide a wealth of in-depth design and reference information. For day to day usage, the user may quickly bypass the Introductory, Design and Applications sections and proceed directly to the Index section, where an individual device in the family may be rapidly selected using either functional characteristics or alpha-numeric order.

Chapter 1 provides a technology overview of Complementary Metal Oxide Semiconductors, commonly referred to as CMOS. It serves as an introduction to CMOS for the new user or as a brief refresher for the seasoned designer. This section also introduces Motorola's McMOS family as well as providing a list of symbols and abbreviations related to this semiconductor technology.

Chapter 2 presents McMOS design information. Included in this section are the details necessary to successfully implement a system of logic which utilizes only CMOS or a mixture of CMOS with various bipolar logic types. Critical parameters such as power supply requirements, fan-out, noise immunity and interfacing with other logic forms are given special attention.

Chapter 3 is the application oriented portion of the Data Book. Specific applications of McMOS are presented as well as an applications index for device types. To enable the designer to gain a broader perspective of CMOS technology, a published article reference section is also provided.

Chapter 4 provides two functional indexes; one index presents the data in tabular form, and a second presents the devices in block diagram form. In addition, this chapter provides previews of devices soon to be announced.

For most efficient use of the detailed information presented in the data sheets, Chapter 5 provides McMOS family characteristics. This section provides ready references for key device parameters to be considered during the design, layout and fabrication of systems using the McMOS family of devices.

Package data is presented in Chapter 6 and includes appropriate mechanical and pictoral information. To assist the layout design effort, a portion of this section has been devoted to package outline diagrams which also include functional outputs.

Concluding the Data Book is Chapter 7 – a compilation of the McMOS data sheets. For ease of use, the sheets have been arranged in alpha-numeric order.

McMOS FUNDAMENTALS

Until recently, a system designer seeking a suitable system logic family had only two choices of technology; random system logic functions were bounded by either the saturated or non-saturated bipolar technologies. A choice of saturated logic offered high speed but non-saturated logic provided a range from high to low speed.

With the advent of CMOS, a new and economical choice was presented to the system designer. Not only does the McMOS family offer very low-power dissipation at medium speeds but additional benefits are obtained, such as freedom from precision power supplies, high noise immunity and large fan-outs. These advantages are offered in a wide variety of basic and complex logic functions allowing the designer complete system design freedom.

To better understand this new family and its use, the following paragraphs explore the basic MOS elements and their combination to form CMOS.

MOS DEVICES

The starting point for any investigation into MOS devices is the enhancement mode Field Effect Transistor. The first FET devices were fabricated using N-type substrate with two diffused regions of P-type material, the source and drain. A metalized layer separated from the substrate by a diffused layer of silicon dioxide formed the gate or control element. Figure 1-1 is a cross-section of the P-channel element and the schematic symbol.

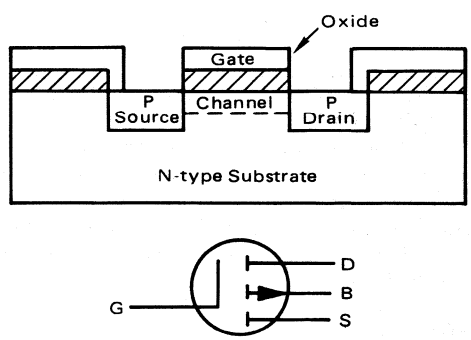


FIGURE 1-1 – P-CHANNEL TRANSISTOR (PMOS)

A voltage applied to the gate establishes a path for hole conduction (P-channel) between the source and drain. Similarly, using a P-substrate with N-doping for the source and drain results in an element utilizing electron conduction after gate turn-on (N-channel). Figure 1-2 is a cross-section of an N-channel element and the schematic symbol.

Either of these FET devices can be implemented into logic elements. Figure 1-3 is an inverter constructed using two N-channel devices.

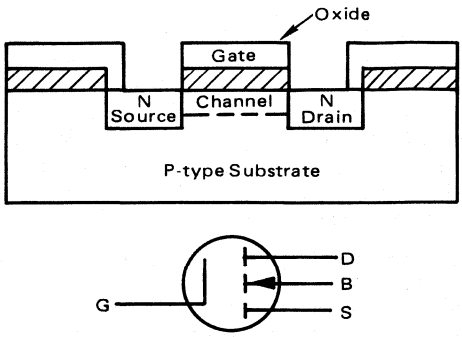


FIGURE 1-2 – N-CHANNEL TRANSISTOR (NMOS)

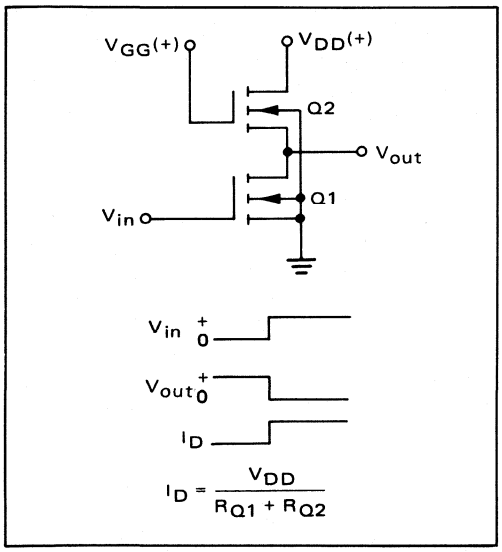


FIGURE 1-3 – TYPICAL N-CHANNEL INVERTER

In the circuit, Q2 serves as a fixed load resistor while transistor Q1 is switched. When Q1 is turned-on by the input signal, current is drawn from V_{DD} dissipating power in Q2. Circuits similar to these are currently in use in devices known as NMOS and PMOS.

CMOS DEVICES

A third configuration can also be implemented which makes use of both the N-channel and the P-channel devices. As shown in Figure 1-4, a complementary inverter may be formed by applying the input signal to the gates of two opposite polarity transistors.

In this circuit a low input signal means the N-channel transistor Q1 is OFF and the P-channel device is ON. The output is shorted to the positive supply, but virtually no load current is drawn if a similar high impedance MOS gate input is assumed as the load. When the input signal goes high, Q1 is turned-on and Q2 is turned-off. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the complementary MOS circuit (CMOS) is thus limited to the crossover conditions existing as the transition occurs from state to state. Proper device design for rapid turn-on and turn-off results in a dissipation factor as low as 2 nW per gate. The high noise immunity is also a direct result of the complementary configuration, since two separate thresholds must be crossed. This threshold is a direct function of power supply voltage, and is typically 45% of the supply voltage.

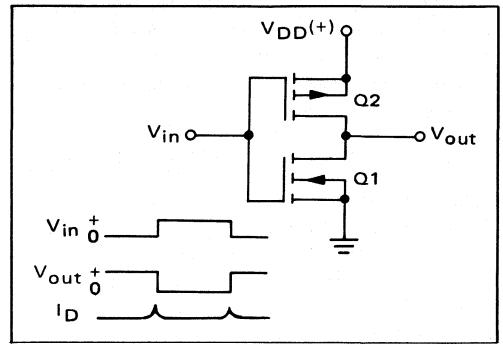


FIGURE 1-4 – TYPICAL COMPLEMENTARY INVERTER

The CMOS circuit results in a more complex fabrication process. Figure 1-5 shows a cross section of the CMOS integrated circuit. The P-channel device remains directly within the N-substrate. To form the N-channel device, however, a P-doped "tub" must be created into which the device is placed. In addition, channel stops must be placed between the "tub" and the P-drain to prevent parasitic channeling effects.

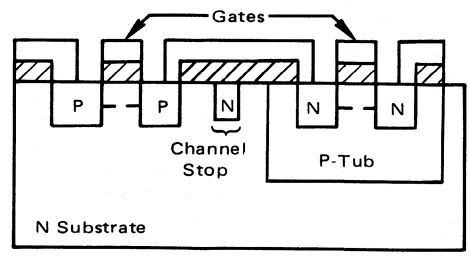


FIGURE 1-5 – TYPICAL CROSS SECTION OF COMPLEMENTARY MOS ELEMENTS (CMOS)

McMOS DEVICES

Using the basic CMOS technique, Motorola has developed the McMOS family of logic elements. A basic building block of logic elements has been designed and designated the MC14000 series. Examples of devices in this series are quad 2-input NOR gates and dual J-K flip-flops. Family expansion into more complex and specialized circuits has resulted in the MC14500 series. Included here are such devices as the dual 4-bit latch and a dual retriggerable/resettable monostable multivibrator. Memories constructed for the McMOS family are listed in the MCM14000 series.

SYMBOL GLOSSARY

BW	Bandwidth
C_{in}	Input Capacitance
C_L	Load Capacitance
f	Frequency (highest system rate)
I	Maximum Current Per Pin
I_{DD}	V_{DD} Supply Current
I_{in}	Input Current
I_{OH}	Output Source Current (high level state)
I_{OL}	Output Sink Current (low level state)
I_{out}	Output Current
I_{SS}	V_{SS} Supply Current
I_{TC}	Through-Current of McMOS Devices per Package
I_{TL}	Three-State Output Leakage Current
P_D	Power Dissipation
$P_{DD}max$	Maximum Power Dissipation per Package
P_L	Power Dissipation Due to Charge and Discharge of Internal and External Capacitance per Package.
$P_{OH}max$	Maximum Power Dissipation per Output Pin (high level output state)
$P_{OL}max$	Maximum Power Dissipation per Output Pin (low level output state)
P_Q	Quiescent Power Dissipation per Package
PRF	Pulse Rate Frequency (clock)
P_T	*Total (dynamic plus quiescent) power Dissipation per Package
P_{TC}	Power Dissipation Due to Switching Through-Current per Package
PW	Pulse Width
R_{ON}	On Resistance
T_A	Ambient Operating Temperature
T_{stg}	Storage Temperature
t_{acc}	Access Time
t_{cyc}	Cycle Time
t_f	Falling Transition Time (high to low)
t_{hold}	Hold Time
T_J	Junction Temperature
t_{PLH}	Propagation Delay Time (low to high output state)
t_{PHL}	Propagation Delay Time (high to low output state)
t_r	Rising Transition Time (low to high)
t_{rem}	Removal Time
t_{rel}	Release Time
t_{setup}	Setup Time
$t_{"0"H}$	Three-State Propagation Delay Time (low to high impedance output state)
$t_{H"0"}$	Three-State Propagation Delay Time (high impedance to low output state)
$t_{"1"H}$	Three-State Propagation Delay Time (high to high impedance output state)
$t_{H"1"}$	Three-State Propagation Delay Time (high impedance to high output state)
V_{DD}	Most Positive dc Supply Voltage
V_{in}	Input Voltage
V_{NH}	Noise Immunity Voltage Range (high level)
V_{NL}	Noise Immunity Voltage Range (low level)
V_{OH}	Output Voltage Level (high level output state)
V_{OL}	Output Voltage Level (low level output state)
V_{out}	Output Voltage Level (general)
V_S	Source Voltage
V_{SS}	Most Negative dc Supply Voltage
"0" or L	**Zero, Low, or False Logic State (most negative level)
"1" or H	**One, High, or True Logic State (most positive level)

*Some IC's may be on a per gate basis.
**Positive logic assumed.

ACRONYM GLOSSARY

ALU	Arithmetic Logic Unit
ASCII	American Standard Code for Information Interchange
BCD	Binary Coded Decimal
BCDIC	Binary Coded Decimal Information Code
CMOS	Complementary MOS
DIP	Dual In-Line Package
DTL	Diode-Transistor Logic
EBCDIC	Extended Binary Coded Decimal Interchange Code
ECL	Emitter-Coupled Logic
FET	Field-Effect Transistor
HTL	High-Threshold Logic
IC	Integrated Circuit
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LTTL	Low Power TTL
LSI	Large-Scale Integration
MOS	Metal-Oxide-Semiconductor
MPU	Micro-Processing Unit
MSI	Medium-Scale Integration
PROM	Programmable ROM
RAM	Random Access Memory
ROM	Read Only Memory
RTL	Resistor-Transistor Logic
SCR	Silicon Controlled Rectifier
SSI	Small-Scale Integration
STRL	Schottky Transistor-Resistor Logic
TTL	Transistor-Transistor Logic

MCMOS
INTEGRATED CIRCUITS

Chapter 2
DESIGN INFORMATION

INTRODUCTION

This chapter presents the systems designer with a complete portfolio of Motorola McMOS design information. The information contained will enable the designer to gain a theoretical and practical background of CMOS systems design and implementation. Areas such as powering, operation, physical information, input/output considerations, loading, etc. are presented in significant detail. Interfacing techniques and three-state operating capability expand and highlight the blend of useful design information for the CMOS logic technology.

McMOS POWER SUPPLY CONSIDERATIONS

Three major advantages of the McMOS technology are:

- very low power dissipation,
- wide power supply voltage operating range, and the
- switching threshold remains as a constant ratio (typically 45% of the power supply voltage) throughout the full voltage range of the device.

These three major advantages enable a designer to operate a system designed with McMOS logic from unregulated and/or poorly-filtered power supplies, while at the same time eliminating the special cooling equipment often found to be a necessity in large bipolar systems. In addition, new areas of design in battery-operated and battery-back-up systems have been introduced using the McMOS logic family.

Obviously, an understanding of the limitations and tradeoffs as well as the flexibility of a CMOS system power supply design can provide the designer with a realized savings in total systems costs and also a means of implementing new designs previously not possible using other technologies.

OPERATING RANGE

Motorola McMOS devices are specified in two power supply ranges. The "AL" series (military temperature range devices) is designed to operate with a net potential difference between the V_{DD} and V_{SS} terminals that may vary from 3 to 18 volts. The "CL" and "CP" series (extended commercial temperature range devices) are designed to operate from 3 to 16 volts.

The published maximum allowable operating supply voltage ($V_{DD} - V_{SS}$) appears to be conservative when compared with the maximum 25 to 35 V low-current junction avalanche measurements obtained in the laboratory. Such maximum supply voltages are not really conservative if the device is forced further into avalanche and the secondary breakdown effects are observed, as shown in Figure 2-1. Sustaining currents (I_S) generally vary only from 10 to 50 mA, but such a current jump can be catastrophic to the device. Once in this breakdown mode, in which the power supply differential ($V_{DD} - V_{SS}$) is above the source voltage (V_S), any on-chip current transient having a value greater than the required sustaining current can forward bias parasitic bipolar devices present in all CMOS devices. The resulting high currents will produce a short circuit reflected at the power supply.

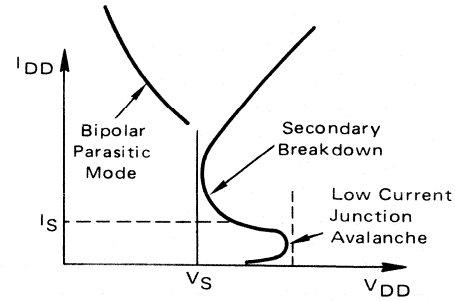


FIGURE 2-1 – SECONDARY BREAKDOWN CHARACTERISTICS

Minimum recommended supply voltage values also require significant consideration. The industry-standard minimum value of 3 V is based on the maximum allowable individual device threshold voltage levels for either P- or N-channel transistors, whichever value is larger. At this minimum value, the CMOS device performs satisfactorily in all "standard" digital logic applications. However, a small but important class of circuit applications exists which require supply voltages greater than the sum of both the P- and N-channel thresholds. Direct feedback circuits such as the linear amplifier and RC oscillator shown in Figure 2-2 represent such applications. In general, caution is necessary when using innovative feedback biasing schemes below a 4 V supply level.

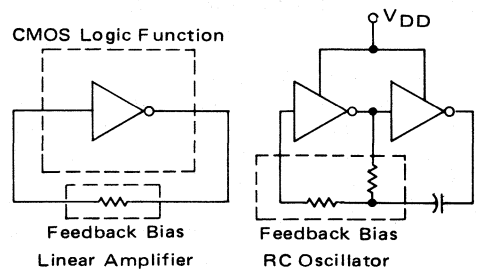


FIGURE 2-2 – LINEAR BIASING SCHEMES

POWER DISSIPATION

Power dissipation in a CMOS device is comprised, in varying degrees, of three basic components:

- quiescent power dissipation, P_Q, (a power dissipation due to surface leakage currents),
- P_{TC} (a power dissipation due to switching through-current), and

- P_L (a CV^2f power dissipation due to the charging and discharging of internal and external capacitances).

Total power dissipation P_T, is the sum of these basic components and is given by the equation:

$$P_T = P_Q + P_{TC} + P_L$$

QUIESCENT DISSIPATION

The first power dissipation component, P_Q (quiescent), is a product of the power supply voltage V_{DD}, and the leakage current I_L, (typically in the nanoampere range). This leakage is due to a combination of surface effects and a network of parasitic diode junctions which are normally reverse-biased and are shown in Figure 2-3(a). The leakage is simulated in the CMOS inverter cross-section shown in Figure 2-3(b).

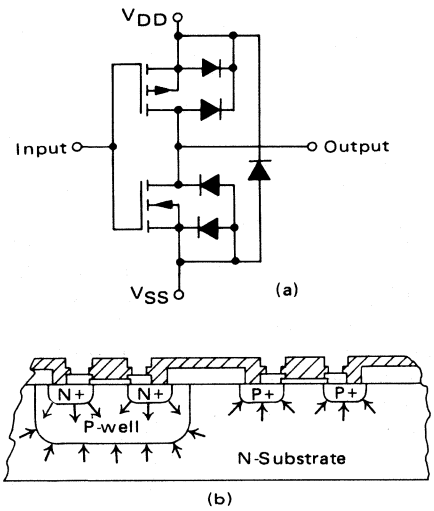


FIGURE 2-3 – LEAKAGE CURRENTS OF P-N DIODE JUNCTIONS

The quiescent power dissipation is extremely low (typically in the nanowatt range) and is usually a negligible portion of the total power dissipation of an operating system. However, many CMOS designs may require long periods of "Standby" operation, during which the logic devices are not actually switching. The worst case power supply drain (often a battery in such a "standby" system) may be calculated by summing the maximum quiescent power dissipation specifications (available in the individual McMOS device data sheet) of all devices within the system.

DYNAMIC DISSIPATION

The remaining two components of power dissipation, P_{TC} and P_L, occur during the dynamic operation of a CMOS device. The through-current dissipation P_{TC}, is a result of current that momentarily flows from the power supply to ground when a CMOS device switches between logic levels. This through-current I_{TC} is a complex function of the input and output rise and fall times, the input signal frequency, the power supply voltage, and the various parameters (mobility, geometric, channel dimension, etc.) of the MOS transistors.

The through-current I_{TC} has a peak value which can be approximated by the equation:

$$I_{TC} \propto K_0 (V_{DD} - K_1)^2$$

where: K_0 is a constant dependent on the N- and P-channel mobility, geometry, and temperature. The constant K_1 is dependent upon the individual MOS device thresholds. A typical normalized plot of this relationship is shown in Figure 2-4.

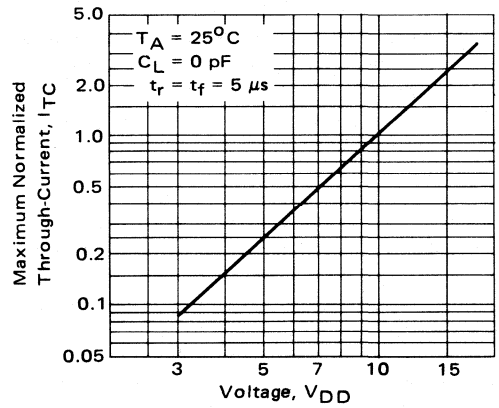


FIGURE 2-4 – NORMALIZED PLOT OF THROUGH-CURRENT VERSUS VOLTAGE

The waveform of the through-current in relationship to the voltage transfer characteristics of a typical inverter pair is shown in the oscillograph, Figure 2-5. The energy contained in the through-current pulse will be a function of the input clock transition time (the time the device remains in the active ON region). The peak current (previously shown in Figure 2-4) can be measured with no-load capacitance. As load capacitance is applied and the input transition time is decreased, the through-current magnitude decreases from its peak value to practically zero as will be described later.

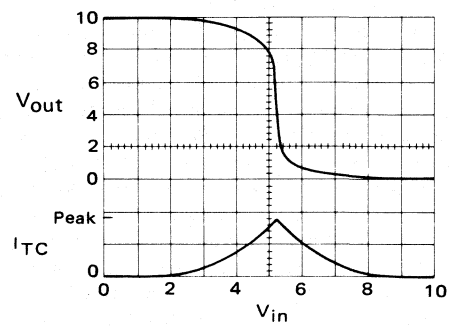


FIGURE 2-5 – THROUGH-CURRENT AND TRANSFER CHARACTERISTICS

The power dissipation, due to through-current P_{TC}, may be theoretically defined as frequency times the integral of the product of the supply voltage and the through-current. This relationship is illustrated by the equation:

$$P_{TC} = f \int_{0}^{t_r} V_{DD}\, I_{TC}\, dt.$$

However, I_{TC}, previously was shown to be:

$$I_{TC} \propto K0\,(V_{DD} - K1)^2.$$

Therefore:

$$P_{TC} \propto fKV^N,$$

where: f = frequency,
K = constant (dependent on device parameters),
N = non-integral number greater than 3.

The second component of the dynamic power dissipation, P_L, is proportional to the energy required to charge and discharge the load capacitance C_L and the small internal circuit capacitance. Power is basically defined as energy per unit time. Therefore, the energy storage E of a capacitor is given by the equation:

$$E = 1/2\, CV^2.$$

Since the capacitance is alternately charged and discharged through the CMOS device during one complete cycle of the input frequency f, the power P_L is given by the equation:

$$P_L = CV^2 f.$$

Thus, the dynamic dissipation increases linearly with the frequency and load capacitance and also as the square of the power supply voltage V_{DD}. Figure 2-6 shows this relationship for a typical McMOS gate.

The power dissipation shown in Figure 2-6 applies for input rise/fall times of 20 nanoseconds. For fast rise and fall times the previously described through-current dissipation P_{TC} is negligible. As the transition times increase, the power (P_{TC}) increases appreciably and is a complex function of the transition times and capacitance.

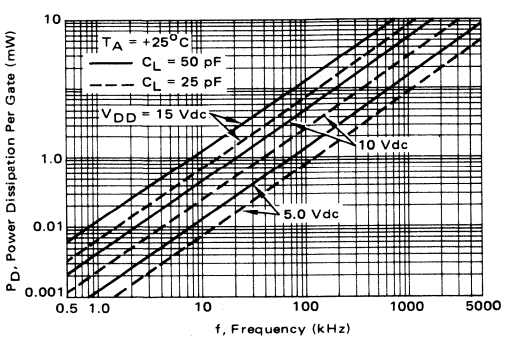
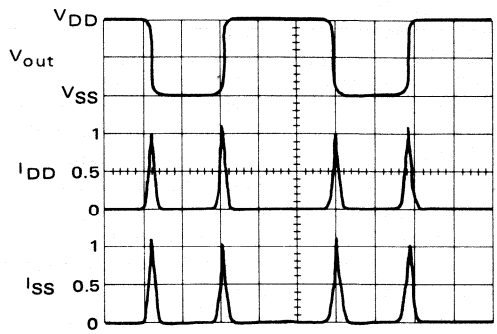
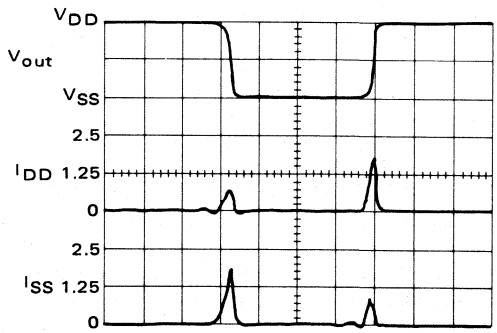


FIGURE 2-6 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

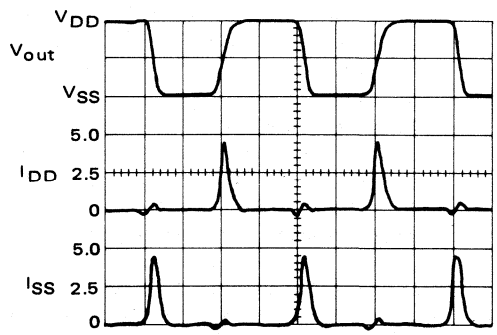
Figure 2-7 (a through c) shows the relationship of the power supply current I_{DD} into the device and the ground current I_{SS} out of the device as a function of the capacitance and transition times. The waveforms in (a) show the currents I_{DD}, I_{SS} and I_{TC} for a rise (t_r) and fall (t_f) time of 10 μs at a 15 pF load. The lesser magnitude of the current pulses (first pulse of I_{DD}) represents the maximum through-current I_{TC} of the device at a given voltage V_{DD}. The increase in amplitude in the current pulse (I_{DD} when V_{out} goes positive or I_{SS} when V_{out} goes negative) is representative of the current required to charge (or discharge) the 15 pF load capacitance. The magnitude of the through-current in (a) is used as the normalizing factor in the current waveforms of (b) and (c).



(a) Input t_r, $t_f \simeq 10$ μs
C_L = 15 pF



(b) Input t_r, $t_f \simeq 400$ ns
C_L = 15 pF



(c) Input t_r, $t_f \simeq 40$ ns
C_L = 65 pF

FIGURE 2-7 – SWITCHING CURRENT WAVEFORMS

Oscillograph (b) was made with the same 15 pF load as (a); however, the input transition times (t_r, t_f) are now 400 ns. Again, the smaller current pulses are through-current. The magnitude of the current I_{TC} in (b) has decreased slightly from that in (a). Also, due to the faster transition time, the current pulse width has also decreased. This indicates that some of the charge is being diverted to the load capacitance.

In (c) the capacitance is increased to 65 pF and t_r and t_f are equal to 40 ns. The sinusoidal characteristic of the through-current, present with very fast transition times, is due to the charging and discharging of the parasitic internal capacitances. The previously observed I_{TC} pulse is now almost entirely directed to the load and the dissipation P_{TC} and is negligible when compared with the CV^2f dissipation P_L. The magnitude of the load current has increased for two reasons. First, the load was increased and now requires approximately four times the previous charge. Second, the charge is an integral of this pulse and since the transition times were decreased (hence the current pulse width decreased), the magnitude must increase to supply the same charge.

Figure 2-7 serves to illustrate the relative changes in charging current as a function of load capacitance and also shows the effect of the input transition time on the through-current and the resultant increase in power dissipation. All of the MSI or complex functional McMOS devices have their inputs buffered and thus do not have a severe through-current versus input transition characteristic. However, the system designer should be cautious when using high current drivers with high supply voltages so that the device power dissipation is not exceeded with a long input rise or fall time.

REGULATION AND BATTERY OPERATION

Because of the wide power supply operating range and the constant ratio of the switching threshold to the supply voltage, simple and inexpensive unregulated supplies of the type shown in Figure 2-8(a) may be used to power a system comprised of McMOS devices. The three primary design considerations of such a supply are:

- the voltage level must remain between the minimum and maximum specifications of the device,
- the lowest instantaneous supply level must allow the devices to operate at the necessary maximum system frequency (see the section entitled "Operating Speed Considerations" in this chapter), and
- the filter capacitor must be large enough to supply the peak instantaneous switching current requirements of the McMOS system.

The zener diode D_Z, in Figure 2-8(a) supplies protection by limiting the maximum voltage V_{DD}, supplied to the McMOS system. The resistor R_S, is chosen to supply the peak transient current of the load current, I_L, (plus the required zener current for maintaining its breakdown) when the input voltage V_S is at the peak value. This design philosophy assumes the transient portion of the load current I_L will charge capacitor C to the zener voltage during the non-switching time of the McMOS system. The current rating on the zener diode D_Z is dictated by the relationship of the equation:

$$I_{Z(max)} = \frac{V_{S(peak)} - V_Z}{R_S}.$$

This assumes the capacitor is fully charged to V_Z and the system is operating in a quiescent (non-switching) mode. The capacitor C is selected by the following equation:

$$C = \frac{q}{V},$$

where: $q = I_P\,[(\text{pulse width})\,(N)] + [(I_Q)\,(t)]$,

and $V = V_{zener} - V_{DD}\,\text{min}.$

The required charge q has two components. The major component is the transient peak load current, I_P, times its pulse width multiplied by the number N of transients during the non-conduction period of diode D1. The second component is the product of the quiescent current I_Q and the non-conduction time t. V_{DD} is the minimum supply voltage dictated by the specifications of the McMOS devices and the maximum desired operating speed.

A battery back-up supply is easily implemented by replacing the filter capacitor with rechargeable battery as shown in Figure 2-8(b). The battery voltage is selected for the desired operating voltage V_{DD}. The zener diode D_Z has a breakdown voltage greater than the battery voltage and is equal to or less than the maximum V_{DD} McMOS device ratings.

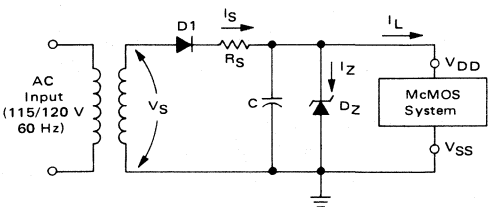


FIGURE 2-8(a) – McMOS UNREGULATED POWER SUPPLY

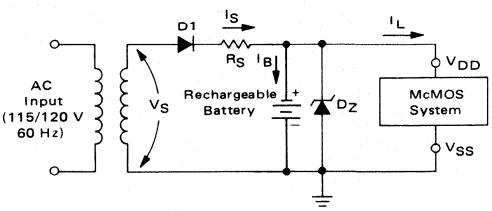


FIGURE 2-8(b) – McMOS BATTERY BACK-UP POWER SUPPLY

In this manner, only the zener conducts and also provides protection during power line transients (which develop voltage spikes due to the battery's characteristic impedance). The resistor R_S in this system supplies the average load current I_L and also a battery "trickle-charge" current I_B. Resistor R_S is calculated by the equation:

$$R_S = \frac{V_S max - V_{battery}}{I_L avg + I_B (\text{"trickle"})}.$$

In the event of a power line failure, the McMOS system can operate for relatively long time periods because of the low dissipation associated with the McMOS family. This type of supply can be used to power McMOS memories and provide a quasi-nonvolatile memory system.

The circuit in Figure 2-9 gives a good indication of how easily a CMOS power supply level can be derived from a high voltage dc source by using a resistor, a zener and a filter capacitor. The zener in this case is actually regulating the voltage rather than providing just overvoltage protection, as in the battery backup supply. Resistor R_S is again calculated from the dc supply voltage, the average load current I_L, and the necessary zener bias current I_Z. The capacitor C, is selected to supply the peak transient load current and maintain the minimum voltage V_{DD} required for the system operating speed.

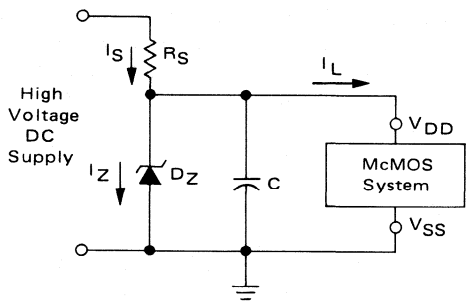


FIGURE 2-9 – DERIVING CMOS POWER FROM HIGH VOLTAGE DC SOURCE

NOISE IMMUNITY

CMOS devices exhibit a sensitivity to only negative-going noise spikes on the power supply line and to only positive-going spikes on the ground. However, bipolar logic families show various degrees of sensitivity to both positive and negative spikes on the power and ground lines, depending upon the output logic state of the device. The sensitivity of the CMOS device will vary as a function of the power supply voltage. This variation is due to the changing of the switching thresholds and the effects of supply voltage on the conductance of the internal MOS transistors. For additional information on noise margins and noise energy immunity of McMOS devices refer to Motorola Application Note AN-707.

THERMAL CONSIDERATIONS

Another advantage realized with McMOS device technology is excellent temperature stability. The "AL" series devices are designed to operate over the full military temperature range of $-55^oC \leqslant T_A \leqslant +125^oC$. Additionally, the commerical ceramic "CL" series and the plastic "CP" series package devices are designed to operate over an extended temperature range of $-40^oC \leqslant T_A \leqslant +85^oC$ (standard commercial range is only $0 \leqslant T_A \leqslant +70^oC$). This extended temperature range is a bonus to designers who do not want to pay the premium price of military temperature range devices for systems that must operate reliably in varying temperature environments. The two major categories of wide temperature range design considerations are package dissipation and specification variations with temperature.

PACKAGE DISSIPATION

CMOS devices consume almost negligible power in the quiescent state and increasing amounts of power in direct proportion to the capacitive load, the operating frequency, and the square of the power supply voltage. A normal CMOS digital system operating at moderate speed does not require special consideration of package dissipation capability.

Special cases invariably arise, however, when the designer is required to extend operation of particular devices to their limits (special load driving, high frequency operation, analog applications, input diode clamping, etc.). In addition, there are specially designed buffers and driver devices that have high current driving capability. Package dissipation and thermal management in these cases may become significant considerations to the designer. Therefore, it is advantageous to know the dissipation capability of standard McMOS packages, as described further.

THERMAL MANAGEMENT

Circuit performance and long term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low. Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. Therefore, the temperature increase depends upon the amount of power dissipated in the circuit and the resulting thermal resistance figure between the heat source and the reference point.

The average temperature at the junction is a function of the system ability to remove heat generated in the circuit (from the junction region to the ambient environment). The basic formula for converting power dissipation to estimated junction temperature is expressed as follows:

$$T_J = T_A + P_D \cdot (\theta_{JC} + \theta_{CA}), \qquad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}), \quad (2)$$

where:

T_J = junction temperature,
T_A = ambient operating temperature,
P_D = calculated power dissipation,
θ_{JC} = thermal resistance, junction to case,
θ_{CA} = thermal resistance, case to ambient,
θ_{JA} = thermal resistance, junction to ambient.

Only two terms on the right side of equation (1) can be varied by the user, namely the ambient temperature, and the device case-to-ambient thermal resistance, θ_{CA}.

Internally, the thermal resistance of an integrated circuit is a function of the package material and size and also the method used in bonding the IC die to the package. The worst case and typical thermal resistance values for some standard IC packages are given in Table 2-1. In Figure 2-10 this basic data is converted into a graph showing the maximum power dissipation allowable at various ambient temperatures for circuits mounted in the 14-pin and 16-pin plastic and ceramic packages; the data also considers the maximum permissible junction temperature for devices packaged in plastic or ceramic. These measurements are taken in still air without heat sinks, since moving air and heat sinking would decrease the value of θ_{CA}.

Package Description	θ_{JA} – °C/Watt (Still Air)		θ_{JC} – °C/Watt
	Worst Case	Typical	Worst Case
Plastic Dual-In-Line, 14 lead or 16 lead (Gold Eutectic Die Bond)	200	135	90
Ceramic Dual-In-Line, 14 or 16 lead (Gold Eutectic Die Bond)	155	100	50
Ceramic Dual-In-Line, 24 lead	100	70	35
Plastic Dual-In-Line, 24 Lead	140	95	50

TABLE 1 – WORST CASE AND TYPICAL THERMAL RESISTANCE RATINGS FOR SELECTED IC PACKAGES.

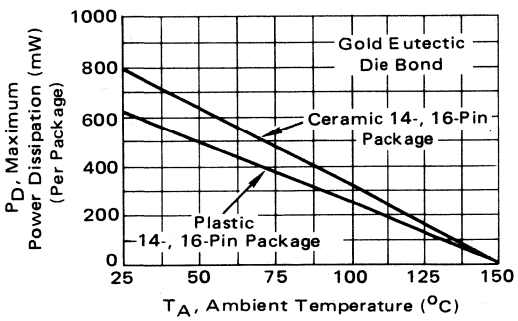


FIGURE 2-10 – AMBIENT TEMPERATURE POWER DERATING

SPECIFICATION VARIATION WITH TEMPERATURE

The fact that a logic family is designed to functionally operate over a wide temperature range does not necessarily mean that specifications will not vary with changes in the ambient temperature. A quick glance at the electrical characteristics section of a data sheet will verify that parameters such as output drive, quiescent power dissipation, and switching time parameters do indeed vary with temperature. Fortunately, these variations are predictable enough that a designer, with information included in this section, can interpolate and extrapolate the performance of the selected McMOS devices over their full temperature rating.

VOLTAGE TRANSFER CHARACTERISTIC VARIATIONS

An inherent advantage of the generic complementary MOS process is the tendency of the N- and P-channel thresholds to "track" together over wide temperature variations in such a manner that the input threshold to a CMOS device remains quite constant. As seen in Figure 2-11, the variation of threshold over the full military temperature range is typically less than five percent. By comparison, a bipolar threshold may vary as much as 40 percent.

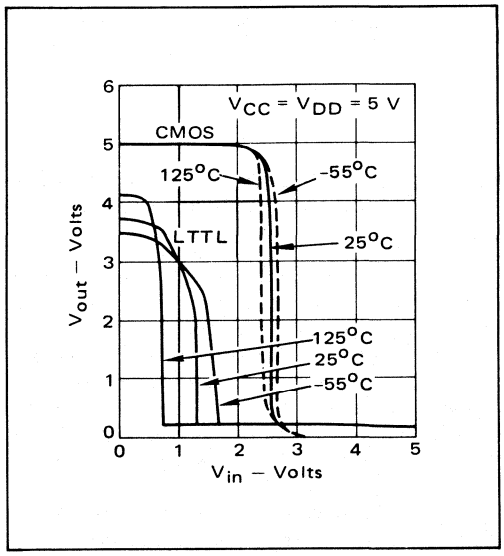


FIGURE 2-11 – TRANSFER CHARACTERISTICS OF THE CMOS INVERTER SHOWS MUCH LESS DEPENDENCE ON TEMPERATURE THAN DOES TTL.

Threshold variation over temperature becomes an important factor when determining worst case noise margins, but it is of greater concern in quasi-analog circuits such as 2-gate oscillators and "one-shot" multivibrators. The threshold levels in these types of circuits directly affect frequency, duty cycle, and time-out. Therefore, the stability of McMOS devices over temperature is a definite advantage in these "special" applications.

LEAKAGE CURRENT VARIATIONS

Leakage current plays an important role in quiescent power supply and three-state loading considerations. When designing a circuit which must operate over wide temperature ranges, the effect of temperature on leakage must be considered in worst case design.

Leakage, as previously described, is due primarily to internal reverse-biased P-N junction leakage. As such, the leakage increases exponentially with increasing temperature, as indicated by the formula:

$$I_L = (T_I) = I_L(T_O)\, e^{\Delta T/K},$$

where $I_L\,(T_O)$ is the leakage current measured at temperature T_O, K is the constant of the rate of increase, and the temperature change is $\Delta T = T_I - T_O$.

For silicon junctions, I_L doubles approximately every 10°C, thus making K_{Si} = 14°C. A CMOS device that has 5×10^{-9} ampere leakage at room temperature (25°C) may be expected to have 5×10^{-6} ampere leakage at 125°C.

CHANNEL RESISTANCE EFFECTS

Variations in the channel resistance of the P-type and N-type MOSFETs in a CMOS circuit affect several important device characteristics, namely current sinking and sourcing capability (I_{OL}, I_{OH}), switching through-current (I_{TC}), propagation delay (t_{PHL}, t_{PLH}), and output voltage rise and fall times (t_r, t_f).

The channel resistance of an MOS device is inversely proportional to the surface mobility of the majority carriers (holes in a P-type device and electrons in an N-type device). Since the mobility is a function of temperature, it is not surprising to find that channel resistance and thus, the current and switching time parameters change with variations in temperature.

The normalized graph of the current and switching parameters versus ambient temperature, Figure 2-12, should prove a useful tool to the designer in predicting the typical performance to be expected of a McMOS circuit at different temperatures.

INPUT RATINGS AND CONSIDERATIONS

The input of a Complementary MOS device is insulated from the MOSFETs channel regions by a thin layer of silicon dioxide (SiO_2). The high impedance and a 5 picofarad input capacitance make unconnected or floating inputs excellent energy storage nodes having the potential for large voltage buildups. The Motorola McMOS process uses resistor-diode gate-protection networks to siphon the accumulated energy away from the MOS transistors and thereby prevent permanent damage to the input gate oxide regions. In addition to device handling precautions, other user considerations include device maximum ratings, termination of unused inputs and input signal waveforms.

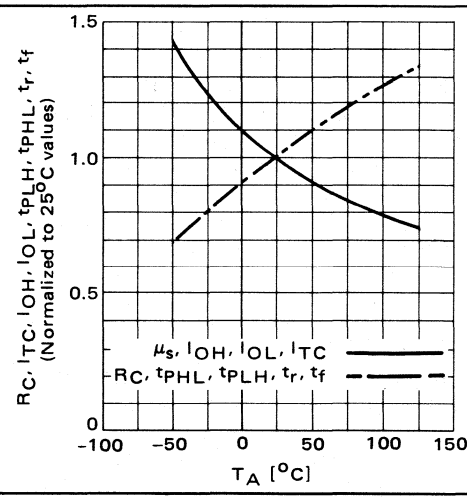


FIGURE 2-12 –NORMALIZED PLOT OF TYPICAL SINK-CURRENT (I_{OL}), SOURCE-CURRENT (I_{OH}), THROUGH-CURRENT (I_{TC}), SURFACE MOBILITY (μ_s), CHANNEL RESISTANCE (R_C), PROPAGATION DELAY TIMES (t_{PHL}, t_{PLH}), AND RISE AND FALL TIMES (t_r, t_f) versus AMBIENT TEMPERATURE (T_A)

INPUT VOLTAGE

To prevent a destructive high-current mode, caused by forward biasing the input protection diodes, the signal voltage V_{in} must be confined to the range of $V_{SS} \leqslant V_{in} \leqslant V_{DD}$. The input thresholds establish the maximum input LOW signal voltage V_{NL}, and the minimum input HIGH signal voltage V_{NH}. These thresholds are specified as a dc noise margin and are defined as the maximum

voltage change from an ideal logical "1" or "0" input level, which will not produce a change of state at the output. The guaranteed noise margin for standard Motorola McMOS devices is 30% of V_{DD} with a typical value of 45% V_{DD}.

To illustrate, the ideal "0" and "1" input levels are V_{SS} and V_{DD}, respectively. Therefore (using positive logic notation), using the formula $V_{IL} = V_{SS} + 0.3\ V_{DD}$ equals the guaranteed minimum maximum input logic "0" threshold level, and V_{IH} is equal to 0.7 V_{DD} or the guaranteed maximum minimum input logic "1" level. Typical values are: $V_{IL} = V_{SS} + 0.45\ V_{DD}$, and $V_{IH} = 0.55\ V_{DD}$.

The calculations relate that if the input level V_{in} is in the range $V_{SS} \leqslant V_{in} \leqslant V_{SS} + 0.3\ V_{DD}$, the output level V_O is guaranteed not to have changed state and will be within the range of 0.7 $V_{DD} \leqslant V_O \leqslant V_{DD}$ for inverting functions, or within the range of $V_{SS} \leqslant V_O \leqslant V_{SS} + 0.3\ V_{DD}$ for non-inverting functions. For a further description of thresholds and noise margin see Motorola Application Note AN-707.

INPUT CURRENT

The very high input impedance (typically 10^{12} ohms) requires an almost negligible source or sinking drive. The typical input current I_{in}, is 10 pAdc. However, there are many system designs that utilize the input protection diodes to clamp the signal levels. In these applications, it is necessary to limit the input currents to the ±10 mAdc maximum rating per package pin. This 10 mA maximum rating also applies to the V_{DD} and V_{SS} pins. Therefore, if the device has four inputs (all of which may be HIGH forward-biasing the input diodes) the current limit on each input would be 10 mA divided by 4 or 2.5 mA. The same reasoning applies if more than one input is below the V_{SS} level.

UNUSED INPUTS

A problem associated with floating CMOS device input pins occurs after the device is installed in an operating system. Energy injected through stray external circuit wiring capacities produces unpredictable, time-varying input values. Power dissipation increases, since the input gates tend to spend more time in their active, biased-ON region. As a result, the uncertainties of the gate logic states combine and cause system failure. This problem is eliminated if all unused CMOS input pins are connected to the appropriate power supply bus.

The proper termination level is determined by the truth table of the device being used. In the case of multi-input gates, it is recommended that unused NAND inputs be connected to V_{DD} and unused NOR inputs be connected to V_{SS}. This will improve reliability and provide maximum device input performance. If an entire gate or portion of a device is not used, it is still necessary to terminate the inputs even though the output is not loaded.

INPUT RISE/FALL TIMES

Special consideration must be given to the specified worst case maximum (slowest) clock input rise and fall times for edge triggered devices such as flip-flops, shift registers and counters. The specified values vary from 5 μsec to infinity and the system designer should consult the device data sheet for this parameter. A description of input waveforms will be presented later.

INPUT PROTECTION NETWORKS

The system designer must remain aware that MOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide regions. Normally the gate oxide is 1000 Å to 1200 Å thick; this range also defines a maximum potential difference that can be tolerated across the gate oxide. The gate oxide breaks down at a gate-to-substrate potential of about 100 V and results in permanent damage to the device.

Unfortunately, the electrical environment during pc board or socket insertion and device handling is very hostile. For example, static voltages generated by a person walking across a common waxed floor, have been measured in the 4 to 15 kV range (depending on humidity, surface conditions, etc.). These static voltages are potentially disastrous when discharged into a CMOS input considering the energy stored in the capacity (≃300 pF) of the human body at these voltage levels. There are two methods used for input protection: a single diode protection method and a double diode-resistor configuration. Both methods provide adequate input protection and all McMOS devices use one of these two protection methods.

Present McMOS gate protection structures can generally only protect against overvoltages in the hundreds of volts range. This is usually sufficient for "in-socket" overvoltage, but an order of magnitude less than that typically found in the handling environment. Following are some suggested handling procedures for McMOS devices.

- Store unused devices in conductive foam, conductive rails, or connect all leads together using a similar electrical shorting method.
- Use grounded tip soldering irons.
- Ground all test equipment.
- All low impedance equipment (such as pulse generators, etc.), should be disconnected from device inputs before dc power supplies are turned-off.
- All unused device inputs should be connected to V_{DD} or V_{SS}.

SINGLE DIODE METHOD

Figures 2-13(a) and 2-13(b) show the single diode protection method. Since the P-tub and the N-substrate are lightly doped, the junction breakdown is high and typically 120 V. Therefore, a heavily doped N+ region and a lightly doped P– region are used for the diodes. The junction between

these two regions (N+ and P–) breaks down at approximately 30 V, and is well below the 100 V gate-to-substrate breakdown.

The single diode method provides protection by clamping positive levels to V_{DD}. Negative protection is provided by the 30 V reverse breakdown. The diode is designed to operate in the breakdown region without damage, provided currents are kept under 10 mA.

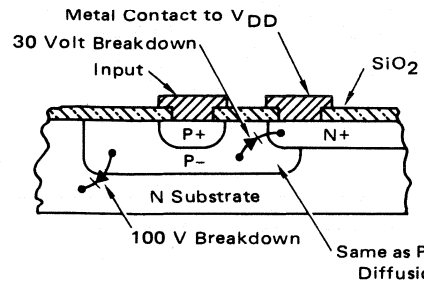


FIGURE 2-13(a) – PHYSICAL DIAGRAM, SINGLE DIODE PROTECTION METHOD

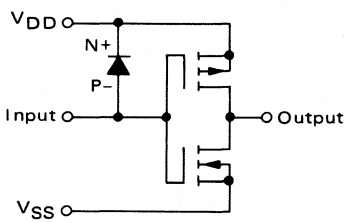


FIGURE 2-13(b) – SCHEMATIC DIAGRAM, SINGLE DIODE PROTECTION METHOD

DIODE-RESISTOR METHOD

The second method, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and V_{SS}, respectively. Figures 2-14(a) and 2-14(b) show the circuitry and diffusion cross-section for the diode-resistor protection method.

The input protection circuit consists of a series isolation resistor R_S, whose typical value is 1.5 k ohms, and diodes D1 and D2, which clamp the input voltages between the power supply pins V_{DD} and V_{SS}. Diode D3 is a useful distributed parasitic structure resulting from the diffusion fabrication of R_S.

In addition to circuit isolation, the series resistor R_S produces a small propagation delay due to the 5 pF gate capacitance. This delay (typically 6 to 7 ns) allows excess energy present at the input terminal to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 are both of the N+, P– type and have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) overvoltage protection, with respect to V_{SS} (V_{DD} – open circuit), is provided by diode D1. Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) overvoltage protection with respect to V_{DD} when V_{SS} is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric.

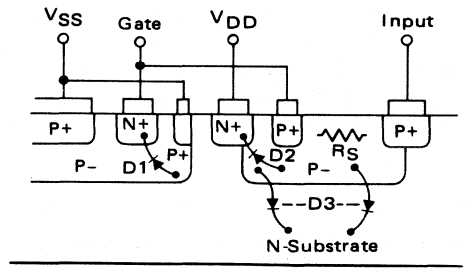
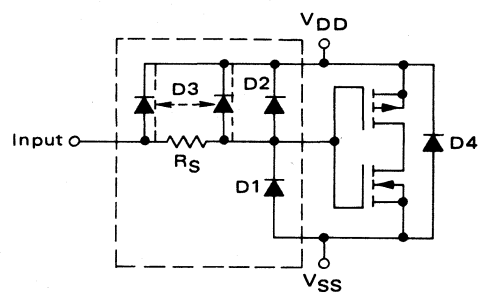


FIGURE 2-14(a) – PHYSICAL DIAGRAM, DIODE-RESISTOR INPUT PROTECTION METHOD



Added Protection Circuitry At Each External Input lead

Notes:
R_S = 1.5 kΩ Nominal
Avalanche Voltages:
BVD1 = 30 V
BVD2 = 30 V
BVD3 = 80 V
BVD4 = 120 V

FIGURE 2-14(b) – SCHEMATIC DIAGRAM, DIODE-RESISTOR INPUT PROTECTION METHOD

USING THE INPUT DIODES IN CIRCUIT DESIGN

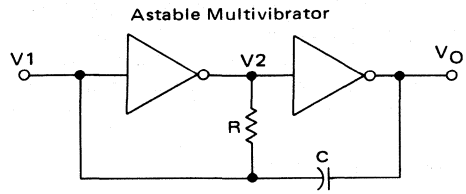
Circuits such as integrators, differentiators and oscillators may forward bias the input protection diodes and actually depend on them to clamp the input signal levels. The forward bias currents generated by such circuit configurations is limited by the impedance and drive capability of the driving device and generally will not exceed the input limitations.

An application that requires consideration, as to the single diode versus the diode-resistor input method, is the two stage oscillator shown in Figure 2-15.

Waveforms for the single diode input network show that the diode clamps the input voltage V1

to the positive V_{DD} voltage. The negative portion of V1 is not limited (the protection diode has not avalanched) and will go negative with respect to V_{SS} by the magnitude of the threshold voltage V_T. This effect will cause the time t_1 to be less than time t_2 and will give the output waveform V_O a duty cycle less than 50%.

The waveforms for the diode-resistor input method show that the input signal V1 is limited to both the V_{DD} and V_{SS} supply voltages. In this case, times t_1 and t_2 are approximately equal, the duty cycle is 50% and the output period T is less than the period of the output for the single diode device.



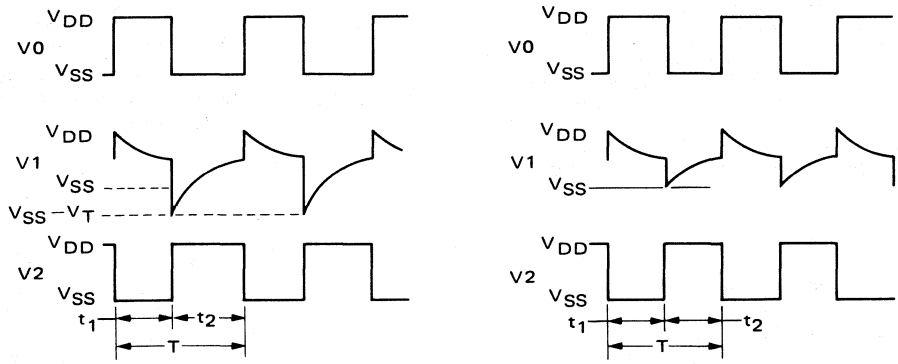
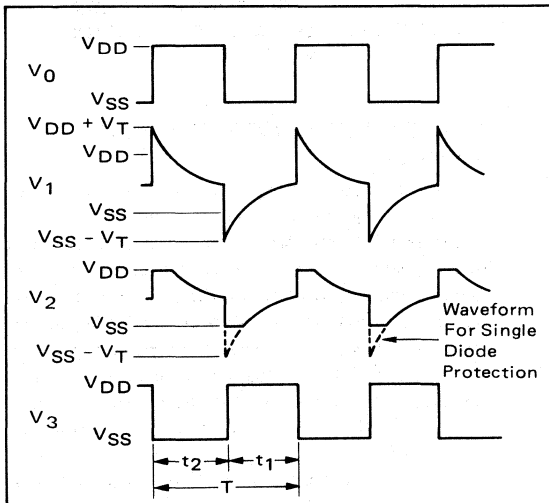


FIGURE 2-15 – WAVEFORM COMPARISON OF INPUT METHODS

Figure 2-16 shows the same astable circuit as Figure 2-15 with the addition of a compensating resistor R_S. Besides compensating for input threshold and power supply variation, resistor R_S also provides isolation from the input protection network. The waveforms illustrate that times t_1 and t_2 are approximately equal and the period T will not vary (as a function of the type of protection circuit the input device has).



The inputs to McMOS devices can be driven with signals outside the range of V_{SS} to V_{DD} if a series resistor is used to limit the current to less than the 10 mA maximum. However, consideration must also be given to the increase in rise, fall and propagation delay times produced by the series resistance and the 5 pF input capacitance. This technique obviously should not be used on the inputs of edge-triggered devices. It is recommended that the inputs be buffered by an additional gate for these devices.

The 10 mA input current limit is established by the device internal metalization. Exceeding the 10 mA limit will cause metal migration and possible long term degradation of the device lifetime.

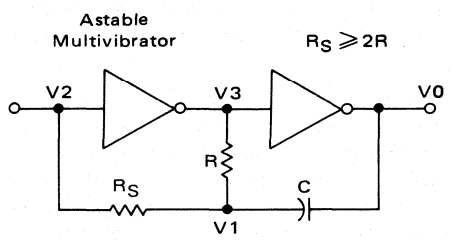


FIGURE 2-16 – DIODE-RESISTOR INPUT METHOD WITH ADDITION OF COMPENSATING RESISTOR R_S

INPUT WAVEFORMS

The 10 to 90% maximum clock transition time for sequential circuits is normally specified in the 5 to 15 μsec range, depending upon the supply voltage used; data ripple-through, false triggering problems, etc. occur above these values. As the system transition times approach these limits, potential timing problems and increased power dissipation levels should be considered.

The possible 15 to 20% process variation in input threshold voltage among random device samples could lead to clock-skew problems, even in synchronous logic systems where clocking is not normally a problem.

As in the example in Figure 2-17, a fairly long clock rise time could produce data ripple-through on the cascaded edge-triggered storage elements. As long as the edge-sensitive clock transition time (t_rC) is confined to a value of less than the sum of the propagation delay time of the driving output stage (for the estimated capacitive load) and of the hold-time of the following parallel clocked device as shown in Figure 2-17, there will not be a problem.

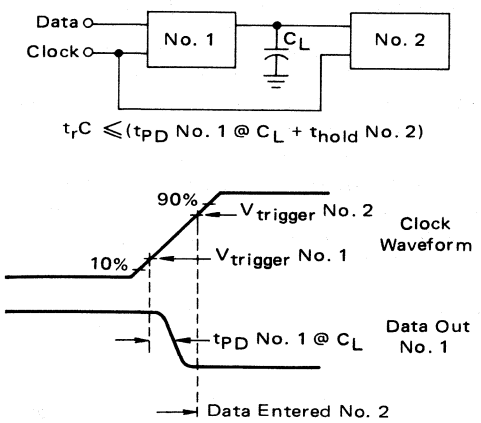


FIGURE 2-17 – SYNCHRONOUS OPERATION LIMITED BY CLOCK TRANSITION TIME

The maximum t_rC transition time due to skew effects could be in the 100 nsec range for the worst case situation of high speed devices having maximum allowed threshold voltage deviations. As clock transition times increase, system power needs also increase; this action results because the logic elements are exhibiting longer periods of time in the active (higher power) operating region.

Schmitt trigger circuit configurations can be utilized for wave shaping very slow external input signals and also provide a decrease in input power dissipation and an increase in overall system performance. The MC14583 dual Schmitt trigger is an ideal solution to applications requiring such wave shaping. Other Schmitt tirgger designs can be found in the articles referenced in the supplementary literature section of this data book.

Several of the McMOS counter and shift register designs incorporate input circuitry having a Schmitt trigger type hysteresis which also eliminates the requirement of a maximum input rise time specification. These counters are very useful for generating a system clock from the common 60 Hz power line frequency. The inputs of such devices can be connected directly to the 120 Vac line through a series connected 1 megohm resistor. A capacitor must also be added between the device input and the V_{SS} pins to absorb the kilovolt line spike energy commonly found on many power lines. The rectification of the ac input voltage is again performed by the internal protection diodes and the current is limited by the series resistor.

OUTPUT LOADING CONSIDERATIONS

Like any logic family, McMOS is limited in the amount of current (sink and source) drive capability while still maintaining a defined logic state. McMOS device output current characteristics are found in a set of curves (refer to Figure 2-18) defined as output drain characteristics. The logic designer should consult these curves when designing specialized systems requiring high current drives. These drain characteristics vary as a function of voltage and temperature and have an effect on the maximum operating speed of the logic system.

OUTPUT CHARACTERISTICS

As shown in Figure 2-18, McMOS N- and P-channel enhancement mode transistors have two basic regions of operation, saturated and non-saturated. The boundary between the two regions is the locus of points at which the drain-to-source voltage (V_{DS}) is equal to the gate-to-source voltage (V_{GS}) minus the device threshold voltage (V_T).

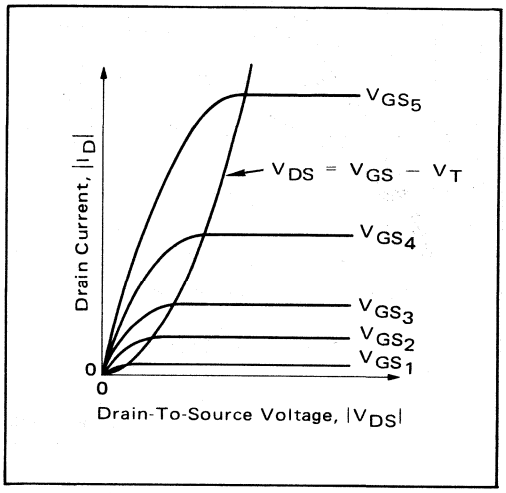


FIGURE 2-18 – OUTPUT DRAIN CHARACTERISTICS

In the non-saturated region, the characteristics of the MOSFET are similar to a resistor; the impedance of the channels is approximated by the slope of the curves. The current in this region is given by the equation:

$$I_D = 2K\,(V_{GS} - V_T)\,V_{DS} - K\,V_{DS}^2,$$

where K is a constant dependent upon processing parameters and the channel geometry.

In the saturated region, the MOSFET behaves similar to a current source as illustrated by the constant drain current independent of the drain-to-source voltage. The currents in the saturated region are given by the equation:

$$I_D = K\,(V_{GS} - V_T)^2.$$

The maximum drain current I_D is almost proportional to the square of the gate-to-source voltage V_{GS}. In Motorola McMOS logic, the gate-to-source voltage is limited to the power supply voltage ($V_{DD} - V_{SS}$). Hence, it can be stated that the drive capability of McMOS is proportional to the square of the power supply voltage.

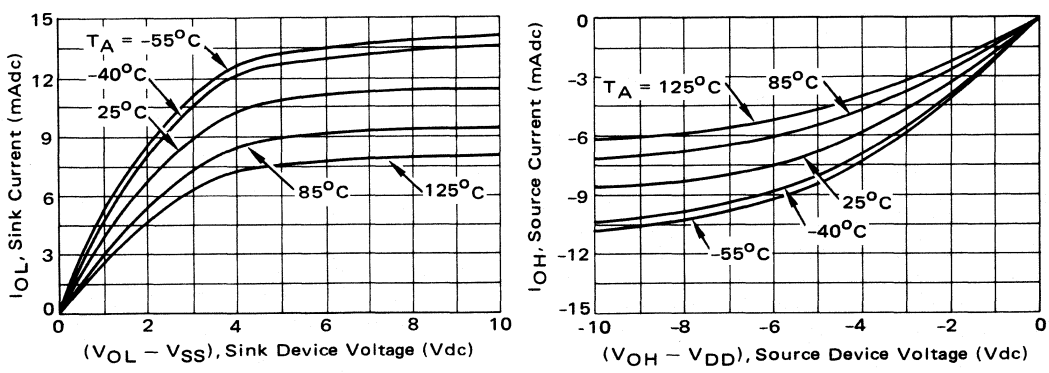
The output drain characteristics also vary as a function of temperature as shown in Figure 2-19. The typical characteristics for a standard McMOS output N-channel device, operating with a supply of 10 volts, is shown in Figure 2-19(a). The complementary P-channel characteristics are shown in Figure 2-19(b). For device temperatures above 25°C, the decrease in drain current can be approximated by a negative temperature coefficient of approximately -0.3%/°C. Refer to Figure 2-12 for a curve of the change in drain current versus temperature.

CONSIDERATIONS AND PRECAUTIONS

The standard McMOS input is capacitive and requires approximately ±10 pA of drive current. Thus, the fan-out on a current basis is in the order of 10^6 devices. The actual fan-out of a McMOS device is limited only by a capacitive load consideration based upon the desired system operating frequency.

Assume that a capacity-loaded McMOS gate has an input signal with almost zero transition time. The output device then charges (or discharges) the load capacitance along the drain characteristic curve for V_{GS} and exits from the saturated region ($V_{DS} = V_{DD}$) to the non-saturated region ($V_{DS} = 0$). This means that initially the voltage across the capacitor changes in a linear fashion due to the constant current I_D(sat). As the drain-to-source voltage V_{DS} decreases to less than that defined for saturation, the current to the load decreases. At this point, the voltage change on the capacitor is no longer linear and, as a result, slows down "rounding off" the rising or falling output waveform as it approaches its limits of V_{DD} or V_{SS}, respectively.

Since the capacitance $\frac{dv}{dt}$ is a function of drain current I_D, the output rise/fall times and also the system operating speed will be limited by the McMOS supply voltage. Operating temperature, because it effects the maximum drain current, will also limit system speed. Considerations on system speed with respect to capacitance, voltage and temperature will be described later in Chapter 2 under the heading Operating Speed.



Curve (a) N-Channel

Curve (b) P-Channel

FIGURE 2-19 – TYPICAL OUTPUT CHARACTERISTICS FOR V_{DD} = 10 VOLTS AS A FUNCTION OF TEMPERATURE

The outputs of a McMOS device consist of a complementary pair, one device for sourcing current and another for sinking current. The outputs of a McMOS device cannot be connected in a "wire-OR" configuration because of the complementary pair configuration. Three-state logic will be described later in Chapter 2.

Many times temporary shorts result from testing mistakes or improper board assembly. When such excessive currents flow and the chip temperature increases, the short circuit current will decrease because of the negative temperature coefficient. This "built-in" thermal protection will usually prevent burn-out on a short term basis. In general, devices with standard family output characteristics can be shorted to the supply rails, provided the supply voltage is 5 volts or less; at this supply voltage, saturation currents are less than the maximum device ratings of 10 mA per pin. Precautions are necessary when using the high current buffers or operating with high supply voltages so that the maximum device current and dissipation limits are not exceeded.

The McMOS drive capability is limited if the outputs are required to maintain a specified logic level. However, if the output is used to drive a discrete device such as a transistor or LED, large currents (within maximum ratings) can be achieved by operating the device in the saturated region. Details on interfacing to other devices will be described shortly.

INTERFACING TECHNIQUES

There are many digital system designs which require low-power dissipation McMOS devices to be integrated with devices of other semiconductor technologies. This raises the question of how to interface between McMOS and other logic families. Most logic families have a compatible set of input-output parameters defined in terms of family unit loads specified at a restrictive or tight tolerance power supply voltage. The McMOS guaranteed power supply operating range of 3 to 18 volts encompasses all of the significant logic families available today. This operating range, together with the simplicity of the input and output characteristics, makes the McMOS technology particularly easy to interface with devices of other technologies. The interface techniques to be described assume the following initial conditions.

1. The power-supply voltage level and tolerances are chosen to accommodate the interfaced logic elements, since McMOS integrated circuit devices will operate over a much wider voltage range.
2. The logic levels at the interface between McMOS and other logic elements will meet or exceed the specified worst case logic levels of the other elements.
3. Fan-in and fan-out rules at the interface shall be derived from the current sinking or sourcing capability of the driving elements.

By adopting these three conditions, the designer can ensure appropriate noise margins at the interface between dissimilar elements.

INTERFACING McMOS WITH TTL, DTL

Since both the DTL (diode-transistor logic) and TTL (transistor-transistor logic) bipolar digital IC families require only a single supply, McMOS devices are well-suited for use with DTL and TTL logic forms. There are two major considerations when interfacing McMOS with bipolar logic elements. The first consideration is whether McMOS can sink the input current requirement of the bipolar logic. The second consideration is whether the output logic levels of the bipolar devices are compatible with the McMOS input threshold levels.

Figure 2-20 shows the input/output level and current requirements of McMOS/bipolar interfaces. For a logic "0" input, the standard medium power TTL and DTL devices have a current sink drive requirement of 1.6 mA at a level of 0.4 volts. Standard gate McMOS devices will not sink 1.6 mA of current. To increase the output current sinking capability of the McMOS device, a 2-input or 4-input McMOS NOR gate could be used with all the gate inputs tied together in parallel. For higher fan-outs, the use of buffer devices (as shown in Figure 2-20) is recommended. These buffers are capable of driving two medium power TTL or two DTL loads with an I_{OL} of 3.2 mA at 0.4 volts. By paralleling the inputs and outputs of the McMOS buffers, even large fan-outs can be obtained. The logical "1" output of any McMOS device has no difficulty driving any TTL or DTL device since the V_{OH} level of 4.5 volts (while sourcing the microampere leakage of the bipolar devices) is 2.5 volts higher than the 2.0 volt V_{IH} input level.

Low-power TTL (LTTL) logic requires a current sinking drive of 0.18 milliamperes at a voltage level less than 0.3 volts. As shown in Figure 2-20, any standard gate McMOS device will drive one LTTL load over the full military temperature range. However, in most cases, two LTTL loads can be driven over the full temperature range. Further, at 25°C any McMOS device will typically drive 4 LTTL loads without burden. The Motorola McMOS buffers are capable of at least 10 LTTL loads over the full temperature range. In the non-saturated mode, as is the present case, the drain current is directly proportional to the drain to source voltage. Therefore, higher fan-outs than the number guaranteed on the data sheet can be obtained with some sacrifice in noise immunity over extended temperatures.

When interfacing bipolar logic to McMOS, the primary consideration is whether the bipolar output levels are compatible to the McMOS input thresholds. The guaranteed McMOS thresholds for a logic "0" or "1" input are respectively 30% and 70% of the power supply voltage; further, with a 5 volt supply this is 1.5 volts and 3.5 volts, respectively. The bipolar V_{OL} level of 0.4 volts is more than capable of driving a McMOS device

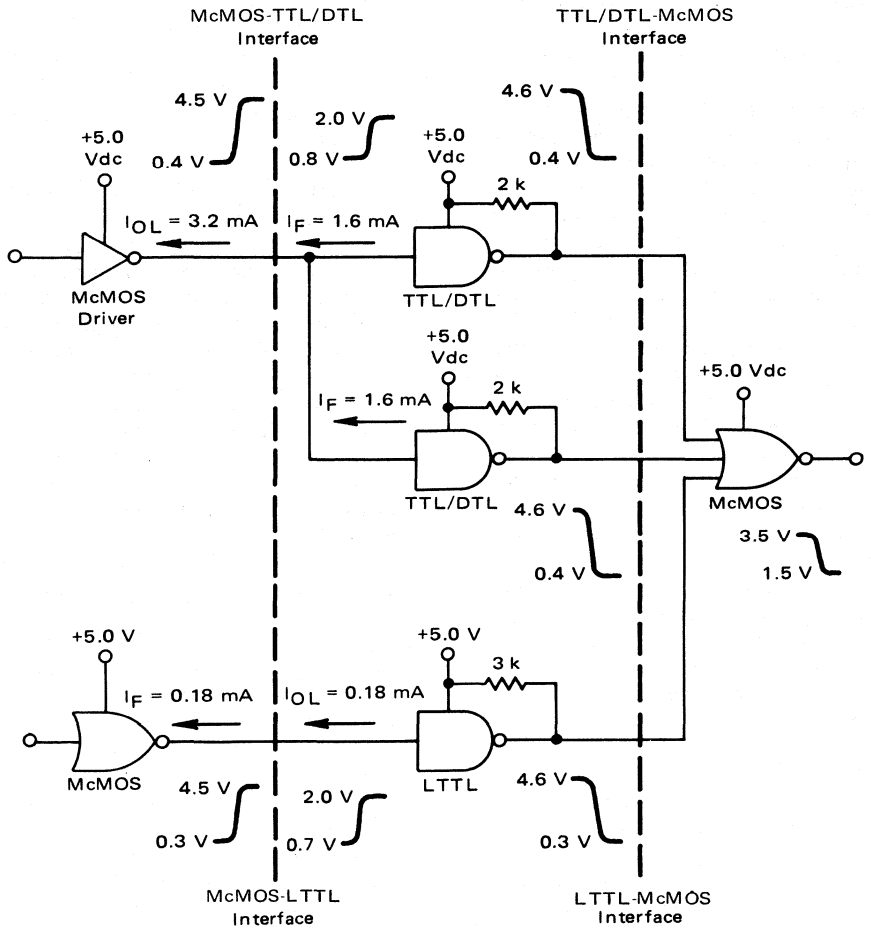


FIGURE 2-20 – McMOS/BIPOLAR SYSTEMS INTERFACE

input to a logical "0" level. The major area of concern is the logic "1" state. The V_{OH} level of TTL/DTL devices is generally specified at 2.4 volts while sourcing 400 μA. This is an absolute worst case bipolar specification and since McMOS inputs only require about 10 picoamperes drive current, the typical V_{OH} level of a bipolar active pull-up output driving McMOS would be equal to approximately two P-N junction voltage drops below V_{CC}, or typically 3.6 volts. This level is greater than the required 3.5 volt input of McMOS; however, there is very little noise margin. For this reason, it is recommended that a pull-up resistor be added to the circuit from the bipolar output to V_{CC} as shown in Figure 2-20. Resistor values of 2 k ohms for TTL/DTL (or 3 k ohms for LTTL) provide satisfactory pull-up and very satisfactory input rise times to the McMOS device. It should be noted that when utilizing a bipolar-to-McMOS interface, the driver should not fan-out to bipolar circuits, only to other McMOS devices. However, when using a McMOS-to-bipolar interface, fan-out may include both bipolar and McMOS devices. As can be seen in Figure 2-20, the noise margins at the collective interface either maintain or exceed the 0.4 volt dc margins of the bipolar logic families. In general, the noise margin at the interface between CMOS and other 5 volt logic systems is higher than that of the bipolar system alone. This situation exists because of the higher positive logic levels at the CMOS interface.

Five volt operation of McMOS restricts the

maximum speed capability, and in many systems where speed is of importance McMOS may be powered with a supply voltage of 15 volts. Figure 2-21 shows the techniques used to interface McMOS devices operating at 15 volts with 5 volt bipolar devices. Here the "down" translation is easily achieved by using the McMOS buffer translators specifically designed for this application.

The "up" translation can be performed by using one of two different methods. One method uses a high voltage, open collector TTL gate such as the MC7406 with a pull-up resistor to the 15 volt V_{DD} supply. The value of the pull-up resistor must be considered in relation to system speed. Since a McMOS input loading is typically characterized by 5 picofarads, the rise time at the 7406-McMOS interface will be determined by the resistor and the number of McMOS loads. High speed and fast rise times may dictate the use of low resistance values and a significant increase in power dissipation.

The second method of "up" translation has a reasonable power dissipation while still maintaining an acceptable rise time. The device used in this method is a MHTL, MC666 level translator. This device is an active pull-up, bipolar High Threshold Logic (HTL) component which has inputs for translating from RTL, DTL or TTL operating levels to 15 volt logic levels.

McMOS device series since typical power dissipation ratings have less than 2 microwatts per gate.

The McMOS series can also be used to expand the MHTL generic designs by providing the complex functions (expansion) for MHTL. The only prerequisite is that proper interface of the two logic types be implemented as shown in Figure 2-22. Both logic types operate from a single +15 Vdc supply. The output logic levels of the typical McMOS gate are made equal to input of the MHTL circuit (i.e., V_{OH} = 13.5 volts and V_{OL} = 1.5 volts for the high and low levels, respectively). Since the MHTL gate responds only to signals that exceed the input logic levels (V_{IH} = 8.5 volts and V_{IL} = 6.5 volts), the full MHTL 5.0 volt noise margin is maintained at the interface. The number of MHTL circuits that can be driven by a typical McMOS gate (fan-out) is determined from the output characteristics. Each MHTL input represents a load current (I_{OL}) of approximately 1.2 milliamperes. The McMOS output voltage (V_{OL}) will remain below 1.5 volts when the device sinks 1.2 milliamperes; this corresponds to a fan-out of the one MHTL load.

Interfacing the MHTL gate to drive McMOS circuits (fan-in) is a somewhat different design consideration. Because the input current to a driven McMOS gate is negligibly small, an MHTL circuit can drive a very large number of McMOS inputs

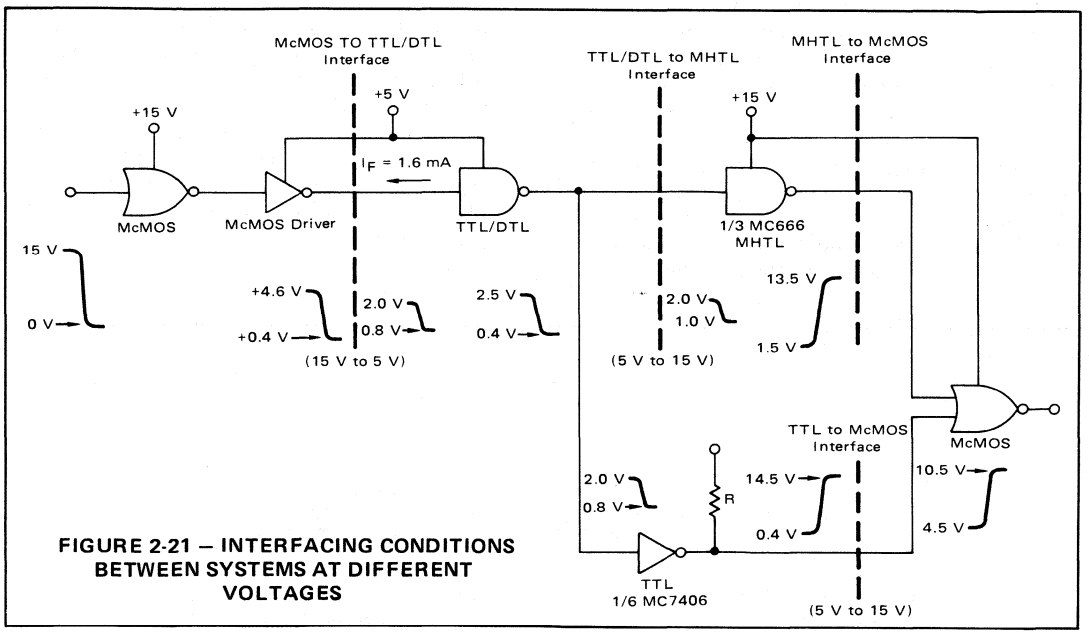


FIGURE 2-21 – INTERFACING CONDITIONS BETWEEN SYSTEMS AT DIFFERENT VOLTAGES

INTERFACING McMOS WITH MHTL

McMOS functions can be used to expand the versatility of standard, industrial high threshold logic systems where a large signal swing and high noise immunity are important. MHTL is generically limited in per device functions by an inherently high power dissipation which is typically 25 mW per logic gate. The condition does not exist in the

(50 or more). However, since the input to a McMOS gate is essentially capacitive (about 5 pF per input) and the internal load resistor of passive MHTL circuits is 15 k ohms, this capacitive loading effect could add an RC time constant of 75 nanoseconds per fan-out. Therefore, the number of McMOS circuits that can be connected is limited primarily by the system dynamic response.

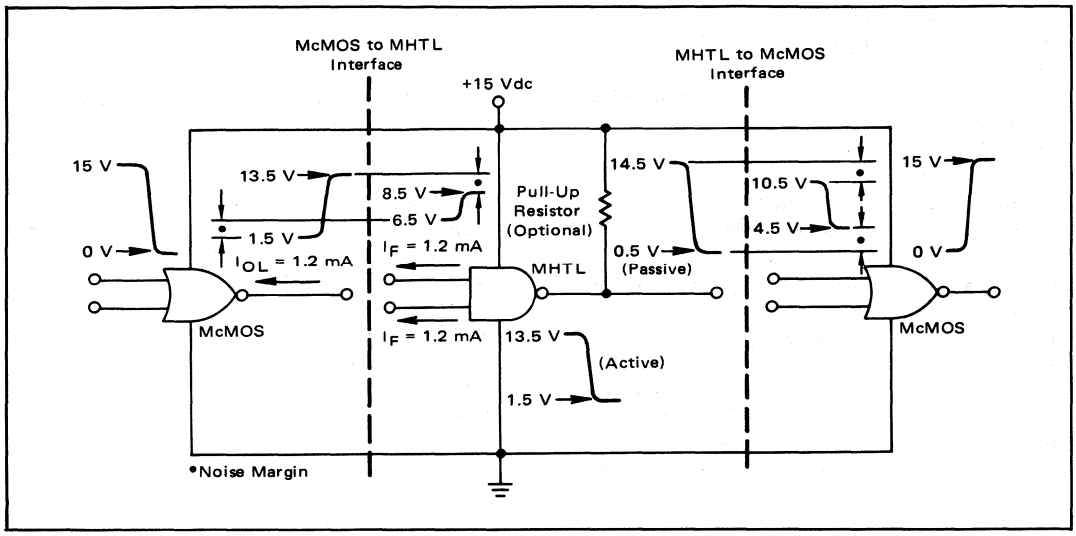


FIGURE 2-22 – INTERFACING CONDITIONS BETWEEN McMOS AND MHTL CIRCUITS

For this reason, a pull-up resistor is recommended at the output of the MHTL circuit to improve speed. Values range from 1.5 k ohms to 5 k ohms, depending on the desired switching speed, allowable power dissipation, and the desired noise immunity factor. A low value pull-up resistor will raise the V_{OL} output level and increase power drain, but it can also increase switching speed by as much as 85 percent. The best compromise appears to be the use of a passive output HTL circuit with an inherently low saturation voltage and a moderate value (2 k to 3 k ohms) external pull-up resistor. An active pull-up MHTL circuit will also drive a large number of McMOS gates with adequate speed, but both the high-noise and low-noise margins will be reduced.

Because McMOS and MHTL can interface directly with each other, they serve to complement one another in system designs where noise immunity or high voltage operation is important. MHTL provides pulse shapers, high current drivers and other interface elements while McMOS will provide complex functions which cannot be economically built with MHTL. Figure 2-23 shows the organization of a system design using McMOS and MHTL with some recommended MHTL interface component types.

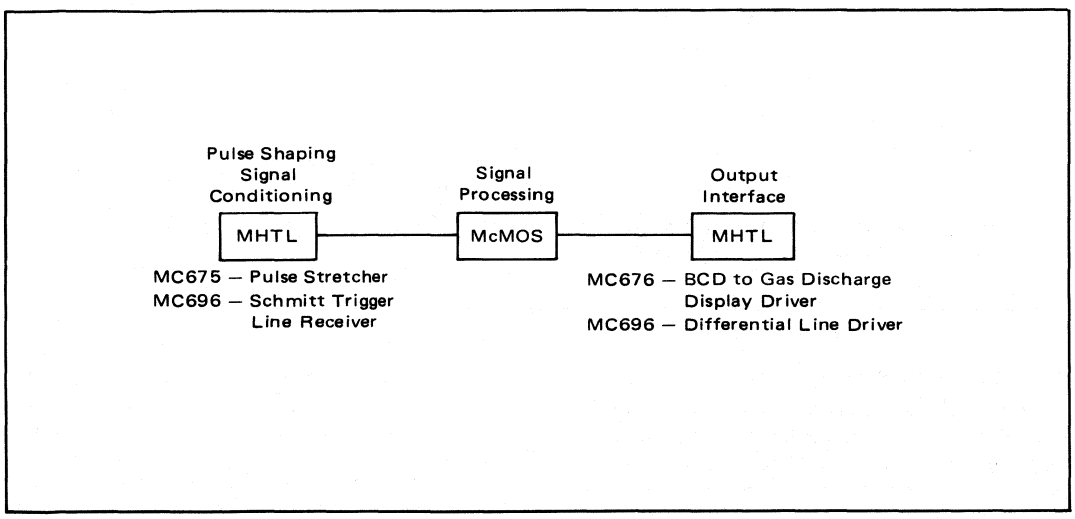


FIGURE 2-23 – USING A COMBINATION OF McMOS AND MHTL

INTERFACING McMOS WITH MECL

In systems with McMOS and MECL negative voltage power supplies are commonly used. The McMOS series can operate at -5.2 V (the MECL supply) or at higher voltages. The advantage of using the higher voltages is that McMOS can operate at higher speeds.

The interface from a McMOS output to MECL levels is shown in Figure 2-24(a). Note that the McMOS operates between ground and $-V_{SS}$; V_{SS} can be any voltage within the range of the McMOS device (18 V maximum). The McMOS output directly drives the MECL 10,000 input. If V_{SS} is greater than -5.2 V, a diode clamp is required to prevent the MECL input from dropping more than a diode voltage drop below the -5.2 V (V_{EE}).

The MECL 10,000 input requires a current of 265 μA (maximum worst case) and has input threshold voltages of V_{IHA} = -1.105 V and V_{ILA} = -1.475 V (25°C). The noise margin is therefore in excess of 225 mV in the high state and 4.3 V in the low state.

Level translation is required to drive a McMOS input with a MECL device. The 800 mV voltage output swing of MECL is not sufficient to drive a McMOS input. The MECL 10,000 output is used to switch a transistor to drive the McMOS input (Figure 2-24(b)). The high MECL output level (-900 mV typical) is not sufficient to forward bias the transistor (V_{BE} + V_{diode}). The low output level of −1.7 V typical turns on the transistor and pulls the McMOS input to within 800 or 900 mV of ground. If V_{SS} = -5.2 V, the transistor switches from -0.9 V to -5.2 V. The high level noise margin will be approximately 0.66 V and the low level noise margin will be approximately 1.56 V. With a greater V_{SS}, noise margins will be correspondingly larger.

INTERFACING McMOS WITH OTHER MOS TECHNOLOGIES

Other than CMOS, the most common Metal Oxide Semiconductor technology available today are the P-channel high threshold (PMOS) components. Becoming more common are low threshold devices (silicon gate and <100> devices). The main difference between the two MOS types is the supply voltage necessary for operation. Typical high threshold supplies are V_{SS} = 0 V, V_{DD} = −13 V and V_{GG} = −27 V. Corresponding low threshold supplies are V_{SS} = +5 V, V_{DD} = −5 V and V_{GG} = −12 V. Another important difference is that high threshold devices generally use negative logic convention ("0" is the most positive level and "1" the most negative) while low threshold devices use positive logic convention. The typical output swing for both high and low threshold devices goes from V_{SS} to V_{DD} when driving the high input impedance McMOS logic function.

The wide supply range of McMOS and the high

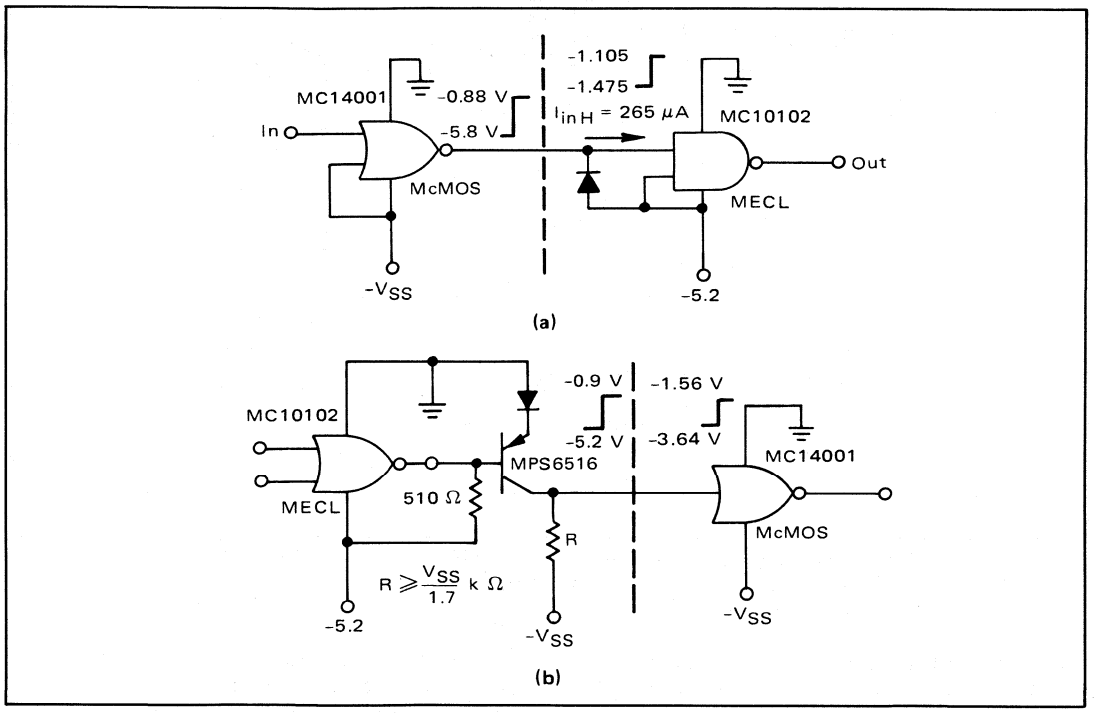


FIGURE 2-24—McMOS–MECL AND MECL–McMOS INTERFACE SYSTEMS

input impedance of MOS and McMOS devices make interfacing a simple matter. Figure 2-25(a) shows a McMOS to high threshold PMOS interface while Figure 2-25(b) shows a McMOS to low threshold PMOS interface.

Another technology commonly used in many logic systems today are N-channel MOS (NMOS) devices. NMOS like PMOS, is available in both the metal gate and silicon gate processes. Very large memories, such as the MCM6570 8192-bit Read Only Memory, are manufactured using the NMOS process.

Although NMOS devices operate using conventional positive logic with positive power supplies in the 5 to 15 volt range (with the exception of a small negative back-bias supply) and use positive logic convention, special consideration must be used when interfacing with McMOS devices. The positive voltage power supplies necessary for NMOS are also compatible with McMOS devices; further, the McMOS devices are normally operated with V_{DD} at a positive voltage and V_{SS} at ground potential. An area of concern to the designer exists when a system requires interfacing NMOS and McMOS. The concern applies primarily to the NMOS device inputs. Several NMOS devices are manufactured with TTL type inputs which use internal pull-up devices. This manufacturing technique requires the designer to use TTL levels and associated sinking requirements to drive the NMOS devices. If this is the case with the NMOS device to be interfaced, regular McMOS gates will not drive the device and a McMOS driver/buffer is required. For this reason, the system designer must be thoroughly familiar with the specific NMOS device to be used (the logic level and current requirements) and select the proper selection of a compatible interfacing McMOS device.

INTERFACING McMOS WITH BIPOLAR LSI

Yet another series of logic integrated circuits available to the system designer are the bipolar large scale integration (LSI) devices. These circuits consist of large gate arrays which are mask-programmable to provide specialized complex system functions. One technology used in these gate arrays is termed STRL and illustrated in Figure 2-26. This STRL gate basically consists of a Schottky transistor and four resistors. Interfacing between McMOS and

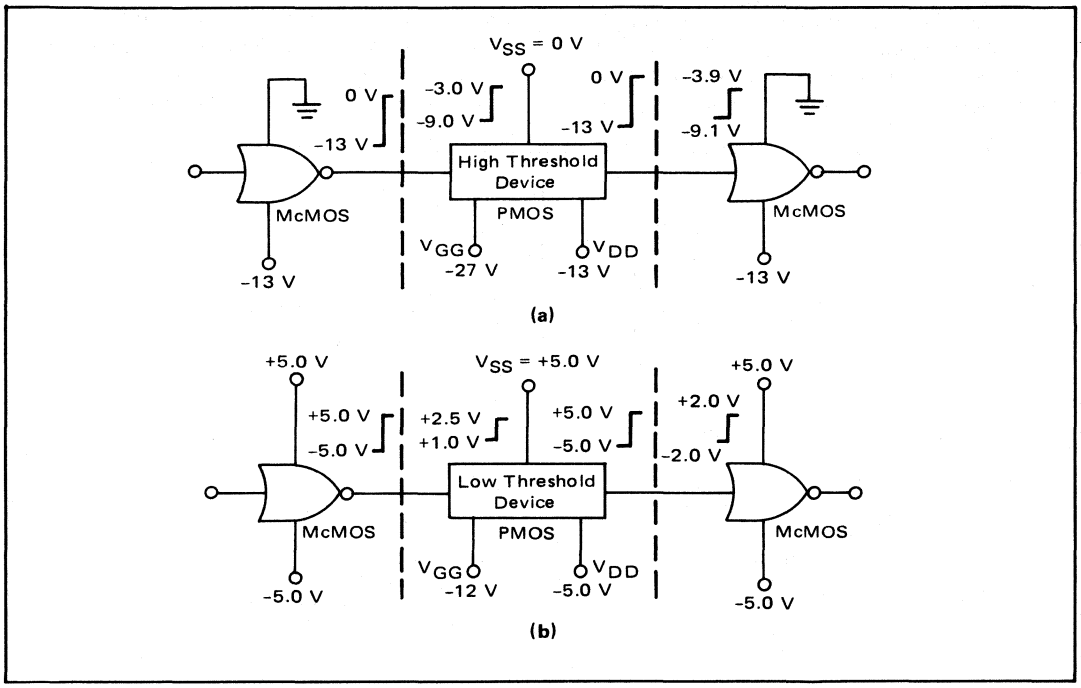


FIGURE 2-25 – McMOS – PMOS AND PMOS – McMOS INTERFACE SYSTEMS

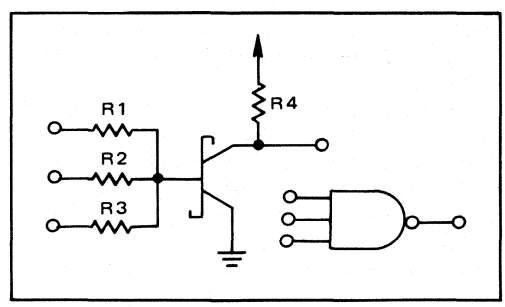


FIGURE 2-26 – A BASIC STRL GATE

STRL gate arrays is shown in Figure 2-27. As shown, the entire system operates with a +5.0 volt supply. While the STRL input levels are exactly like TTL, the STRL family exhibits a much lower sinking requirement I_{inl}. These characteristics make any McMOS device compatible in driving STRL logic with resulting noise margins at the high and low state of 2.5 and 0.5 volts, respectively. STRL also has a TTL fan-out of 1 with TTL-type output logic specifications. However, under worst case consideration with a resistor tolerance of +30% (R4 in Figure 2-26) and sourcing the total leakage of the Schottky transistor, the V_{OH} level will be approximately 4.2 volts rather than the specified 2.4 volts at an I_{OH} of 300 μA. The worst case noise margins for the STRL to McMOS interface are therefore 0.7 and 1.0 volts, high and low state, respectively.

However, there are specified current limitations which are 10 milliamperes into or out of any package pin on standard McMOS devices or as high as ±45 milliamperes per output on certain buffer/driver configurations. Data sheets must be consulted so as not to exceed the device current or dissipation limits.

Figure 2-28 shows an example of a standard McMOS device driving an NPN transistor. The value of the base resistor R_B is dependent upon the value of the McMOS V_{DD} operating voltage. If the supply V_{DD} is 5 volts, the R_B resistor is not required since the source current limit is typically 2.0 milliamperes. This figure is determined from the saturated area of the P-channel drain characteristics. A V_{DD} voltage of 10 volts is marginal for operation when R_B = 0 ohms, since the saturated P-channel current in this case (approximately 9 milliamperes), is very close to the allowed 10 mA device limit. Therefore, in this application a value of 500 ohms is recommended for resistor R_B. At 15 volts, it is necessary to use a value of approximately 1 k ohm for resistor R_B to limit the current to 10 mA, since the typical saturated current level in this case is approximately 18 mA. The same reasoning applies to applications where driving PNP transistors; the McMOS device N- and P-channel

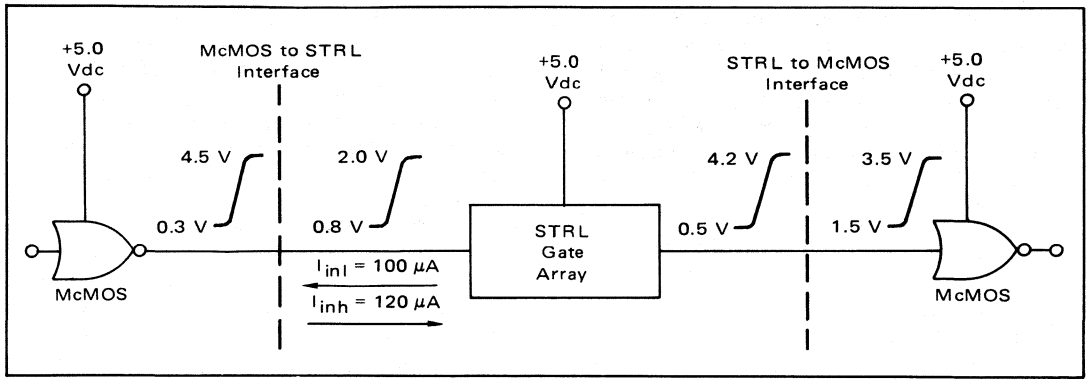


FIGURE 2-27 – McMOS – STRL LSI SYSTEMS INTERFACE

STRL gate arrays are also available with open collector outputs. When using these devices it is necessary to use an external pull-up resistor and a suitable value would be approximately 3 to 4 k ohms. Another of the LSI gate arrays uses low power Schottky TTL logic cells. The input and output characteristics of these cells are similar to standard low power TTL and can also be interfaced with McMOS logic in the same manner as LTTL.

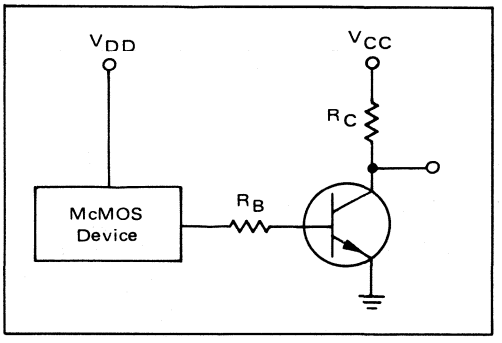


FIGURE 2-28 – McMOS TO DISCRETE INTERFACE

INTERFACING McMOS WITH OTHER SEMICONDUCTOR DEVICES

One misconception that many circuit designers have with McMOS is that this technology cannot source or sink any appreciable or usable amount of current when interfacing with other than McMOS devices. This is not always true, as this chapter previously described in the section entitled Output Loading Considerations. The sinking and sourcing capability of a McMOS device, as found on data sheets, are measured at specific output voltages and illustrate fixed points in the non-saturated region of the McMOS output drain characteristic curves. In fact, McMOS devices can drive high current loads if large drain to source voltages (V_{DS}) are allowed across the N- or P-channel devices.

drain characteristic curves should be consulted to select the proper values of current limiting resistors. Obviously, the choice of pull-up resistor R_C and the transistor are based upon the required drive current level and the h_{FE} versus I_C characteristics of the selected transistor.

The technique used in Figure 2-28 can also be used as a driver interface from McMOS to several TTL or LTTL gates or devices. The fan-out of such a circuit is dependent upon the current gain of the transistor and the properly selected pull-up resistor R_C.

One specific application of a McMOS device gate driving a high current load is shown in Figure 2-29. In this application, a load current of 4 amperes is required. The selected interface, a 2N6055 power Darlington, requires a base current of 16 milliamperes for a V_{CE} saturation of 2 volts; to supply this current, the McMOS MC14049 hex-inverter, buffer/driver is used. From the P-channel drain characteristics curve, the saturated source current is found to be approximately 32 milli-amperes for a V_{DD} of 10 volts. In driving the Darlington with a 20 mA, the McMOS characteristics exhibited a drain to source voltage of −4.0 volts. Therefore, the base resistor R_B can be calculated by the equation:

$$R_B = \frac{V_{DD} - V_{DS} - V_{BE(sat)} - V_{diode}}{I_B}$$

or approximately 100 ohms.

The addition of the diode and 1 k ohm bias resistor in the Darlington emitter circuit ensure a slight reverse bias on the Darlington when the McMOS driver is in the low state and thus prevents thermal runaway. For pulsed operation, the MR751 six ampere diode is used; for continuous operation, it is recommended that a stud mounted MR1120 be used for power dissipation reasons.

One advantage of using a McMOS device to drive a circuit as shown in Figure 2-29 is that the driver circuit dissipates very little power when in the idle or OFF state. The push-pull type output of McMOS dissipates power only when driving the load device unlike a TTL open collector driver which must shunt all the drive current when the load device is OFF.

By using techniques similar to Figure 2-29, McMOS can be used to directly drive LEDs, opto-couplers or other discrete devices. Examples of interfacing to high power drivers, such as SCRs and triacs, are described in Motorola application note AN-712 entitled "Interface Techniques Between Industrial Logic and Power Devices".

INTERFACING SUMMARY

With a wide range of power supply operating voltages and simplified input/output characteristics, McMOS logic elements may be successfully interfaced with any other logic·device technology available today. Table 2-2 shows the noise margins, logic levels and fan-out for various logic family interfaces.

McMOS elements can also be used as current drivers for interfacing with a variety of discrete semiconductor devices. The sourcing and sinking capability for driving discretes may be extrapolated from the McMOS device output drain characteristic's curves. By using these curves and observing the device maximum current and dissipation limits, a reliable McMOS to discrete power interface may be achieved.

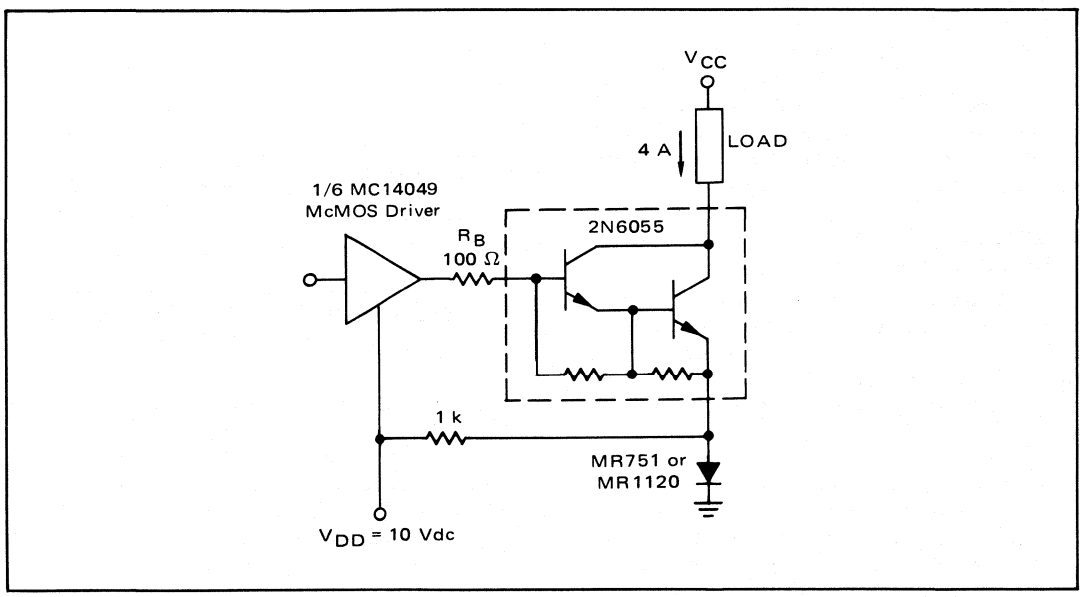


FIGURE 2-29 – McMOS TO BIPOLAR 4 AMPERE DRIVER

TABLE 2-2 – McMOS GENERAL INTERFACE PARAMETERS

INTERFACE	INTERFACE† NOISE MARGIN		INTERFACE‡ LOGIC LEVELS		INTERFACE MAXIMUM FAN-OUT	REMARKS
	"1"	"0"	"1"	"0"		
McMOS-McMOS	1.5 V	1.5 V	3.5 V	1.5 V	>50	5-volt system.
	3.0 V	3.0 V	7.0 V	3.0 V	>50	10-volt system.
	4.5 V	4.5 V	10.5 V	4.5 V	>50	15-volt system.
McMOS-MHTL	5.0 V	5.0 V	8.5 V	6.5 V	1	
MHTL-McMOS	3.0 V	3.0 V	10.5 V	4.5 V	>50	Active pull-up MHTL
	4.0 V	4.0 V			>50	Passive pull-up MHTL with 2 k to 5 k ohm pull-up resistor
McMOS-LTTL	2.5 V	0.4 V	2.0 V	0.7 V	1	Two-input McMOS NOR gates driven in parallel will drive two LTTL loads; Four-input McMOS NOR gates driven in parallel will drive four LTTL loads.
LTTL-McMOS	1.1 V	1.2 V	3.5 V	1.5 V	See Remarks	3-k ohm pull-up resistor. Fan-out determined by dynamic requirements.
McMOS-TTL/DTL	2.5 V	0.4 V	2.0 V	0.8 V	2	Buffers only.
TTL/DTL-McMOS	1.1 V	1.1 V	3.5 V	1.5 V	See Remarks	2-k pull-up resistor for TTL or open-collector DTL. Fan-out determined by dynamic requirements.
McMOS-MOS	3.0 V	4.0 V	-3.0 V	-9.0 V	>50	High Threshold PMOS (V_{SS}-V_{DD}) = 13 V
	2.5 V	6.0 V	2.5 V	+1.0 V	>50	Low Threshold PMOS (V_{SS}-V_{DD}) = 10 V
MOS-McMOS	3.9 V	3.9 V	3.5 V	1.5 V	>50	High Threshold (V_{SS}-V_{DD}) = 13 V
	3.0 V	3.0 V	2.0 V	-2.0 V	>50	Low Threshold (V_{SS}-V_{DD}) = 10 V
McMOS-MECL	0.225 V	4.325 V	-1.105 V	-1.425 V	2	V_{DD} = Ground V_{SS} = -5.2 V
MECL-McMOS	0.66 V*	1.56 V*	-1.56 V	-3.64 V	>50	V_{DD} = Ground V_{SS} = -5.2 V *Typical
McMOS-STRL	2.5 V	0.5 V	2.0 V	0.8 V	2	
STRL-McMOS	0.7 V	1.0 V	3.5 V	1.5 V	See Remarks	Fan-out determined by dynamic requirements.

†Interface Noise Margin
– For "1" column-difference between output high level of one device and input high level of next,
– For "0" column-difference between output low level of one device and input low level of next.

‡Interface Logic Level: worst case threshold level going from one device to the input of another.

OPERATING SPEED

The operating speed of a logic system is based upon signal propagation delays and the output rise and fall times. In the CMOS logic family these parameters vary as a function of the output load capacitance, the operating voltage, and the device temperature.

CAPACITIVE LOAD EFFECTS

The McMOS family is designed to have equal propagation delays from the low-to-high and high-to-low states (t_{PLH}, t_{PHL}, respectively). In addition, the McMOS devices also have equal rise and fall times (t_r, t_f) with a 15 pF load. These four parameters all vary as a function of the load capacitance and in most data sheets are characterized by a form of the formula:

$$t = K_0 C_L + K_1.$$

The formula constants are different for t_r, t_f and the propagation delay $t_{PLH} = t_{PHL}$. Both K_0 and K_1 are device dependent and functions of logic complexity, internal capacitance, carrier mobility, etc. The important coefficient in determining dynamic performance for a given capacitive load is K_0 and is given in nanoseconds per picofarad.

Special consideration must be given to capacitive loading effects, especially to t_r and t_f when driving edge-triggered devices, and also to the propagation delays when operating totally synchronous systems. (See the previously described section entitled Input Considerations). The effects of the load capacitance on the above mentioned ac parameters are shown in Figures 2-30 and 2-31.

VOLTAGE EFFECTS

The constants, K_0 and K_1, in the formula above are given in the data sheets for power supply voltages of 5, 10 and 15 volts. The relationships of the delay and transition times with operating voltage are also shown in the typical family characteristics in Figures 2-30 and 2-31. In general, the delay and transition times decrease approximately as the inverse of the operating voltage. Similarly, the maximum operating frequency increases proportionally to the supply voltage.

TEMPERATURE VARIATIONS

As the temperature of a McMOS chip increases, the mobility of the N- and P-channel devices decrease; as a result, longer times to charge or discharge the external load capacitance are required. A previous section entitled Thermal Considerations described and illustrated (Figure 2-12) a normalized plot of the change in delay and transition times as a function of ambient temperatures. To generalize this plot, the increase in delay or transition times is approximately +.25%/°C for temperatures increasing above 25°C.

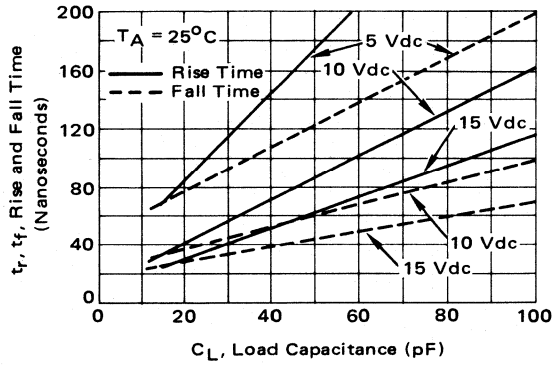


FIGURE 2-30 – TYPICAL RISE AND FALL TIME versus LOAD CAPACITANCE

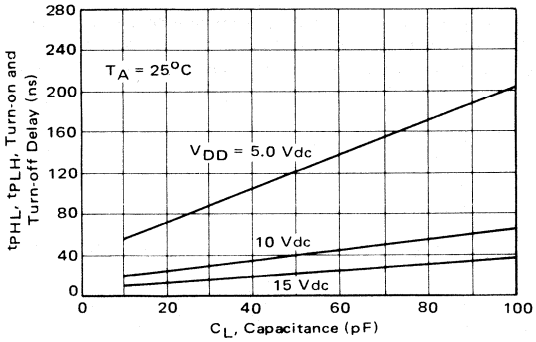


FIGURE 2-31 – TYPICAL PROPAGATION DELAY TIMES versus LOAD CAPACITANCE

THREE-STATE LOGIC AND ANALOG SWITCHING CONSIDERATIONS

In many system applications, the wire-ORing technique of the passive pull-up outputs has been used in bussing type applications. This technique greatly reduces system wiring and package count by the sharing of common input/output lines. When TTL logic was introduced, active pull-up devices were used in the output circuitry rather than the passive elements as in DTL logic. The active pull-up outputs prevented these devices from being used in wired-OR applications, and the only way to achieve the wired-OR was to use logic elements incorporating open collector type outputs with external pull-up resistors. To eliminate the problems of wire-ORing in TTL, the concept of three-state logic was introduced. This allowed the system designer to develop multiplexing schemes which select a single element to drive a common line while disabling all other drivers on that line. The concept also allowed more drivers to be attached to a common input/output bus line.

CMOS, like active pull-up TTL, cannot be wire-ORed since both the current sinking and sourcing devices in a CMOS output are MOS transistors. To illustrate, one may consider two CMOS gates with their outputs connected as shown in Figure 2-32. If the output of gate A is a logic "1" (P-channel transistor ON) and the output of gate B is a logic "0" (N-channel transistor ON), a current path exists from V_{DD} internally through gate A to the output, and also into the output of gate B, and finally to V_{SS}. If the impedances of the N- and P-channel transistors are comparable, the output level between gates A and B will be approximately 1/2 of $(V_{DD} - V_{SS})$.

If the power supply voltage is less than 10 volts, gates A and B will probably not be destroyed in this example. However, the power dissipation will increase and the output level will not be a usable logic state.

To eliminate the problems of wire-ORing, the three-state logic concept is provided in many CMOS logic functions because it can be very easily implemented, as will be described later.

WHAT IS THREE-STATE LOGIC?

The output of a standard logic element has two stable and defined states (a logic "1" or true state and a logic "0" or false state). Both of these states can be represented by a low impedance device coupled to one of the power supply rails. A three-state logic element simply provides an additional third output state. When in the third state (output disable or OFF), the output is effectively disconnected from the logic driving devices by a high impedance network at its output.

In the active logic "1" or "0" mode, three-state outputs have the same electrical equivalent as non three-state outputs. As shown in Figure 2-33(a), the output network for CMOS consists of capacitors connected to both power supplies. In parallel, diode structures serve to restrict logic levels to within the operating voltage supply range.

When switched to the three-state (high impedance) mode, as shown in Figure 2-33(b), the source-sink drive resistances increase to the 150-200 megohm range, effectively by an open circuit. For data sheet specifications, this open circuit resistance is defined by a three-state leakage current measured with respect to either voltage supply bus.

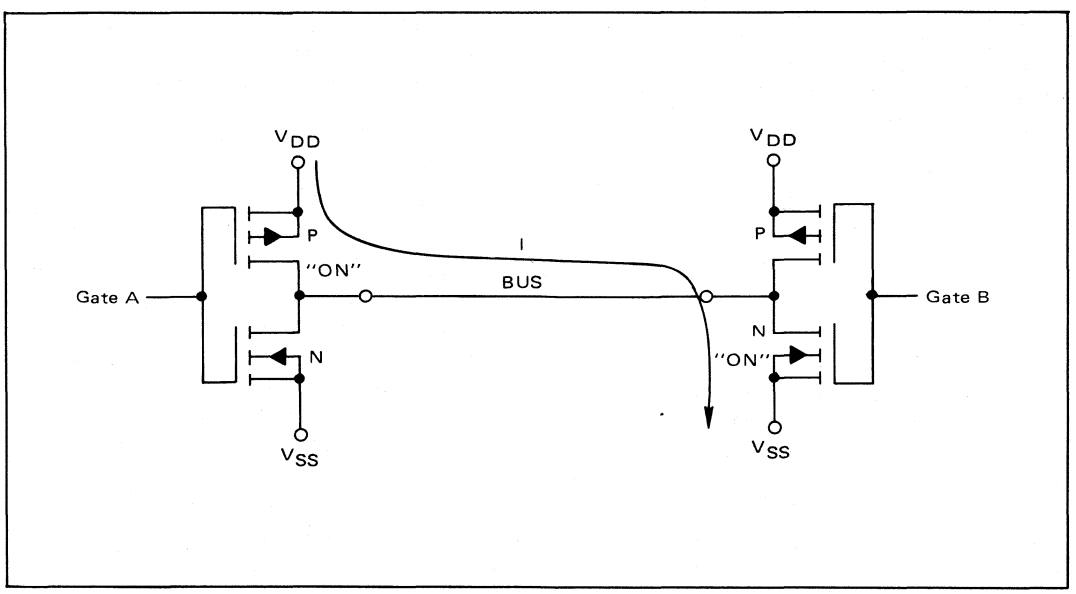


FIGURE 2-32 – CMOS GATES WITH OUTPUTS CONNECTED

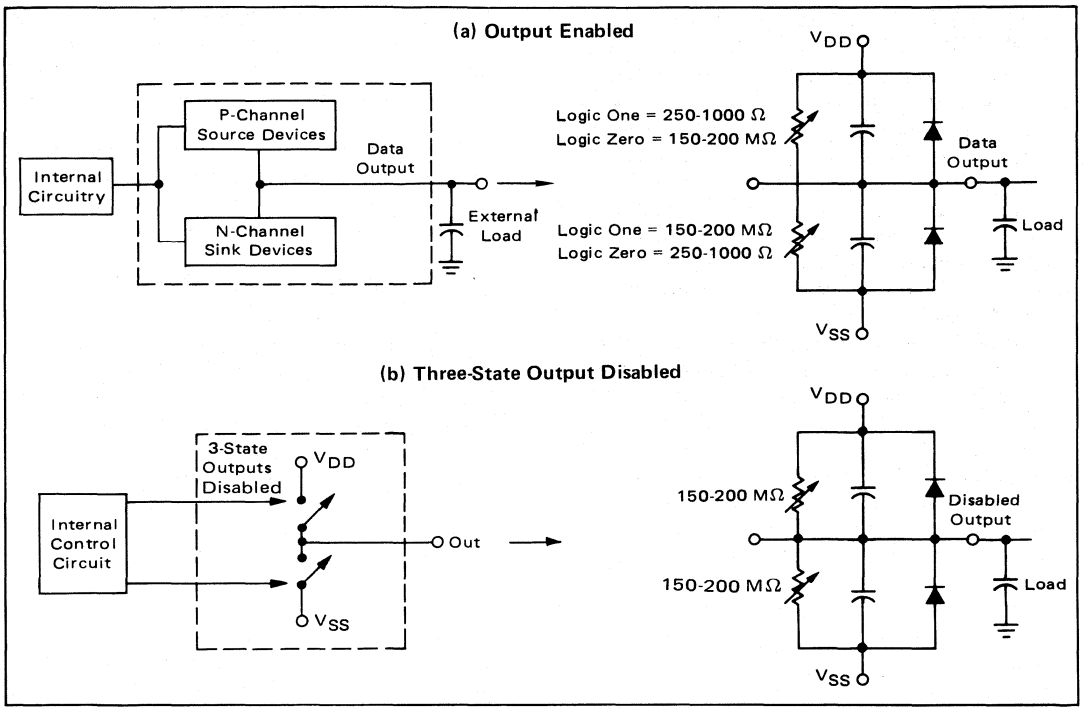


FIGURE 2-33 – CMOS OUTPUT EQUIVALENTS

THREE-STATE LOGIC IMPLEMENTATION

The prime objective in a three-state device design is to disconnect the output terminal from the active logic driving sources. There are two basic methods to achieve this objective: either a transmission gate or a disabling function may be implemented. The first method uses a transmission gate in series with the output signal line. The transmission gate is an important building block for the construction of CMOS integrated circuits; its characteristics which are easily provided in CMOS would be difficult to duplicate in any other IC technology available today. The circuit of the basic McMOS transmission gate is shown in Figure 2-34. When the transmission gate is enabled, a low resistance exists between the input and the output which allows current flow through the gate in either direction. The voltage on the input line must always be positive with respect to the substrate (V_{SS}) of the N-channel device, and negative with respect to the substrate (V_{DD}) of the P-channel device. The gate is enabled when the gate (G1) of the P-channel device is at V_{SS} and the gate (G2) of the N-channel device is at V_{DD}. When G2 is at V_{SS} and G1 is at V_{DD}, the transmission gate is disabled and a resistance greater than 10^9 ohms exists between input and output.

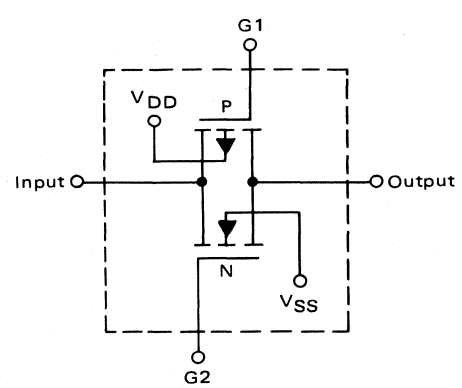


FIGURE 2-34 – BASIC McMOS TRANSMISSION GATE

The diagram of a three-state element using a transmission gate to provide the output disable is shown in Figure 2-35(a). Figure 2-35(b) shows the logic symbol and definition of a transmission gate. The second method of design of a three-state output disables or disconnects both the sourcing and sinking driving devices from the V_{DD} and V_{SS} power supply rails. The circuit for this method is shown in Figure 2-35(c). In this figure segment, the center P- and N-channel MOSFETs are connected as a standard CMOS inverter. In series with the inverter are an additional P-channel device to V_{DD} and an N-channel device to V_{SS}. By using a second inverter to provide the two phase signals from an input disable signal, both P- and N-channel series MOSFET devices can be simultaneously enabled or disabled. When the series devices are enabled (ON), the output functions as a normal CMOS inverter. When they are disabled (OFF), the three-state logic inverter is a "don't care" state since the output is disabled. The logic symbol and truth table of the described three-state circuit is shown in Figure 2-35(d).

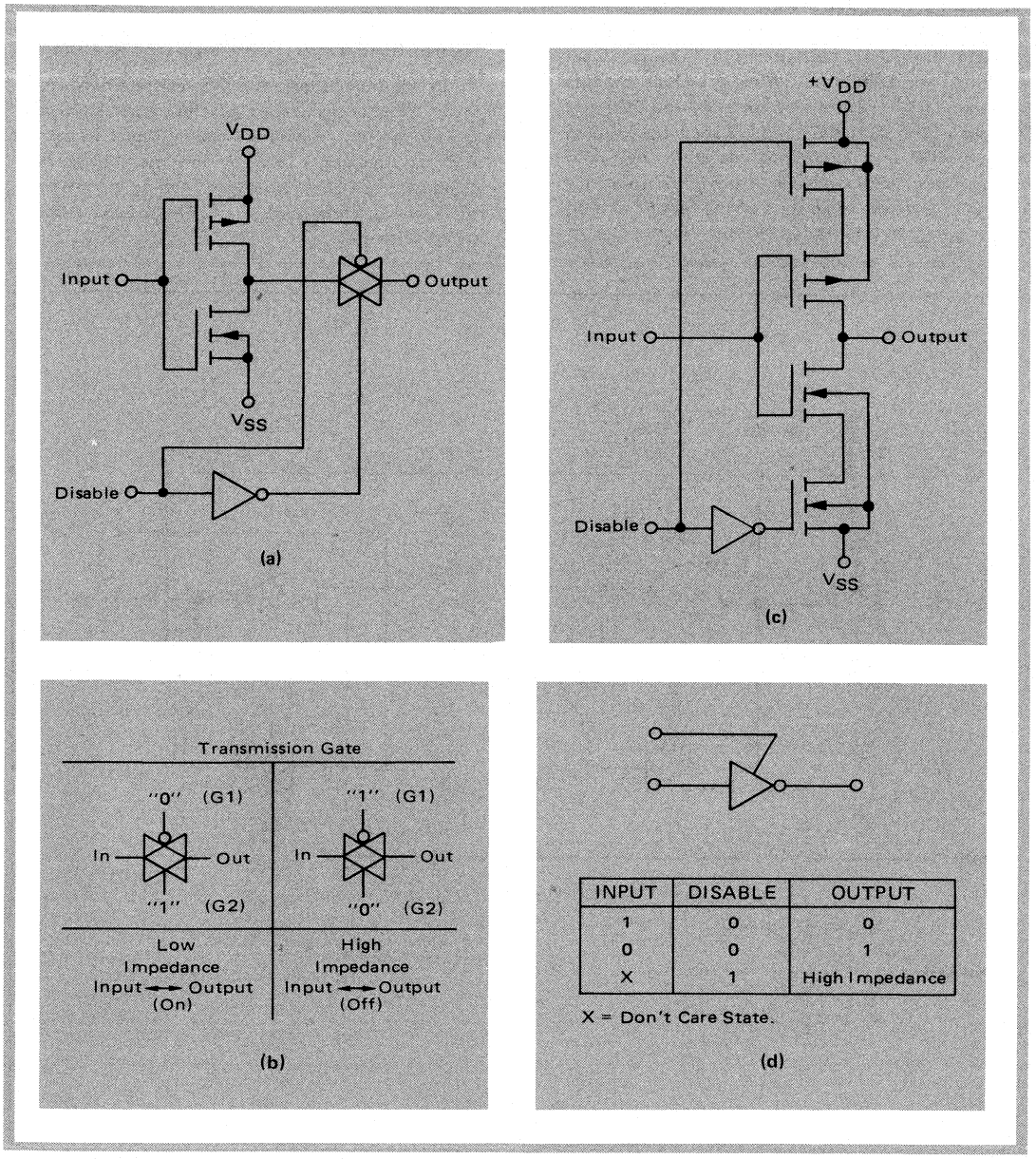


FIGURE 2-35 – BASIC THREE-STATE OUTPUTS

INTERNAL LOGIC TRANSMISSION GATES

The transmission gate is a valuable tool used for accomplishing many CMOS technology MSI and LSI designs. An illustration of using the basic transmission gate is provided in the McMOS MC14013, Type-D flip-flop as shown in Figure 2-36. The flip-flop works on the Master/Slave principle and consists of four transmission gates (TG). Four NOR gates, two inverters, and a clock buffer/inverter, comprise the configuration. When the clock is a logic "0", transmission gates TG2 and TG3 are OFF and 1 and 4 are ON. In this condition, the Master is logically disconnected from the Slave. With TG4 ON, gates G3 and G4 are cross-coupled and latched in a stable state. Assuming that the Set and Reset inputs are low, the logic states of gates G1 and G2 are determined by the logic signal applied to the Data input. When the clock changes to a logic "1", TG2 and TG3 turn ON and TG1 and TG4 turn OFF. Gates G1 and G2 are cross-coupled through TG2 and latch into the state they held at the time the clock changed from a "0" to a "1". With TG3 ON, the logic state of the Master section (output of gate G1) is fed through an inverter to the Q output and G3 through an inverter and finally to the $\overline{Q}$ output. When the clock returns to a "0", TG3 turns OFF, and TG4 turns ON. This disconnects the Slave from the Master and latches the Slave into the state existing in the Master when the clock changed from a "1" to a "0" Thus, data is entered into the Master on the positive edge of the clock pulse. When the clock is logical high, the output of the Master is transmitted directly through the Slave to Q and $\overline{Q}$. When the clock transfers to a logical low state, the Master logical state is stored by the Slave which then provides the outputs. Transmission gates and flip-flops are commonly used in system counter and shift register designs.

ANALOG APPLICATION CONSIDERATIONS

In addition to generating three-state outputs or internal digital signal steering, the transmission gate is very useful as a gate for analog signal switching and multiplexing. Two of the most important characteristics of an analog switching element are the ON resistance and the OFF leakage current specifications.

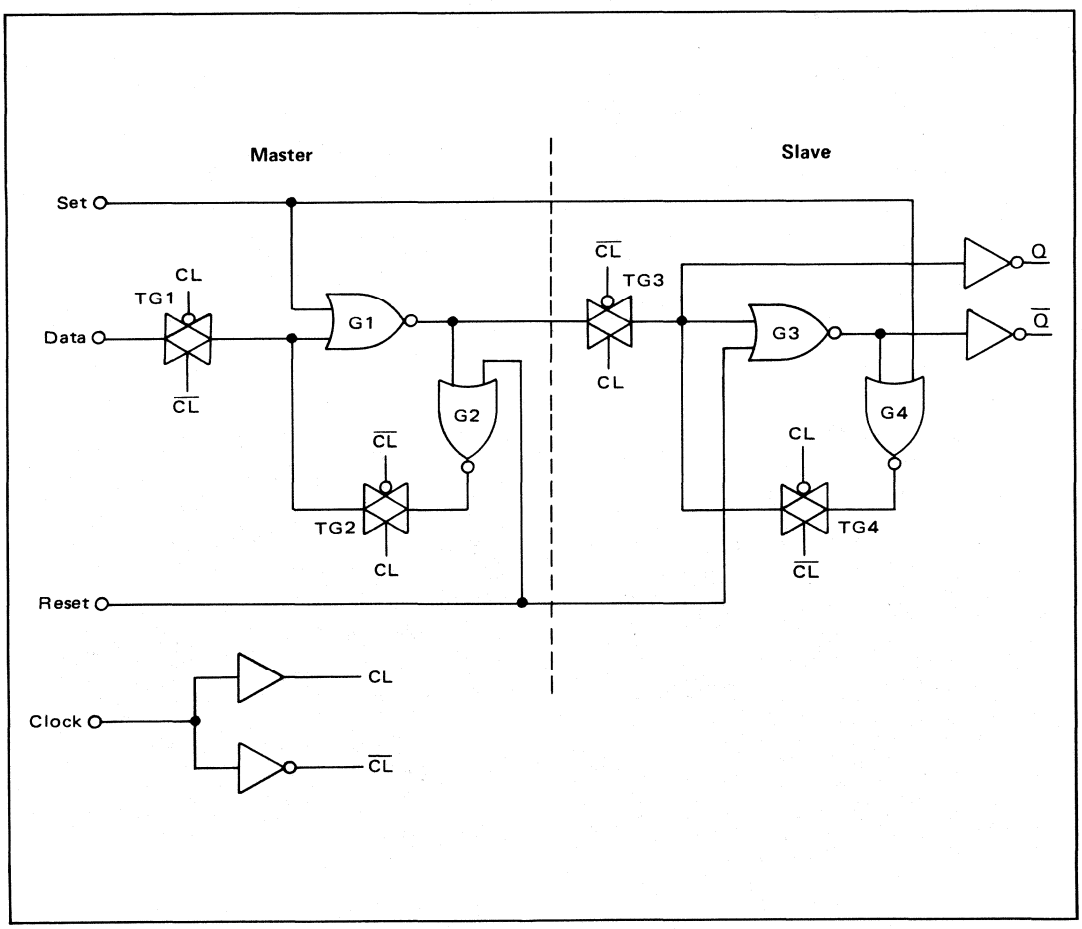


FIGURE 2-36 – McMOS TYPE D FLIP-FLOP

ON RESISTANCE

The resistance between the input and output of a basic transmission gate in the ON condition is dependent upon the voltage applied at the input, the potential difference between the two substrates ($V_{DD} - V_{SS}$), and the load on the output. R_{ON} is defined as the input-to-output resistance with a 10 k ohm load resistor connected from the output to ground. Figure 2-37 illustrates an interesting peaking effect which occurs in the R_{ON} versus V_{in} curves of the basic transmission gate in Figure 2-34. When V_{in} is at or near V_{DD}, the P-channel device provides the low resistance. The N-channel device is OFF since the potential difference between G2 and the drain or source of the N-channel device is less than the threshold voltage. When V_{in} is at or near V_{SS}, the N-channel device is conducting and the P-channel device is OFF. At voltages between the two extremes, both devices are partially ON and the value of R_{ON} is due to the parallel resistance of the P-channel and N-channel devices. The different slope of the curve on either side of the peak is due to the greater sensitivity of the N-channel resistance to the substrate degeneration (or substrate bias). Thus, the rate of increase in R_{ON} with respect to V_{in} is greater for input voltages between V_{SS} and the "peaking voltage" than for input voltages greater than the "peaking voltage".

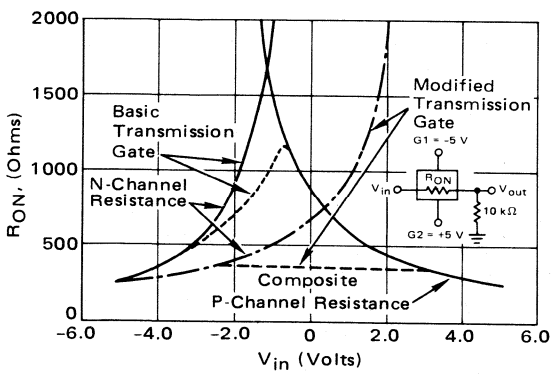


FIGURE 2-37 – McMOS TRANSMISSION GATES R_{ON} versus V_{in}

Figure 2-38 shows a modification to the basic McMOS transmission gate with the addition of a third device to control the substrate bias of the N-channel device. The effect of this third device is to delay the turn OFF of the N-channel device which results in a much flatter R_{ON} versus V_{in} curve, as shown in Figure 2-37. This concept is used in the MC14016 Quad Analog Switch. Even with the addition of devices to control the substate bias, R_{ON} will still vary as a function of the input signal amplitude. This variation will always be the greatest at the lower power supply ($V_{DD} - V_{SS}$) voltages and decrease as the power supply voltage is increased to the maximum value. With a 10 volt

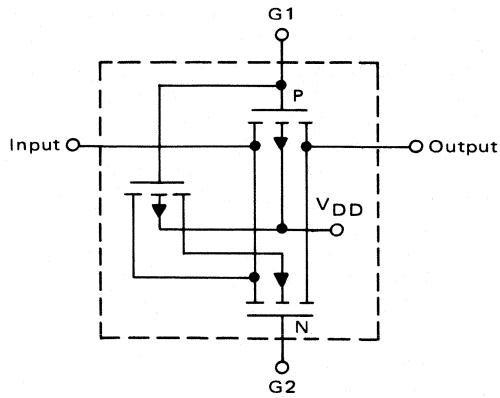


FIGURE 2-38 – MODIFIED McMOS TRANSMISSION GATE

supply, the change in R_{ON} will typically vary less than ±15% from the nominal resistance – over the specified range of input voltages ($V_{SS} < V_{in} < V_{DD}$). The change in R_{ON} between any two gates in an analog gate package will typically be less than 5% of the nominal value.

SIGNAL DISTORTION

The variation of the gate resistance versus input level causes analog signal distortion. Distortion may be minimized if the analog gate is operated from a split power supply. To illustrate, if V_{DD} = +5 volts and V_{SS} = –5 volts, the input analog signal will swing from $-V_{sig}$ to $+V_{sig}$, where V_{sig} is the peak amplitude of the analog signal with reference to ground. Note that the V_{sig} component must be restricted to the range of $V_{SS} < V_{sig} < V_{DD}$. If this condition is not held, destruction will occur because of the internal forward biasing of P-N junctions.

In the case of the MC14016 Quad Analog Switch, the signal distortion is measured using V_{DD} = +5, V_{SS} = –5, R_{load} = 10 k ohms and a V_{in} swing of ±5 volts (1.77 V_{RMS}) at 1 kHz. The specified total harmonic distortion is typically less than 0.16%. Obviously, the distortion will increase as the power supply voltage is lowered. Distortion will also increase as the load resistance is decreased from 10 k ohms because of the voltage division relationship. The equation, $\frac{R_L}{R_L + R_{ON} + \Delta R_{ON}}$, illustrates this relationship.

Insertion loss is also a measure of the magnitude of the R_{ON} value. This parameter is measured using an input frequency of 1 MHz and various loads R_L. The insertion loss in dB = 20 $\log_{10}$ (V_{out} / V_{in}). At low values of R_L (i.e., <10 k ohms), $V_{out} \cong \frac{R_L V_{in}}{R_L + R_{ON}}$. This equation is valid only for low load impedances and relatively low signal frequencies. With a frequency of 1 MHz or higher and load impedances greater than 100 k

ohms, the insertion loss begins to be dominated by the output capacitance parallel to the load.

INPUT/OUTPUT LEAKAGE

In the OFF state, the transmission gate has a very high resistance (in the order of 10^9 ohms) and is specified in McMOS device data sheets by an input/output leakage current value. This parameter is measured by using a positive and negative power supply (V_{DD} and V_{SS}, respectively), disabling the transmission gate, applying a signal input forced to V_{DD} or V_{SS} (two measurements), and the output leakage current being measured with respect to ground. This is the reason for the plus and minus specification on the data sheets. The leakage currents at 25° C will be typically in the order of nanoamperes with several orders of magnitude difference between the typical and maximum values. The leakage currents components and the variation over temperature is the same as that previously discussed in the section entitled Thermal Considerations.

DEVICE CAPACITANCE

A simplified ac model of a transmission gate including the gate ON/OFF impedances and associated capacitances are shown in Figure 2-39. The definitions of the circuit elements are:

- $C_{CS_{1,2}}$ – control to switch capacitance
- C_{in} – control input capacitance
- C_{IOS} – switch feedthrough capacitance
- C_{IS} – switch input capacitance
- C_{OS} – switch output capacitance
- $C_{SS_{1,2}}$ – switch to switch capacitance
- R_L – leakage impedance
- R_{OFF} – gate OFF resistance
- R_{ON} – gate ON resistance

coupling capacitance (control-to-switch) C_{CS}. This test is performed by loading the input and output of the analog switch and driving the control line with a signal having a specific rise/fall time and pulse width. The "noise" pulse amplitude coupled from the control logic to the switch is measured and specified in millivolts.

The effect of the coupling capacitance C_{SS} between switches is characterized by the crosstalk specification between any two switches within a single package. This crosstalk is measured by loading both analog switches with one statically turned ON and the other OFF. The ON switch is driven with a 1 MHz sine wave and the output of the OFF switch is measured in dB with reference to the drive. A typical value for the MC14016 Quad Analog Switch is –80 dB and represents a coupling capacitance of less than 0.02 picofarads.

The feedthrough capacitance C_{IOS} is the capacitance (input-to-output) of the analog switch parallel to the ON/OFF resistances. The effect of this capacitance is signal feedthrough from input-to-output when the switch is OFF. One method of measuring this effect is to drive an OFF switch with a sine wave oscillator and increase the frequency until the feedthrough reaches a predetermined value (such as –50 dB) and record the driving frequency.

The capacitance C_{IOS} is typically 0.2 pF, and with a load impedance of 1 k ohms, the frequency for the –50 dB level will be greater than 1 MHz. This –50 dB frequency will decrease as the load impedance is increased because of the following mathematical relationship.

$$-50\ dB = 20\log_{10}(V_{out} \div V_{in}),$$

$$\text{where } V_{out} = V_{in} \cdot \frac{Z_L}{Z_L + Z_F},$$

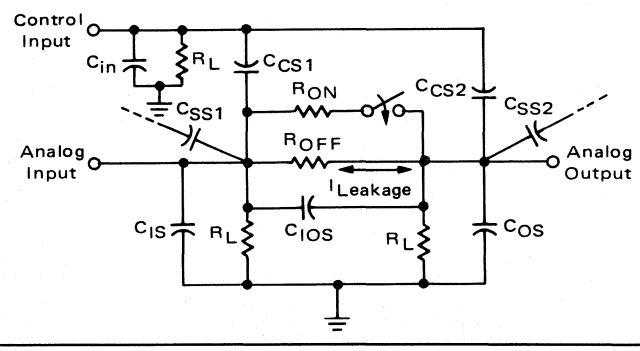


FIGURE 2-39 – AC MODEL OF SIMPLE TRANSMISSION GATE

Of all the internal capacitances of an analog switch, only four are specifically given in the data sheet: both inputs, the output, and the switch feedthrough capacitances. However, the elements not listed specifically are either the causes or effects for other electrical parameters contained in the data sheet.

The control-to-output crosstalk, measured in millivolts, is a measure of the amount of internal

and Z_L = load impedance,

and Z_F = feedthrough impedance.

With a load of one megohm, the frequency for the –50 dB level will be only a few kilohertz.

The output capacitance C_{OS} is the limiting factor of an analog switch bandwidth. The bandwidth is the frequency at which the output signal is 3 dB below the output level at the midband

frequency and is measured with a sine wave input and various loads. The 3 dB point is the frequency at which the output capacitance is determined from the following equation:

$$X_C = \frac{.707}{1-.707} \frac{R_{ON}R_L}{R_{ON} + R_L}.$$

The output capacitance is typically 5 pF and with a 1 k ohm load, the bandwidth is greater than 50 MHz. As the load R_L increases in impedance the bandwidth decreases. With loads greater than 100 k ohms, the value of $\frac{R_L}{R_{ON} + R_L}$ approaches 1 in the relationship of X_C to R_{ON}.

The switch input capacitance C_{IS} is typically 5 pF as was the output capacitance C_{OS}. The analog switches are bidirectional and their characteristics in both the input or output ports are identical. If the switch is driven from a low impedance source, the input capacitance may be neglected. However, with a high impedance source or with the cascading or treeing of switches in multiplexing, the capacitance must be considered since the signal frequencies may be attenuated and/or shifted in phase.

As analog switch outputs are paralleled to form multiplexers, the output capacitance increases proportionally to the number of outputs that are common. When systems require a large number of high frequency signal lines to be multiplexed, it is recommended that multiplexing be accomplished in several levels (tree fashion) with a smaller number of switches on each branch. This method will somewhat increase the complexity of the digital control logic and add to the signal delay; however, the system design goals will be more easily achieved.

SWITCHING SPEED

Besides the signal speed which was previously discussed with switch bandwidth, the switching speed must also be considered. The control input frequency is limited by the time required to turn the switch ON and OFF. The time required for the switch to change states will be typically less than 25 nanoseconds and will turn OFF faster than it turns ON. In relay terminology, a "break-before-make" action is necessary to prevent faults in multiplexing applications where several outputs are connected together.

In MSI or LSI parts designed for multiplexing, the delay from the control to the switch changing states will be longer than that previously mentioned. This delay time will be a function of the complexity of the required internal BCD or Binary decoding logic and must be considered when selecting a component to perform high frequency multiplexing. Obviously, as with CMOS speed in general, the maximum switching speeds are obtained at the highest $V_{DD} - V_{SS}$ power supply voltages.

DIGITAL APPLICATION CONSIDERATIONS

As previously described, there are several methods used to generate three-state outputs; however, regardless of the method, the same considerations in digital bussing apply. The major areas of concern to the designer are the number of devices that can be bussed and the frequency limitations.

DRIVING REQUIREMENTS

Calculations for a McMOS bus system generally focus on external bus current requirements since the dc fan-out due to device leakage current limitations is in the order of several hundred devices. Specifically, the number of devices (N) which may be connected to a bus line is calculated from the following equation:

$$N = \frac{I_{OD} - I_L}{I_L} + 1.$$

In the equation, the component I_{OD} is the active logic "1" or "0" output level of drive current available to supply the I_{TL} output leakage current of disabled or three-state devices connected to the line. The component I_L is the external load current required to drive the bus line. Component N must be calculated for both the high and low bus line logic states.

In a total CMOS system, dc fan-out considerations will allow approximately 94 devices (N) to be connected to the bus with a 5 V power supply and the worse case parameters of T = 125°C, I_{OD} min = −0.28 mA, I_L = 100 nA and I_{TL} = 3.0 μA. With such large values, fan-out is normally determined from switching performance requirements such as load capacitance and the required operating speed.

OUTPUT AND LOAD CAPACITANCE

When a three-state logic element is disabled, the output is a very high impedance and has an associated capacitance characteristic. This capacitance can be measured with a suitable bridge, or by observing a time constant on an oscilloscope when the output is disabled and a known value external load resistor is used. Care must be exercised when measuring the output capacitance, and all test fixture and instrumentation capacitances must not be overlooked.

The three-state output capacitance will typically fall in the range of 10 to 15 picofarads. This capacitance acts as a load to the bus line driving device and has a definite effect on the rise, fall and propagation times of the driver. Therefore, the three-state output capacitance must be considered in determining the number of devices which can be bused for a given data frequency.

BUS LINE RISE AND FALL TIMES

As was previously described in the section entitled Operating Speed, the rise and fall time is equal to: $t = K_0C_L + K_1$, where K_0 and K_1 are constants

dependent upon the McMOS device. All the capacitances of the three-state outputs (10 to 15 pF each), all inputs (5 pF each), and the bus wiring must be summed together to determine the rise and fall times of a bus-oriented system. For standard devices, at a supply voltage of 10 volts, the effect of the loading capacitance is typically 1.0 to 2.5 nanoseconds per picofarad increase in rise time and 0.5 to 1.5 nanoseconds per picofarad increase in fall time. In applications having a high bus capacitance, three-state bus drivers such as the MC14502 should be used. When using high bus capacitance drivers, the time increase is typically 0.6 nanoseconds per picofarad in rise time and 0.2 nanoseconds per picofarad in fall time. Propagation delays also increase as a function of the load capacitance C_L. This rate of increase is approximately half the rate increase in the rise and fall times.

MULTIPLEXING SPEED

The factors that limit the multiplexing speed of a bus system are the times required to switch a device into and out of the three-state "high impedance" mode. These propagation delay times are referred to as $t_{"0"H}$, $t_{H"0"}$, $t_{"1"H}$ and $t_{H"1"}$. For the definition and test procedure used for determining these parameters refer to Chapter 5 entitled Family Data in this book.

The capacitive load effect on the delay times follows the same relationship ($t = K_0C_L + K_1$) previously described regarding rise and fall times. The results of all the delays caused by bus line capacitance are shown in the timing diagram of Figure 2-40. In a three-state bus system, the data strobe of the receiver logic must be delayed a minimum time from the enable signal (which was applied to one of the bus drivers) to assure the accuracy of the data being received. This delay time is the summation of the maximum three-state delay time ($t_{H"1"}$ or $t_{H"0"}$), the maximum rise/fall time (t_r or t_f), the propagation delay of the bus lines, and the minimum setup time of the receiver logic.

A worst case three-state enable control pulse width would be the summation of the previously described minimum strobe delay, the minimum strobe pulse width, and the maximum receiver logic data hold time. The enable pulse width can actually be decreased from the worst case value because, as shown by the cross-hatched area of Figure 2-40, valid data is still present on the bus for the minimum delay time required of both the three-state output to go to the high impedance states and conversely from a high impedance state to a logic state.

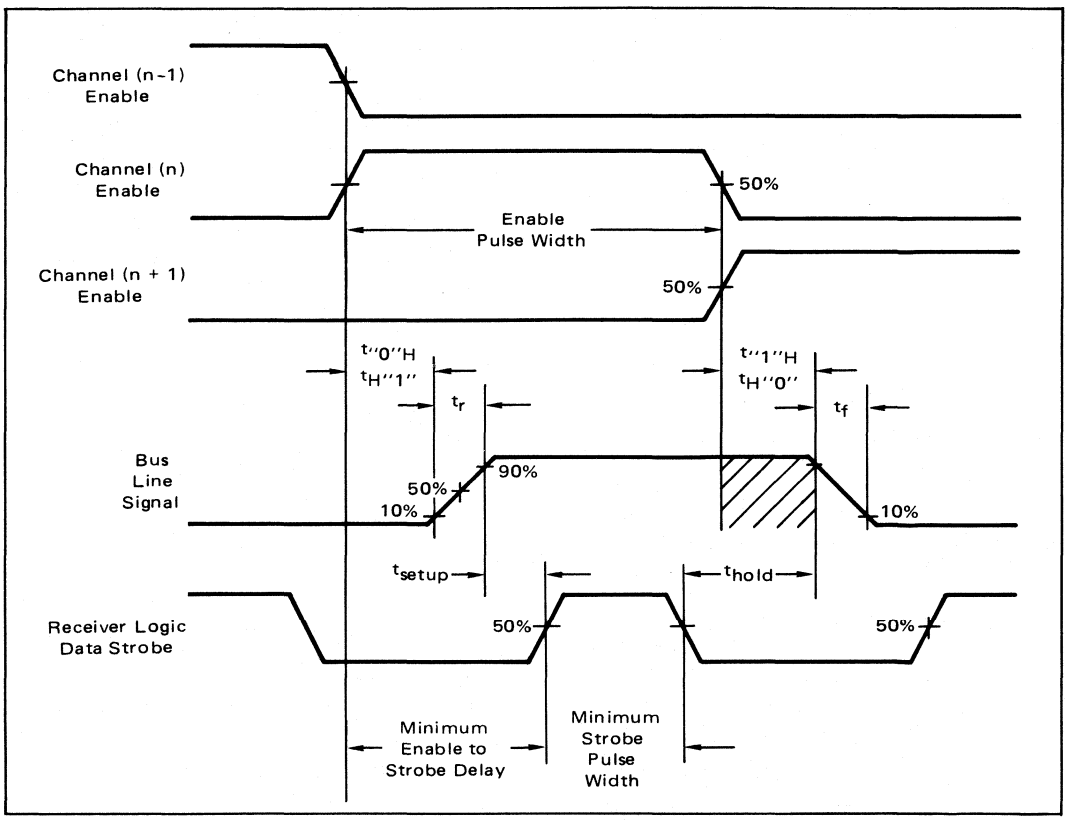


FIGURE 2-40 – THREE-STATE BUS TIMING DIAGRAM

BUS LINE PULL-UP/PULL-DOWN

The example used in the previous section illustrated that when the driver n was disabled, driver n + 1 was enabled to drive the bus line. Not all of the numerous three-state logic applications have a driver attached to the bus line at all times; these applications require special consideration.

If a bus system (at some period of time) has all drivers disabled, all outputs will be high impedance and the bus will be capacitive. The McMOS inputs of the bus receiver logic are also capacitive and will require very little drive current. In the totally disabled mode, high impedance bus lines make the receiver inputs very susceptable to both noise and oscillation, similar to open McMOS inputs. This situation can cause higher than normal receiver power dissipation and possible input destruction.

An obvious solution is to use pull-up/pull-down resistors on the bus lines. These resistors will have an associated rise time or fall time constant in relation to the total bus capacitance. This rise or fall time could present a problem; however, the use of resistors also limits the drive capability of the drivers when they are enabled.

An ideal solution is shown in Figure 2-41. In this application, the MC14016 Quad Analog Switch is used to dynamically pull-up or pull-down (depending on desired logic state) the bus lines when all of the driving devices are disabled. The low ON resistance of the analog switch produces faster rise (and fall) times than the resistor technique since the resistor minimum value is limited by the driver capability. When any one of the drivers is enabled, the analog switch is disabled, thus minimizing the power dissipation consistently present with passive pull-up or pull-down elements.

POWER DISSIPATION

Power dissipation in three-state bus systems is a function of the load capacitance, input transition times, frequency, and power supply voltage, similar to the relationship found with any standard CMOS device. Refer to the section entitled Power Supply Considerations for power dissipation information.

Shorted bus lines may sometimes occur in a system. With the exception of CMOS drivers, standard device outputs (when operating at 5 volts) will not cause serious device damage. At higher voltages, excessive currents (design limits are 10 mA per output pin) will be realized if the outputs are shorted to V_{DD} or V_{SS}. For this important reason, the system designer must exercise care when using bus systems with lines vulnerable to shorts. Such systems should be carefully staged prior to the initial power-up. One method would be to use a variable power supply and apply power slowly during the staging phase.

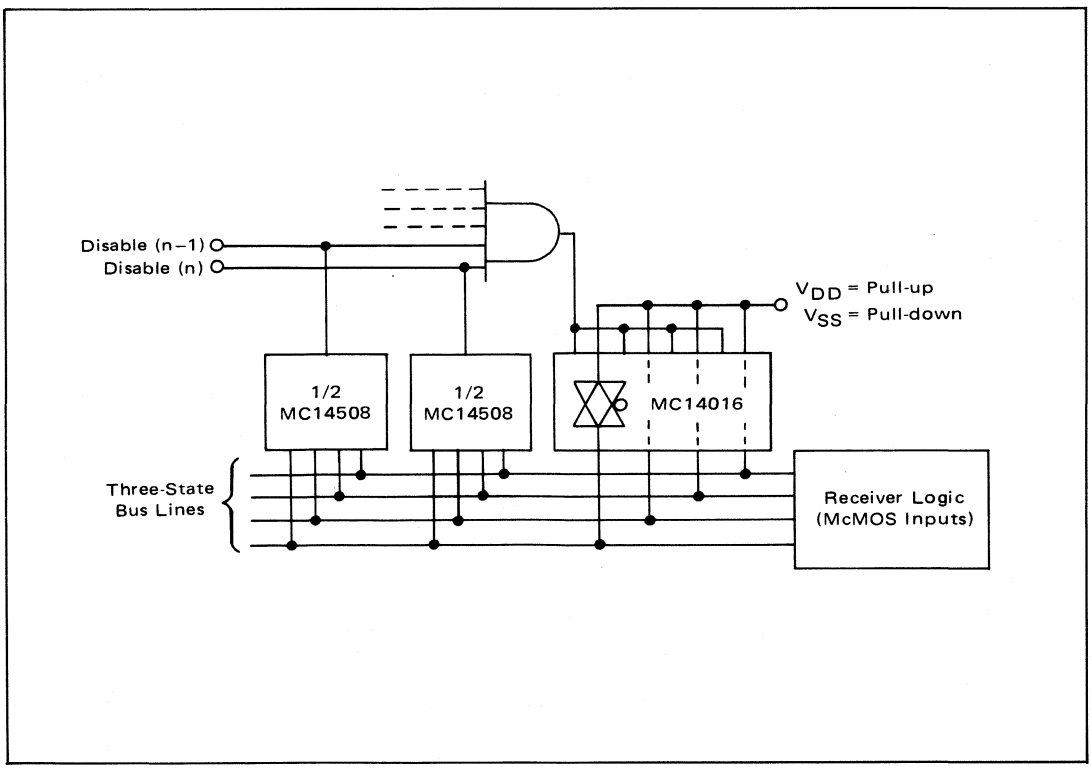


FIGURE 2-41 – THREE-STATE BUSING USING ACTIVE PULL-UP/PULL-DOWN

NOTES

McMOS

INTEGRATED CIRCUITS

Chapter 3

APPLICATION NOTES AND REFERENCE LITERATURE

The Motorola Semiconductor Products Division Applications Engineering Department is staffed with circuit and systems design engineers who have extensive experience and professional accomplishments in almost every field of electronics design engineering. The department goals are to provide customer assistance, to develop state-of-the-art design ideas, and to acquaint the circuits and systems engineer with the broad line of Motorola semiconductor products and their usage in the form of published applications notes and literature.

Many of the design ideas or concepts found in the more than two hundred available application notes can be implemented with the Motorola McMOS logic family. This chapter contains a complete listing of the currently available application notes that feature theoretical and practical descriptions of McMOS device usage. Included also is a listing of articles containing design information using CMOS logic devices.

For reference purposes, all the available Motorola application notes and their abstracts are tabulated in the Application Information section of the Motorola Semiconductor Data Library Reference Volume. A copy of the Application Note Catalog may also be obtained by sending your request on your company letterhead to the following address:

Technical Information Center
Motorola Semiconductor Products Inc.
P. O. Box 20912
Phoenix, Arizona 85036

ABSTRACTS OF AVAILABLE MOTOROLA APPLICATION NOTES FEATURING McMOS DEVICES

AN-538A MOTOROLA COMPLEMENTARY MOS INTEGRATED CIRCUITS

This note discusses some of the properties of N- and P-channel MOSFET's and describes how they are used to construct complementary MOS integrated circuits. Some basic McMOS logic functions are then discussed and methods of cascading McMOS counters are given.

AN-574 CMOS: A NEW LOGIC TYPE FOR CONTROL SYSTEMS

Designing circuits that operate properly in high noise environments such as those commonly found in an industrial plant is often the bane of the control systems designer. CMOS circuits offer high noise immunity, plus the additional benefits of operation over a broad range of power supply levels and very low power dissipation. This article compares CMOS to other logic types and then describes how to interface it to them.

AN-591 USING McMOS IN SYSTEM DESIGNS – THOSE ALL-IMPORTANT DETAILS

While much of the available literature has focused on introducing the CMOS technology and describing its potential, this discussion proceeds one step further and explores how to use CMOS devices most efficiently. There are important interrelationships behind the device features and performance specs, the parameter sensitivities and the operating subtleties, which are sometimes ignored. The correct approach to CMOS design, wherein such interrelationships are taken into account, can do a great deal to optimize a system design.

AN-703 DESIGNING DIGITALLY-CONTROLLED POWER SUPPLIES

This application note shows two design approaches: a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in any application.

AN-707 NOISE IMMUNITY COMPARISON OF CMOS VERSUS POPULAR BIPOLAR LOGIC FAMILIES

This application note compares the noise immunities of the four major logic families used today in industrial logic systems designs: TTL, DTL, HTL, and CMOS. Also included are general discussions of common noise sources, precautions against noise, noise specification, and standard noise tests.

AN-712 INTERFACE TECHNIQUES BETWEEN INDUSTRIAL LOGIC AND POWER DEVICES

Worst case design approaches are used to illustrate the methods of interfacing McMOS and MHTL logic to various power level loads, both ac and dc. The interface devices vary from small signal transistors to power transistors and thyristors using direct coupling/level translation and optoelectronic coupling techniques.

AN-713 BINARY D/A CONVERTERS CAN PROVIDE BCD-CODED CONVERSION

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2½ digit digital voltmeter.

AN-714 A PERSONALIZED HEART-RATE MONITOR WITH DIGITAL READOUT

Using the micropower operational amplifier MC1776 and CMOS digital intergrated circuits, entirely self-contained portable electro-medical monitoring equipment can be built. This note details the construction of a heart-rate monitor giving a digital indication, beat-by-beat.

AN-715 INTRODUCTION TO CMOS INTEGRATED CIRCUITS WITH THREE-STATE OUTPUTS

This note describes a wide variety of standard CMOS integrated circuits incorporating transmission gates with standard logic. Design rules and applications of these devices include the areas of analog switching and multiplexing, digital multiplexing, and data transmission.

McMOS PART NUMBER TO APPLICATION NOTE CROSS REFERENCE

Motorola Part Number	Functional Description	Application Note AN Number
–	General Family Information	538A, 574, 591, 707, 712, 715
MC14000	Dual 3-Input NOR	712
MC14001	Quad 2-Input NOR	538, 713, 714
MC14002	Dual 4-Input NOR	538A
MC14007	Dual Pair and Inverter	715
MC14008	Four-Bit Full Adder	703
MC14009	Hex Inverter/Buffer	703, 712, 713
MC14010	Hex Buffer	703, 712
MC14011	Quad 2-Input NAND	538A, 707, 714
MC14012	Dual 4-Input NAND	538A
MC14013	Dual Type-D Flip-Flop	538A, 713, 714
MC14015	Dual 4-Stage Static Shift Register	715
MC14016	Quad Analog Switch	715
MC14017	Decade Counter/Divider	715
MC14022	Divide-by-8	715
MC14027	Dual J-K Flip-Flop	707
MC14034	8-Stage Static Bus Register	715
MCM14505	65-Bit RAM	715
MC14506	Expandable A.O.I.	715
MC14507	Quad Exclusive OR	538A
MC14508	Dual 4-Bit Latch	703, 715
MC14511	Latch and 7-Segment Decoder/Driver	713, 714
MC14512	8-Channel Data Selector	715
MC14517	Dual 64-Bit Static Shift Register	715
MC14518	Dual BCD Up Counter	538A, 713, 714
MC14519	4-Bit AND/OR Select	715
MC14522	Programmable BCD Divide-by-N 4-Bit Counter	714
MC14534	5 Decade Counter	715
MC14580	4 x 4 Multiport Register	715
MC14583	Dual Schmitt Trigger	715

REFERENCE LITERATURE

The following is a bibliography of articles containing information about, or designs using, Complementary MOS logic devices.

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MCMOS

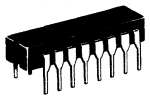
INTEGRATED CIRCUITS

Chapter 4

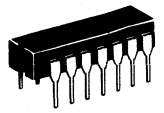
SELECTOR GUIDE

McMOS INTEGRATED CIRCUITS McMOS

MC14000 and MC14500 Series Complementary MOS



L SUFFIX
CERAMIC PACKAGE
CASE 620



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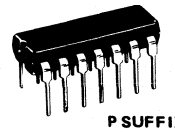
CASE 632



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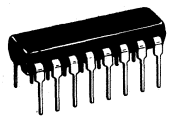

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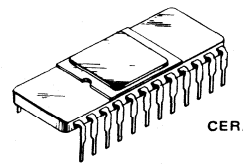


L SUFFIX
CERAMIC PACKAGE
CASE 684

4

FUNCTION AND CHARACTERISTICS

Function	Type		Quiescent Power Dissipation nW typ/pkg		Propagation Delay ns typ	Case	Page No.
			Series				
	V_{DD} = 18 Vdc −55 to +125°C	V_{DD} = 16 Vdc −40 to +85°C	AL	CL/CP			
Dual 3-Input NOR Gate/Inverter	MC14000AL	MC14000CL/CP	10	50	25	632,646	7-3
Quad 2-Input NOR Gate	MC14001AL	MC14001CL/CP	10	50	25	632,646	7-7
Dual 4-Input NOR Gate	MC14002AL	MC14002CL/CP	10	50	25	632,646	7-10
18-Bit Static Shift Register	MC14006AL	MC14006CL/CP	50	200	80	632,646	7-14
Dual Complementary Pair Plus Inverter	MC14007AL	MC14007CL/CP	10	50	15	632,646	7-18
4-Bit Full Adder	MC14008AL	MC14008CL/CP	1000	1000	170	620,648	7-22
Hex Inverter/Buffer	MC14009AL	MC14009CL/CP	100	500	9.0	620,648	7-28
Hex Noninverting Buffer	MC14010AL	MC14010CL/CP	100	500	20	620,648	7-28
Quad 2-Input NAND Gate	MC14011AL	MC14011CL/CP	10	50	25	632,646	7-33
Dual 4-Input NAND Gate	MC14012AL	MC14012CL/CP	10	50	25	632,646	7-36
Dual Type D Flip-Flop	MC14013AL	MC14013CL/CP	100	100	40	632,646	7-39
Dual 4-Bit Static Shift Register	MC14015AL	MC14015CL/CP	10 μW	10 μW	125	620,648	7-43
Quad Analog Switch/Quad Multiplexer	MC14016AL	MC14016CL/CP	200	200	7.0	632,646	7-50
Decade Counter/Divider	MC14017AL	MC14017CL/CP	5.0 μW	10 μW	200	620,648	7-56
14-Bit Binary Counter	MC14020AL	MC14020CL/CP	200	200	140	620,648	7-60
8-Bit Static Shift Register	MC14021AL	MC14021CL/CP	5000	5000	100	620,648	7-63
Octal Counter/Divider	MC10422AL	MC14022CL/CP	5.0 μW	10 μW	200	620,648	7-66
Triple 3-Input NAND Gate	MC14023AL	MC14023CL/CP	10	50	25	632,646	7-70
Seven-Stage Ripple Counter	MC14024AL	MC14024CL/CP	10	10	120	632,646	7-73
Triple 3-Input NOR Gate	MC14025AL	MC14025CL/CP	10	50	25	632,646	7-77
Dual J-K Flip-Flop	MC14027AL	MC14027CL/CP	50	200	75	620,648	7-81
BCD-To-Decimal Decoder/ Binary-To-Octal Decoder	MC14028AL	MC14028CL/CP	10	10	57	620,648	7-86
Triple Serial Adder (Positive Logic)	MC14032AL	MC14032CL/CP	1000	1000	90	620,648	7-90
8-Bit Universal Bus Register	MC14034AL	MC14034CL	5000	5000	175	684	7-94
4-Bit Parallal-In/Parallel-Out Shift Register	MC14035AL	MC14035CL/CP	100	100	100	620,648	7-99
Triple Serial Adder (Negative Logic)	MC14038AL	MC14038CL/CP	1000	1000	90	620,648	7-90
12-Bit Binary Counter	MC14040AL	MC14040CL/CP	200	200	140	620,648	7-103
Quad Latch	MC14042AL	MC14042CL/CP	50	500	40	620,648	7-107
Hex Inverter/Buffer	MC14049AL	MC14049CL/CP	100	500	18	620,648	7-110
Hex Buffer	MC14050AL	MC14050CL/CP	100	500	18	620,648	7-110

(continued)

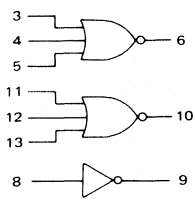
FUNCTION AND CHARACTERISTICS (continued)

Function	Type		Quiescent Power Dissipation nW typ/pkg		Propagation Delay ns typ	Case	Page No.
			Series				
	V_{DD} = 18 Vdc -55 to +125°C	V_{DD} = 16 Vdc -40 to +85°C	AL	CL/CP			
Triple Gate (Dual 4 Input NAND Gate and 2 Input NOR/OR Gate or 8 Input AND/NAND Gate)	MC14501AL	MC14501CL/CP	10	50	25	620,648	7-114
Strobed Hex Inverter/Buffer	MC14502AL	MC14502CL/CP	250	2500	20	620,648	7-120
Dual Expandable AND OR INVERT Gate	MC14506AL	MC14506CL/CP	100	100	80	620,648	7-124
Quad Exclusive OR Gate	MC14507AL	MC14507CL/CP	10	50	35	632,646	7-129
Dual 4 Bit Latch	MC14508AL	MC14508CL	1000	1000	55	684	7-134
BCD Up/Down Counter	MC14510AL	MC14510CL/CP	1000	1000	100	620,648	7-140
BCD To Seven Segment Latch/Decoder/Driver	MC14511AL	MC14511CL/CP	100	100	250	620,648	7-145
8 Channel Data Selector	MC14512AL	MC14512CL/CP	1000	1000	75	620,648	7-151
4 Bit Latch/4 to 16 Line Decoder (High)	MC14514AL	MC14514CL	200	200	300	684	7-155
4 Bit Latch/4 to 16 Line Decoder (Low)	MC14515AL	MC14515CL	200	200	300	684	7-155
Binary Up/Down Counter	MC14516AL	MC14516CL/CP	1000	1000	40	620,648	7-160
Dual 64 Bit Static Shift Register	MC14517AL	MC14517CL	500	1000	180	620	7-164
Dual BCD Up Counter	MC14518AL	MC14518CL/CP	4000	4000	100	620,648	7-168
4 Bit AND/OR Selector (Quad 2 Channel Data Selector or Quad Exclusive NOR Gate)	MC14519AL	MC14519CL/CP	100	100	85	620,648	7-174
Dual Binary Up Counter	MC14520AL	MC14520CL/CP	4000	4000	100	620,648	7-168
24 State Frequency Divider	MC14521AL	MC14521CL/CP	400	400	1700	620,648	7-178
Programmable Divide By N 4 Bit Counter (BCD)	MC14522AL	MC14522CL/CP	1000	1000	100	620,648	7-183
Programmable Divide By N 4 Bit Counter (Binary)	MC14526AL	MC14526CL/CP	1000	1000	100	620,648	7-183
BCD Rate Multiplier	MC14527AL	MC14527CL/CP	1000	1000	70	620,648	7-190
Dual Retriggerable/Resettable Monostable Multivibrator	MC14528AL	MC14528CL/CP	50	50	80	620,648	7-196
Dual 4 Channel Analog Data Selector	MC14529AL	MC14529CL/CP	250	250	–	620,648	7-200
Dual 5 Input Majority Logic Gate	MC14530AL	MC14530CL/CP	100	100	180	620,648	7-202
12 Bit Parity Tree	MC14531AL	MC14531CL/CP	100	100	140	620,648	7-206
8 Bit Priority Encoder	MC14532AL	MC14532CL/CP	50	50	80	620,648	7-208
Dual 4 Channel Data Selector/Multiplexer	MC14539AL	MC14539CL/CP	100	100	75	620,648	7-214
BCD To Seven Segment Latch/Decoder/Driver	MC14543AL	MC14543CL/CP	100	100	220	620,648	7-218
Successive Approximation Register	MC14549AL	MC14549CL/CP	500 μW	500 μW	180	620,648	7-222
2 x 2 Bit Parallel Binary Multiplier	MC14554AL	MC14554CL/CP	100	100	80	620,648	7-227
Dual Binary to 1 of 4 Decoder/Demultiplexer	MC14555AL	MC14555CL/CP	100	100	80	620,648	7-232
Dual Binary to 1 of 4 Decoder/ Demultiplexer (Inverting)	MC14556AL	MC14556CL/CP	100	100	90	620,648	7-232
Successive Approximation Register	MC14559AL	MC14559CL/CP	500 μW	500 μW	180	620,648	7-222
Quad 2 Input OR Gate	MC14570AL	MC14570CL/CP	28	28	45	632,646	7-235
4 Bit Arithmetic Logic Unit	MC14581AL	MC14581CL	100	100	225	684	7-238
Look Ahead Carry Block	MC14582AL	MC14582CL/CP	100	100	115	620,648	7-243
Dual Schmitt Trigger	MC14583AL	MC14583CL/CP	10	10	200	620,648	7-247
4 Bit Magnitude Comparator	MC14585AL	MC14585CL/CP	100	100	150	620,648	7-253
64 Bit Random Access Read Write Memory	MCM14505AL	MCM14505CL	300	300	Read Cycle = 150 Write Cycle = 200	632	7-257
1024 Bit Read Only Memory	MCM14524AL	MCM14524CL	31	31	180	620	7-265

McMOS LOGIC DIAGRAMS

GATES

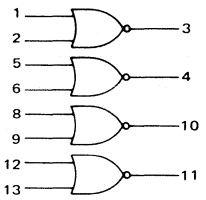
MC14000
Dual 3-Input NOR Gate plus inverter



V_{DD} = Pin 14
V_{SS} = Pin 7

$6 = \overline{3 + 4 + 5}$
$9 = \overline{8}$

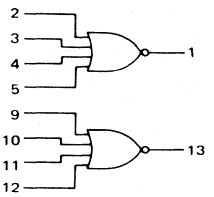
MC14001
Quad 2-Input NOR Gate



$3 = \overline{1+2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

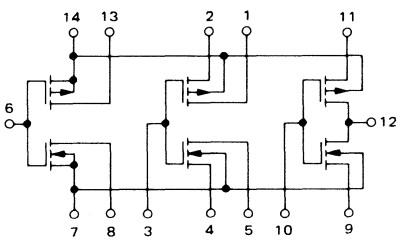
MC14002
Dual 4-Input NOR Gate



$1 = \overline{2 + 3 + 4 + 5}$

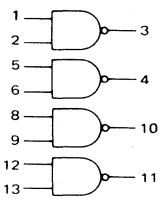
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14007
Dual Complementary Pair Plus Inverter



V_{DD} = Pin 14
V_{SS} = Pin 7

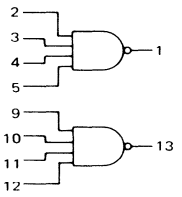
MC14011
Quad 2-Input NAND Gate



$3 = \overline{1 \bullet 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

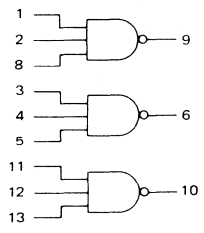
MC14012
Dual 4-Input NAND Gate



$1 = \overline{2 \bullet 3 \bullet 4 \bullet 5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

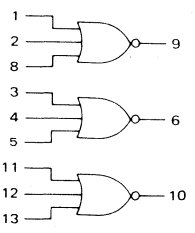
MC14023
Triple 3-Input NAND Gate



$9 = \overline{1 \bullet 2 \bullet 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14025
Triple 3-Input NOR Gate

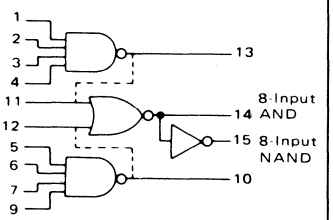


$9 = \overline{1 + 2 + 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14501
Triple Gate

Use Dotted Connection Externally to Obtain 8-Input Functions.



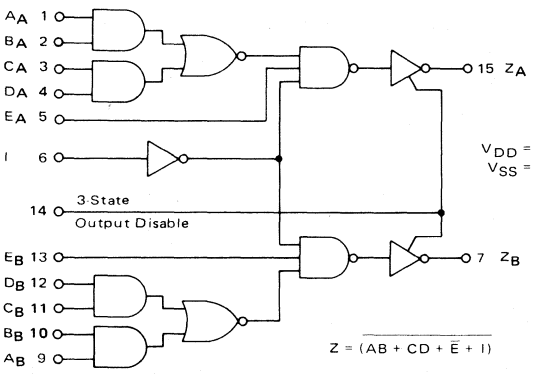
Note: Pin 14 must not be used as an input to the inverter.

V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS LOGIC DIAGRAMS

GATES (continued)

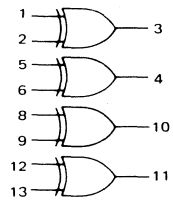
MC14506
Dual Expandable AND-OR-INVERT Gate



V_{DD} = Pin 16
V_{SS} = Pin 8

$Z = \overline{(AB + CD + E + I)}$

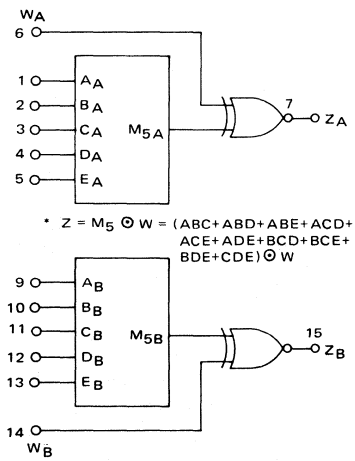
MC14507
Quad Exclusive OR Gate



$3 = 1 \oplus 2$

V_{DD} = Pin 14
V_{SS} = Pin 7

MC14530
Dual 5-Input Majority Logic Gate



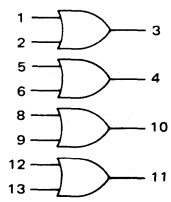
* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot \equiv$ Exclusive NOR $\equiv \overline{\text{Exclusive OR}}$

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14570
Quad 2-Input OR Gate

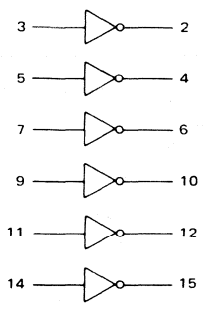


$3 = 1 + 2$

V_{DD} = Pin 14
V_{SS} = Pin 7

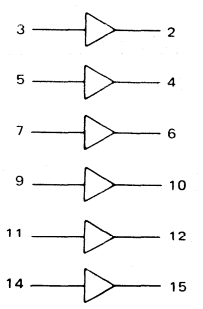
BUFFERS

MC14009
Hex Inverter/Buffer



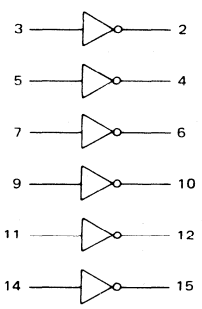
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14010
Hex Buffer



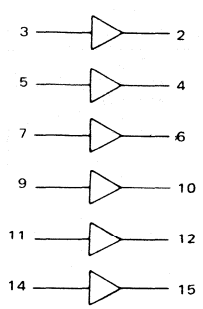
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14049
Hex Inverter/Buffer



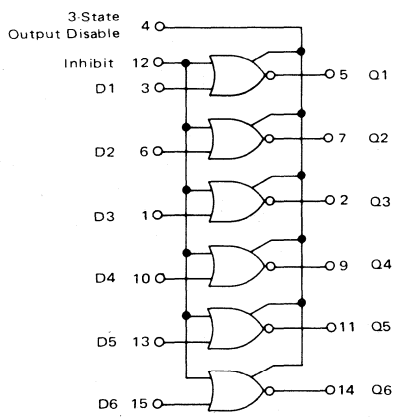
NC = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14050
Hex Buffer



NC = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

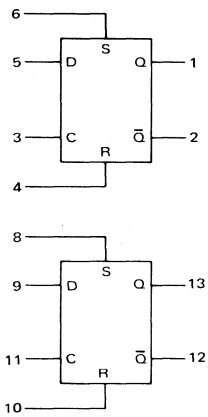
MC14502
Strobed Hex Inverter/Buffer



V_{DD} = Pin 16
V_{SS} = Pin 8

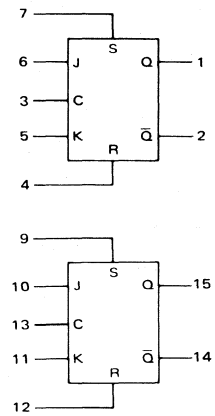
FLIP-FLOPS

MC14013
Dual Type D Flip-Flop



V_{DD} = Pin 14
V_{SS} = Pin 7

MC14027
Dual J-K Flip-Flop



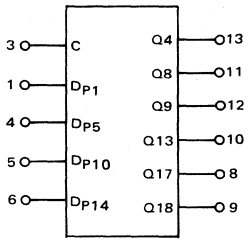
V_{DD} = Pin 16
V_{SS} = Pin 8

4

McMOS LOGIC DIAGRAMS

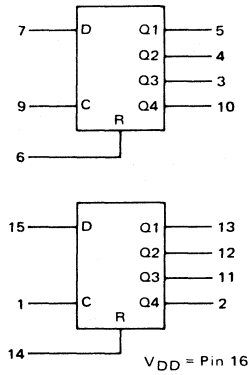
SHIFT REGISTERS

MC14006
18-Bit Static Shift Register



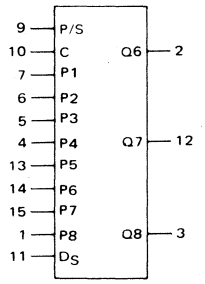
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14015
Dual 4-Bit Static Shift Register



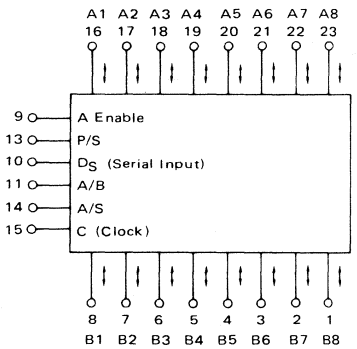
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14021
8-Bit Static Shift Register



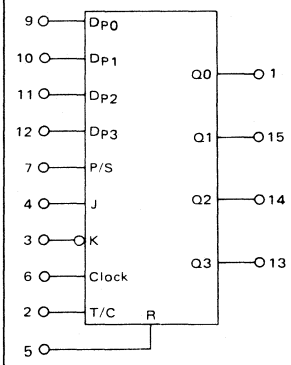
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14034
8-Bit Universal Bus Register



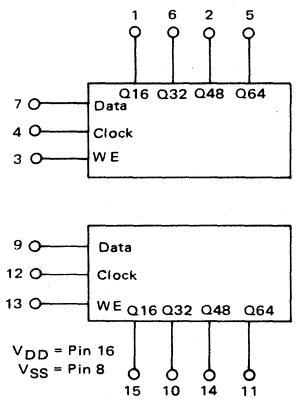
V_{DD} = Pin 24
V_{SS} = Pin 12

MC14035
4-Bit Parallel-In/Parallel Out Shift Register



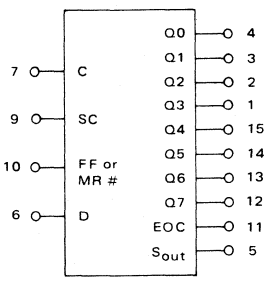
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14517
Dual 64-Bit Static Shift Register



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14549/MC14559
Successive Approximation Registers

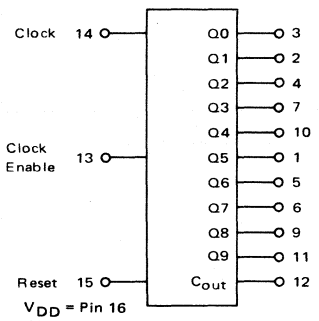


V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549 Pin 10 is MR input
For MC14559 Pin 10 is FF input

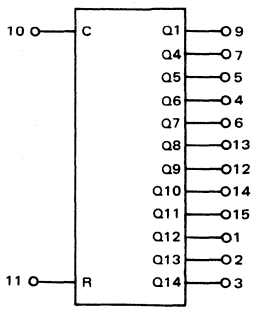
COUNTERS

MC14017
Decade Counter/Divider



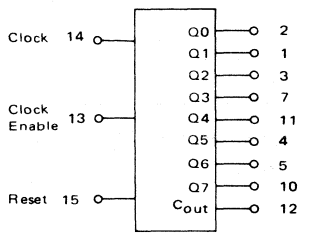
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14020
14-Bit Binary Counter



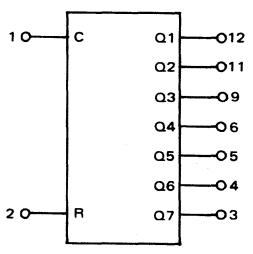
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14022
Octal Counter/Divider



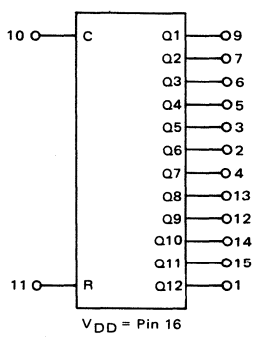
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14024
Seven-Stage Ripple Counter



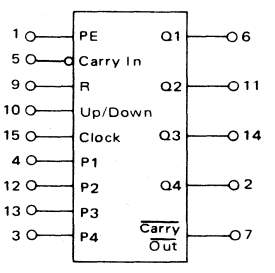
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14040
12-Bit Binary Counter



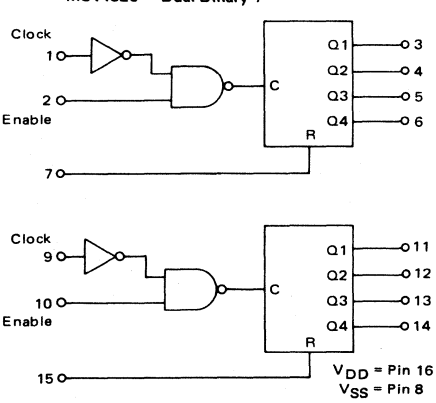
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14510 – BCD
MC14516 – Binary } **Up/Down Counters**



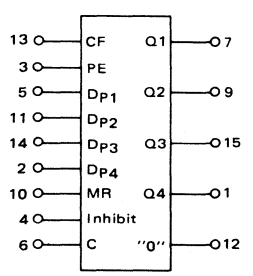
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14518 – Dual BCD
MC14520 – Dual Binary } **Up Counters**



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14522 – BCD
MC14526 – Binary } **Programmable Divide-by-N 4-Bit Counters**



V_{DD} = Pin 16
V_{SS} = Pin 8

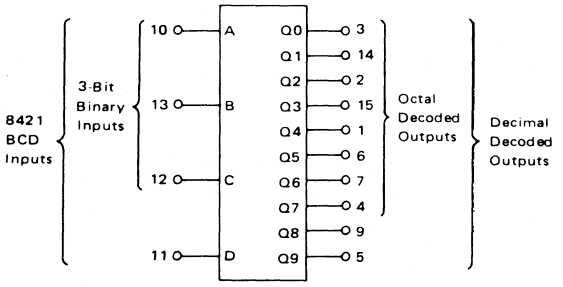
4

McMOS LOGIC DIAGRAMS

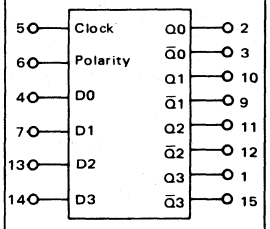
DECODERS/LATCHES

MC14028
BCD-to-Decimal Decoder
Binary-to-Octal Decoder

V_{DD} = Pin 16
V_{SS} = Pin 8

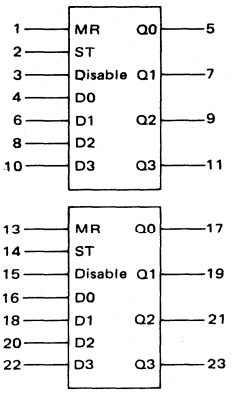


MC14042
Quad Latch



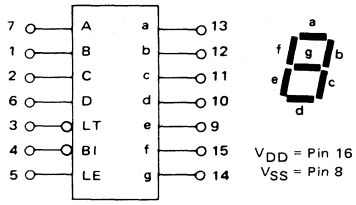
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14508
Dual 4-Bit Latch



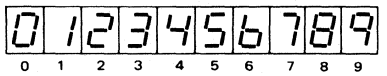
V_{DD} = Pin 24
V_{SS} = Pin 12

MC14511
BCD-to-Seven Segment
Latch/Decoder/Driver



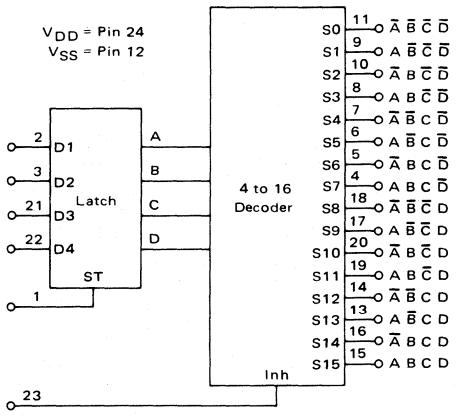
V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY



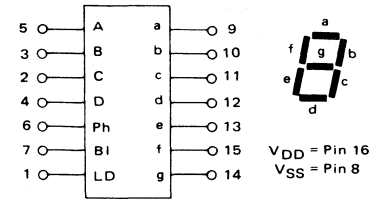
MC14514, MC14515
4-Bit Latch/4-to-16 Line Decoder

V_{DD} = Pin 24
V_{SS} = Pin 12



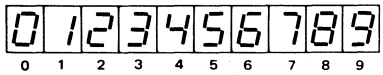
DECODERS/LATCHES (continued)

MC14543
BCD-To-Seven Segment Latch/Decoder/Driver

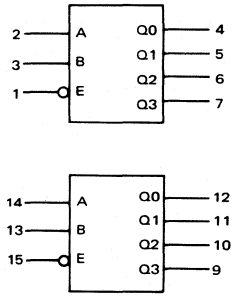


V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY

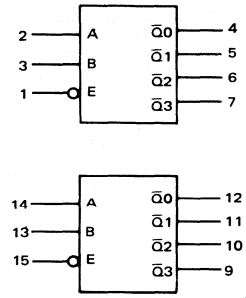


MC14555
Dual Binary To 1-of-4 Decoder/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8

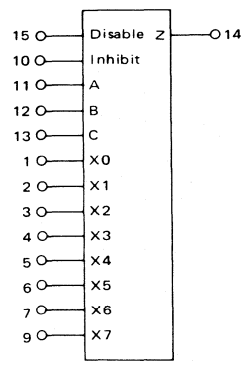
MC14556
Dual Binary To 1-of-4 Decoder/Demultiplexer



V_{DD} = Pin 16
V_{SS} = Pin 8

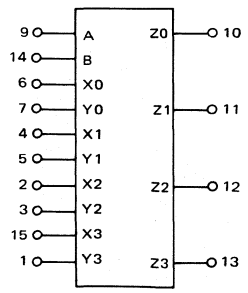
DATA ROUTING FUNCTIONS

MC14512
8-Channel Data Selector



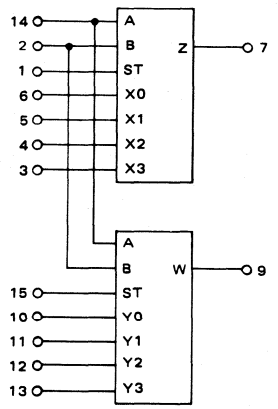
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14519
4-Bit AND/OR Selector



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14539
Dual 4-Channel Data Selector/Multiplexer



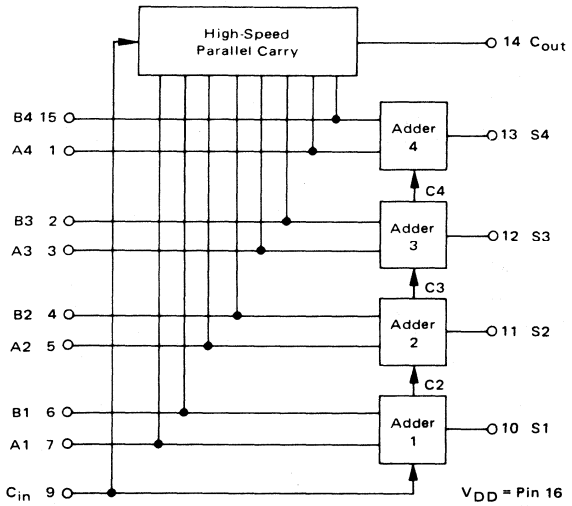
V_{DD} = Pin 16
V_{SS} = Pin 8

4

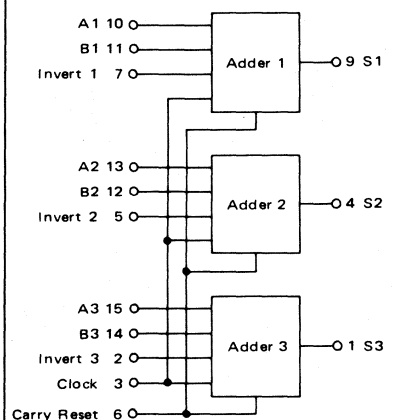
McMOS LOGIC DIAGRAMS

ARITHMETIC FUNCTIONS

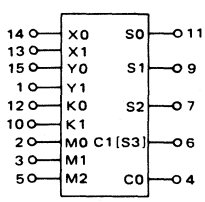
MC14008
4-Bit Full Adder



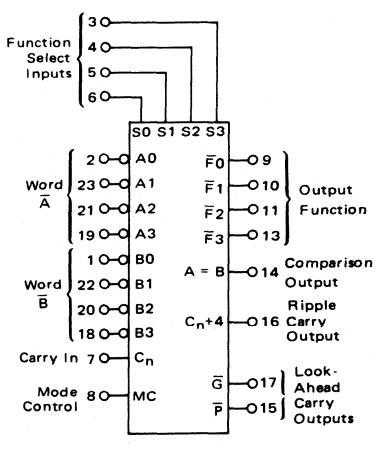
MC14032 – Positive Logic
MC14038 – Negative Logic
Triple Full Adders



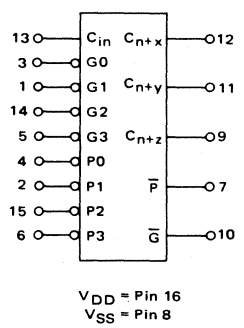
MC14554
2 x 2-Bit Parallel Binary Multiplier



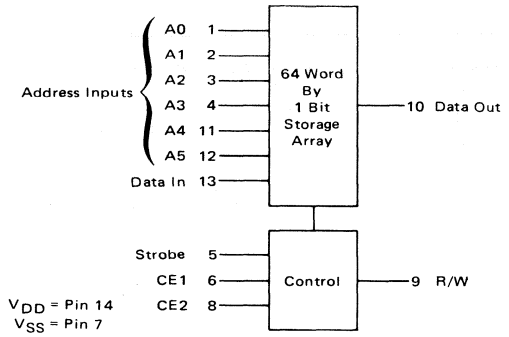
MC14581
Arithmetic Logic Unit



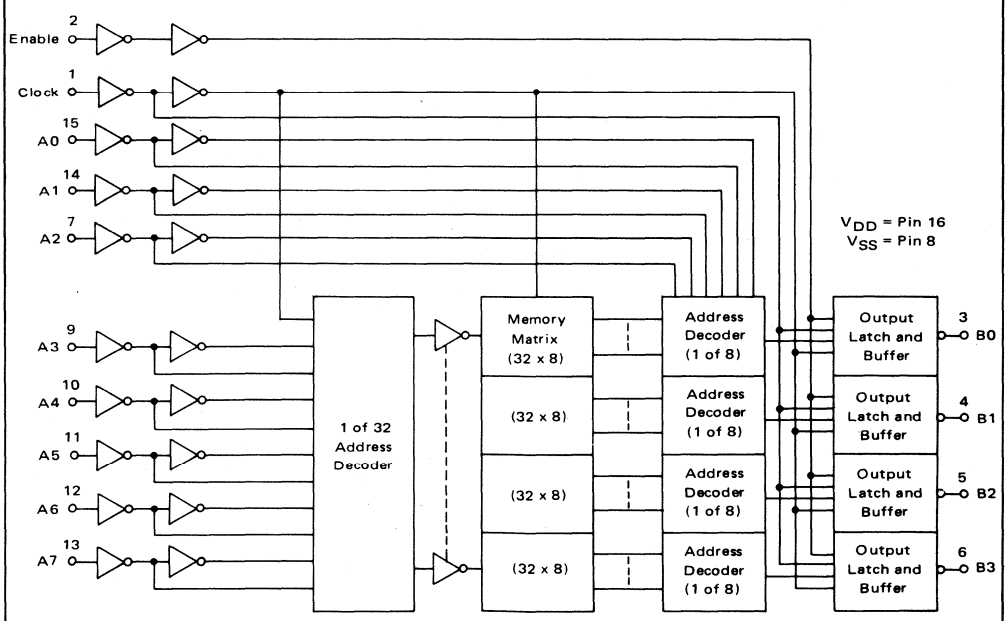
MC14582
Look-Ahead Carry Block



MCM14505
64-Bit Random Access Read-Write Memory



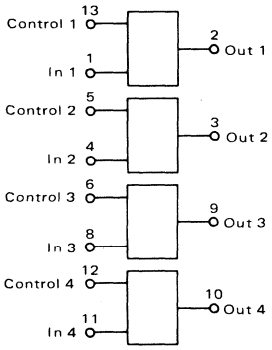
MCM14524
1024-Bit Read Only Memory



McMOS LOGIC DIAGRAMS

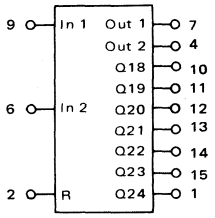
SPECIAL FUNCTIONS

MC14016
Quad Analog Switch
Quad Multiplexer



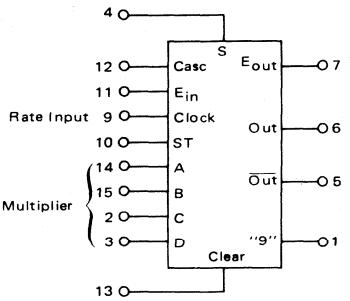
V_{DD} = Pin 14
V_{SS} = Pin 7

MC14521
24-Stage Frequency Divider



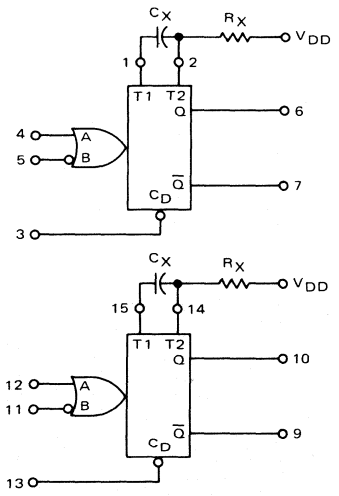
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14527
BCD Rate Multiplier



V_{DD} = Pin 16
V_{SS} = Pin 8

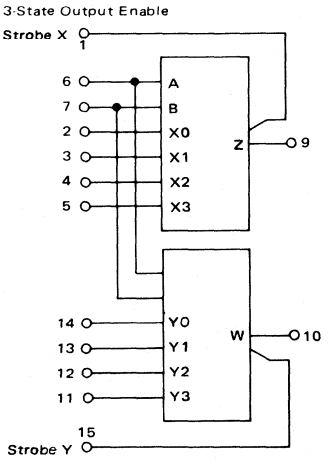
MC14528
Dual Retriggerable/Resettable
Monostable Multivibrator



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

MC14529
Dual 4-Channel Analog Data Selector
or
8-Channel Analog Data Selector

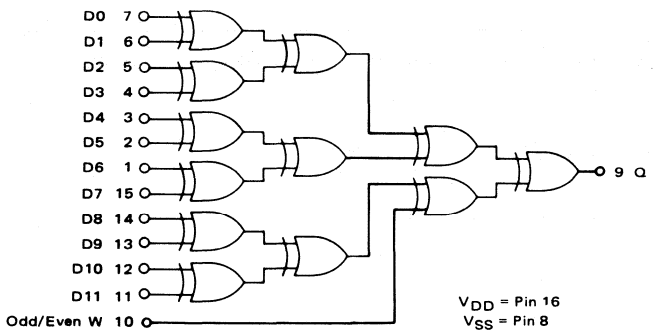


V_{DD} = Pin 16
V_{SS} = Pin 8

4

SPECIAL FUNCTIONS (continued)

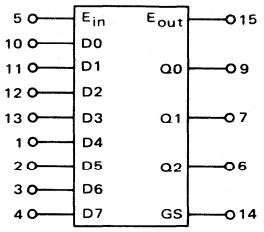
MC14531
12-Bit Parity Tree



V_{DD} = Pin 16
V_{SS} = Pin 8

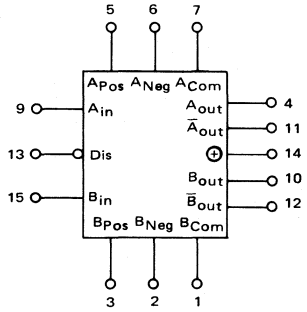
$Q = D0 \oplus D1 \oplus D2 \oplus \ldots . \oplus D11 \oplus W$

MC14532
8-Bit Priority Encoder



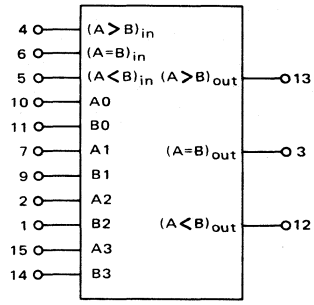
V_{DD} = Pin 16
V_{SS} = Pin 8

MC14583
Dual Schmitt Trigger



V_{DD} = Pin 16
V_{SS} = Pin 8

MC14585
4-Bit Magnitude Comparator



V_{DD} = Pin 16
V_{SS} = Pin 8

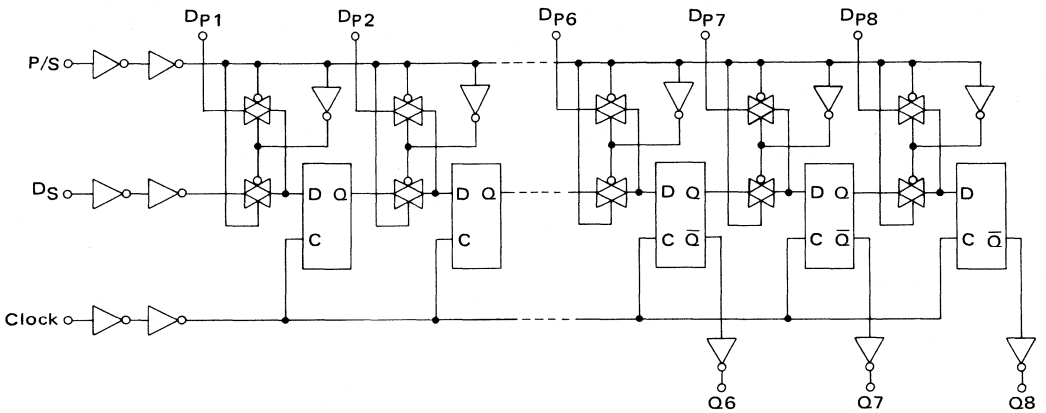
4

MC14014

8-Stage Static Shift Register

The MC14014 8-stage static shift register finds primary use in parallel to serial data conversion, synchronous parallel or serial input and serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity.

- Synchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 5.0 MHz @ V_{DD} = 10 V
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Pin-for-Pin Replacement for CD4014A



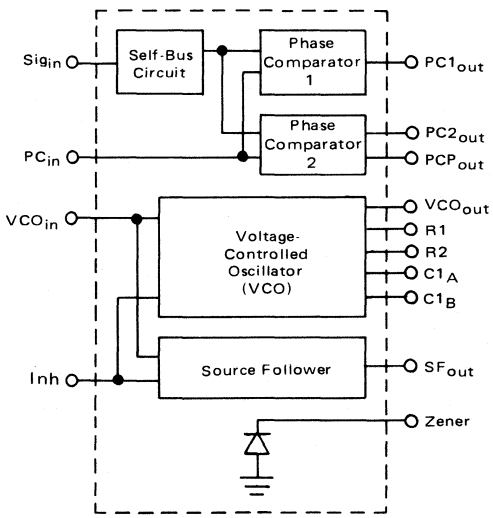
MC14046

Phase-Locked Loop

The MC14046 CMOS phase-locked loop contains two phase comparators, voltage controlled oscillator (VCO), source follower, and zener diode.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion, and motor control.

- Low Power Dissipation
- Low Frequency Drift With Temperature — 500 ppm/°C
- High VCO Linearity — 1.0% typical
- Pin-for-Pin Replacement for CD4046



MC14534

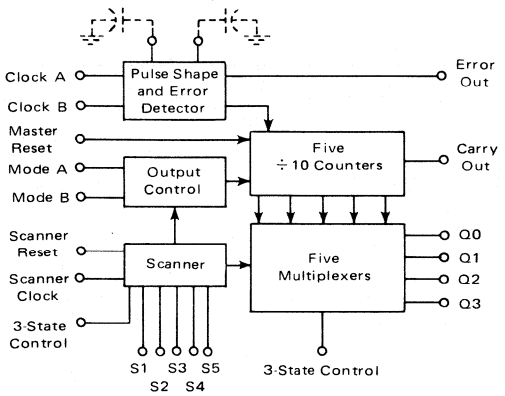
Real Time 5-Decade Counter

The MC14534 consists of five ripple-type decade counters whose outputs are time-multiplexed using an internal scanner. It can be used for any application requiring real time electronic counting and displaying.

Four modes of operation are available:

Mode 0 — Five-decade mode
Mode 1 — Test mode
Mode 2 — Four-decade counter with "half-pence" capability
Mode 3 — Four-decade counter with divide-by-ten and roundoff at the front end

- 3-State Output
- Fully Static Operation
- Pulse Shaping Permits Slow Rise Times On Inputs

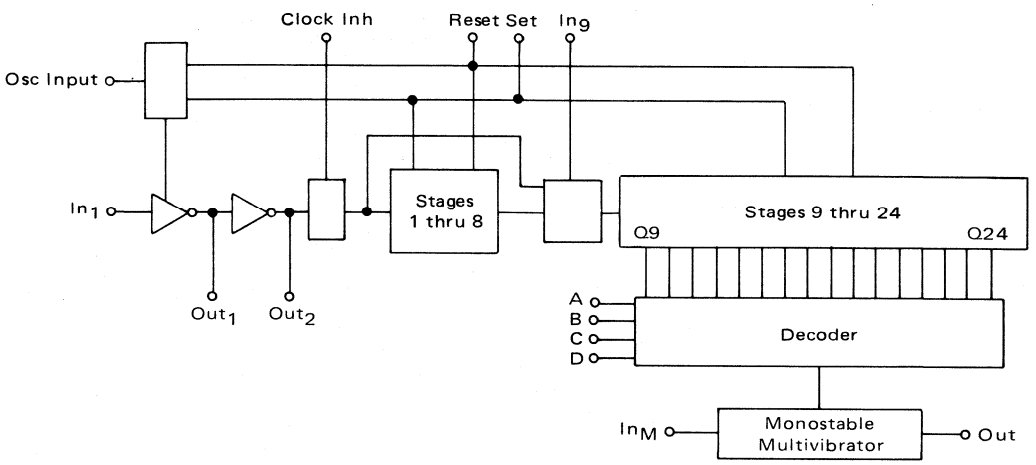


MC14536

Programmable Timer

The MC14536 programmable timer is a very flexible 24-stage ripple binary counter with the last 16-stages selectable by a four-bit binary code. Provisions for an on-chip RC oscillator, or an external clock are provided. An on-chip monostable circuit incorporating a pulse-type output has also been included. By selecting the appropriate output in conjunction with the correct input clock frequency, a variety of timing intervals can be achieved.

- 24 Flip-Flop Stages — Will Count From 2^0 to 2^{24}.
- First 8-Stage Bypass Input
- Set or Reset Function Disables the On-Chip RC Oscillator and Allows Very Low Power Standby Operation
- Various Pulse-Widths Can Be Obtained By Connecting the Monostable Circuit Pin to An RC Network
- Clock Input $f_{(max)}$ = 8.0 MHz typical @ V_{DD} = 10 Vdc
- Clock Conditioning Circuit Permits Operation With Very Slow Rise and Fall Times



MC14553

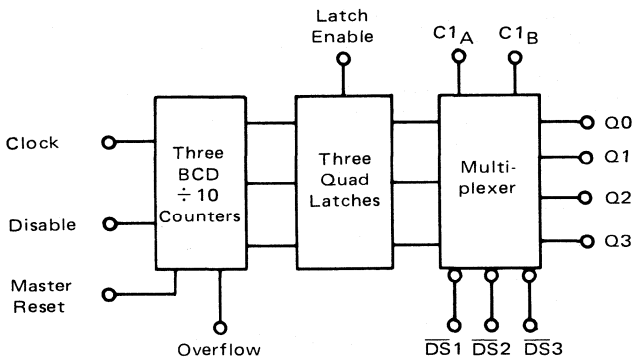
Three-Digit BCD Counter

The MC14553 three-digit BCD counter consists of three synchronous BCD counters which are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing one BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible.

An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector.

This device is useful in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

- Internal Or External Clock
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Slow Rise Times On Inputs



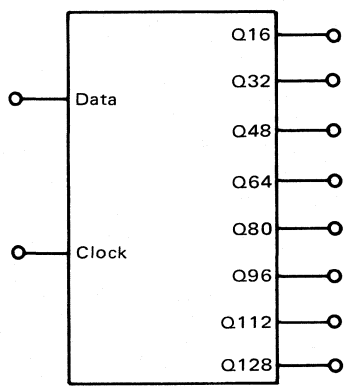
4

MC14562

128-Bit Static Shift Register

The MC14562 is a 128-bit static shift register. Data is clocked in and out of the shift register on the positive edge of the clock input. Data outputs are available every 16 bits, from 16 through 128.

- Fully Static Operation
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 5.0 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths — (1.5 MHz Operation @ V_{DD} = 10 Vdc)

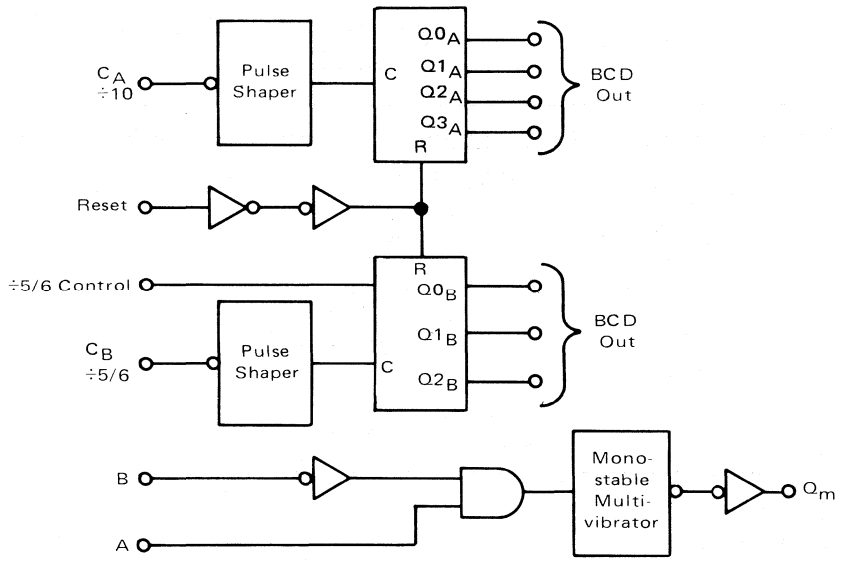


MC14566

Industrial Time Base Generator

The MC14566 industrial time base generator consists of a divide-by-10 ripple counter and a divide-by-5 or divide-by-6 ripple counter to permit stable time generation from a 50 or 60 Hz line. By cascading this device as divide-by-60 counters, seconds and minutes can be counted and are available in BCD format at the circuit outputs. An internal monostable multivibrator is included whose output can be used as a reset or clock pulse providing additional frequency flexibility. Also a pin has been included to allow divide-by-5 counting for generating 1.0 Hz from European 50 Hz line.

- Negative Edge Triggered Counters for Ease of Cascading
- Pulse Shapers on Counter Inputs Accept Slow Input Rise Times
- Monostable Multivibrator Positive or Negative Edge Triggered

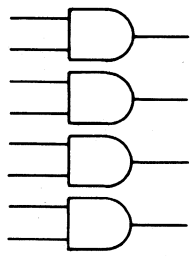


MC14571

Quad 2-Input AND Gate

The MC14571 is a quad 2-Input AND gate. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 5.0 nW/package typical @ V_{DD} = 5.0 V
- Noise Immunity = 45% of V_{DD} typical
- Fanout > 50
- Input Impedance = 10^{12} ohms typical

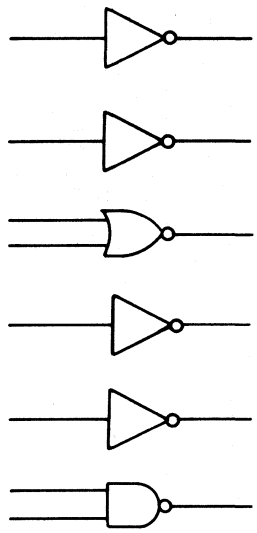


MC14572

Hex Functional Gate

The MC14572 is a hex functional gate. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired. The chip contains four inverters, one NOR gate and one NAND gate.

- Quiescent Power Dissipation = 25 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Fanout > 50
- Input Impedance = 10^{12} ohms typical



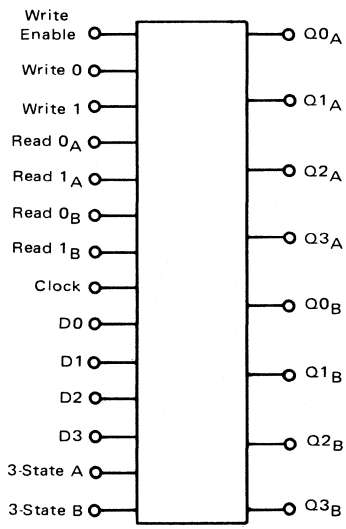
MC14580

4 x 4 Multiport Register

The MC14580 is a 4 by 4 multiport register useful in small scratch pad memories, arithmetic operations when coupled with an adder, and other data storage applications. It allows independent reading of any two words (or the same word at both outputs) while writing into any of four words.

Address changing and data entry occur on the rising edge of the clock. When the write enable input is low, the contents of any word may be accessed but not altered.

- Logic Swing Independent of Fanout
- No Restrictions on Clock Input Rise or Fall Times
- 3-State Outputs
- Single Phase Clocking

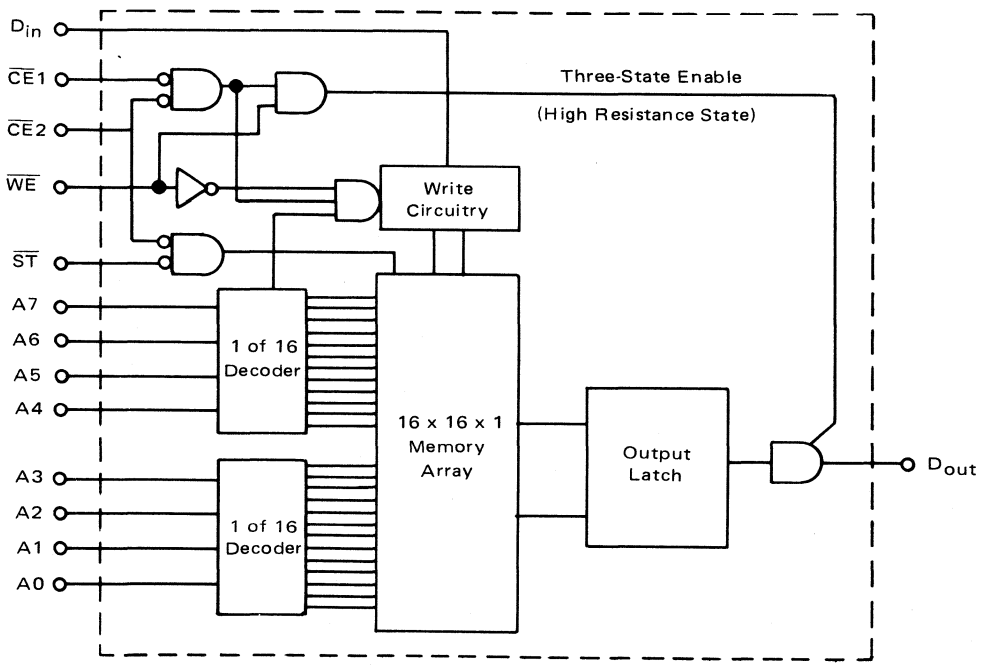


MCM14537

256-Bit Static Random Access Memory

The MCM14537 is a random access memory (RAM) organized in a 256 x 1-bit pattern. The circuit consists of eight address inputs (A_n), one data input (D_{in}), one write enable input ($\overline{WE}$), one strobe input ($\overline{ST}$), two chip enable inputs ($\overline{CE}_n$), and one data output (D_{out}).

- Quiescent Power Dissipation = 10 μW/package typical
- Wired-OR Output Capability (3-state output) for Memory Expansion
- Output Data Latch Eliminates Need for Storage Buffer
- Access Time = 700 ns typical @ V_{DD} = 10 Vdc
- Fully Decoded and Buffered



NOTES

McMOS
INTEGRATED CIRCUITS

Chapter 5
FAMILY DATA

INTRODUCTION

This chapter presents the complete family characteristics for the Motorola McMOS logic family. Included are: definitions, handling precautions, interface considerations, reliability factors, input/output capabilities, etc. Ready references for key device parameters are also presented for the design, layout, and fabrication of McMOS logic systems.

MC14000 AND MC14500 SERIES OF COMPLEMENTARY MOS

The McMOS series of monolithic integrated logic circuits provides the systems designer with a medium-speed integrated circuit family which approaches the ideal in performance. The low power dissipation and flexible power supply requirements of this device family greatly simplifies power supply design; the high noise immunity and large fan-out capability reduces parts count and simplifies printed circuit board layouts.

The MC14000 and MC14500 series devices are designed with particular attention given to achieving unified, family-oriented specifications. Therefore, all devices in this series exhibit common performance characteristics appropriate to the respective logic function (gate, flip-flop, counter, etc.) and temperature-voltage series, including guaranteed family interface parameters.

Three categories of McMOS integrated circuits are available. The categories are: the AL ceramic, the CL ceramic, and the CP plastic devices. The AL ceramic package provides the most stringent device limits with the widest temperature range for military applications. The CL ceramic package and the CP plastic package both provide wider device limits with a narrower temperature range for less demanding applications. Table 5-1 lists the key characteristics of each device category.

All McMOS devices may also be obtained in chip form for the user concerned with manufacturing hybrid microcircuits. For this purpose, consult the Motorola Semiconductor Chips Data Book for listings.

COMMON FEATURES

The McMOS series provides all the basic gates, flip-flops, storage elements, and complex logic required to perform all digital system functions. In addition, many McMOS components are well adapted to both analog and linear design applications. Following are primary design features of the McMOS device family.

- Diode Protection on All Device Inputs
- Noise Immunity:
  45% of V_{DD} Typical
  30% of V_{DD} Guaranteed Minimum
- Buffered Output Compatible with HTL or Low Power TTL
- Low Quiescent Power Dissipation: 25 nW per package Typical (V_{DD} of 5 Vdc)
- Wide Power Supply Range:
  3 to 18 Vdc for AL device category
  3 to 16 Vdc for CL and CP device categories
- Single Supply Operation: Positive or Negative
- High Fan-out: greater than 50
- Logic Swing: independent of fan-out
- Input Impedance: 10^{12} Ohms Typical
- Low Input Capacitance: 5 pF Typical

RELIABILITY

All McMOS series devices receive reliability and quality assurance with in-line monitor verification of all dc, functional, and switching parameters. In addition, all AL category devices receive the following 100% high-reliability processing steps.

- Internal Visual Inspection:
  MIL-STD-883, Method 2010.1B (modified)
- Temperature Cycling:
  MIL-STD-883, Method 1010C (10 cycles, 65 to 150°C)
- Fine Leak Test (Sample):
  MIL-STD-883, Method 1014A (10^{-8} atm cc/s)
- Gross Leak Test: Dye Penetrant
- Marking: per Specification
- External Visual Examination:
  MIL-STD-883, Method 2009

INPUT CONSIDERATIONS

McMOS logic has high impedance inputs (typically 10^{12} ohms and 5 pF) which result in minimum loading of previous driving stages. When McMOS is used with other CMOS devices, the interface is simplified, provided the V_{DD} and V_{SS} supply voltages are the same. Due to the wide supply voltage range and high input impedance,

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TABLE 5–1 McMOS CHARACTERISTICS AND CATEGORIES

Characteristic	AL	CL	CP
Supply Voltage Range	3.0 to 18 volts	3.0 to 16 volts	3.0 to 16 volts
Operating Temperature Range	−55°C to +125°C	−40°C to +85°C	−40°C to +85°C
Package Type	Hermetic Ceramic	Hermetic Ceramic	Plastic
Processing Level	100% Hi-Rel	Industrial	Industrial

McMOS may be used with other logic families either directly or with a resistor component to guarantee noise immunity. See the section in Chapter 2 entitled Interfacing for more details.

McMOS has one of the highest noise immunity characteristics of any logic family. Typically, the threshold of the input/output transfer characteristic is nearly 50% of the supply voltage value and is virtually temperature insensitive. A range of 30% of V_{DD} minus V_{SS} on either side of the supply voltages (V_{SS} and V_{DD}) is guaranteed. Thus, variation of input levels and transients can be tolerated without a change occurring in the output state(s).

OUTPUT CONSIDERATIONS

McMOS logic outputs are capable of driving other CMOS inputs with almost unlimited fan-out capability. It has been estimated (worst case) that not less than 1000 CMOS inputs (i.e., a fan-out of 1000) can be driven by a single McMOS output before the output voltage fails to meet the guaranteed noise immunity range. The only system consideration is the reduction of speed with the addition of capacitive loading. When CMOS is used with other logic families which have resistive inputs (i.e., DTL, ECL, HTL, LTTL, RTL, or TTL), a specific fan-out should be assigned. For LTTL, the McMOS fan-out is equal to one over temperature (V_{DD} = 5 Vdc). For HTTL, the McMOS fan-out is equal to one over temperature (V_{DD} = 15 Vdc). Special parts may drive up to one or two regular TTL loads. Paralleling of McMOS outputs will provide a greater output drive capability. In general, the output drive current (sink and source) versus the output voltage, minus the supply voltage (i.e., the MOS drain-source voltage) is given for supply voltages of from 5 to 15 volts and for temperatures of from $-55^{o}C$ to $125^{o}C$. The typical values are representative of the standard output buffer devices used in the McMOS series.

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SPEED CONSIDERATIONS

The typical family curves shown later in this chapter indicate the rise and fall transition times for the standard buffer driver and for the turn-off and turn-on propagation times for a specific example over load capacitance C_L. The equations or curves used in the McMOS data sheets serve as aids in calculating those typical time parameters over load capacitance values that are not 15 pF. Extrapolation over different supply voltages can easily be made since the equations are given for supply voltages of 5, 10, and 15 volts.

A special feature of certain McMOS synchronous circuits is a clock conditioning input that virtually eliminates the rise and fall time restraints of the clock signal. More detailed information is contained in the individual device data sheets.

THREE-STATE OUTPUTS

Some McMOS devices have been designed with three-state capability. This feature is used in systems where common input/output busses exist. When disabled, the output becomes a high-impedance that disconnects the device from the bus lines. With the three-state enable OFF, the output has the characteristics of a regular McMOS driver so that information can be transmitted on the data bus.

INPUT PROTECTION CIRCUIT AND HANDLING

All McMOS circuits have built-in protection circuitry on all inputs to prevent damage to the MOS input gates of the device. The MOS gates consist of a metal layer over a thin silicon dioxide layer making contact with the silicon die. This gate oxide can tolerate approximately 100 volts, but electrostatic potentials can build-up to several hundred volts with sufficient energy content to rupture the oxide. To prevent this action, an input diode and resistor network is used to dissipate the electrical energy before damage occurs. However, this structure does not mean that precautions may be neglected. Therefore, it is recommended that McMOS circuits be left in their conductive carriers until they are used, and that equipment used to insert those devices into boards be sufficiently grounded to avoid any static charge build-up.

UNUSED INPUTS

Unused inputs must always be electrically connected to an appropriate logic voltage (e.g., either V_{SS} or V_{DD}). If those inputs are not tied in this manner, the input protection structure may "float" to some undesired voltage level that prevents the device from functioning properly. In addition, "floating" inputs may be subjected to damaging electrostatic potentials.

INPUT, OUTPUT SIGNALS AND SUPPLY VOLTAGES

The supply voltages to McMOS integrated circuits must be applied before the input signals for proper operation. Input and output voltages should be constrained within the supply voltage range [i.e., $(V_{SS} - 0.5\ V) \leqslant (V_{in}$ or $V_{out}) \leqslant (V_{DD} + 0.5\ V)$], since high energy-backed levels or transients outside this range can damage the input or output diode structures and possibly initiate a latch-up (or SCR) situation. The SCR situation occurs since any CMOS integrated circuit has parasitic NPN and PNP bipolar devices in its structure that electrically couple when current flows through the bases of those devices. Normal low energy overshoot and undershoot transients will not cause system problems.

The following Tables present a summary of the significant ratings and characteristics for the McMOS devices series. Table 5-2 presents maximum device ratings and Table 5-3 details device electrical characteristics.

TABLE 5-2 – MAXIMUM RATINGS

Rating	Symbol	*AL Series	CL/CP Series	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	–	Vdc
DC Current Drain per Pin	I	10	–	mAdc
Operating Temperature Range AL Series CL/CP Series	T_A	-55 to +125	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	–	°C

*Voltage referenced to V_{SS}.

TABLE 5-3 – ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS $T_A = 25°C$

Characteristic	Symbol	V_{DD} Vdc	AL Series Min	AL Series Typ	AL Series Max	CL/CP Series Min	CL/CP Series Typ	CL/CP Series Max	Unit
Operating Power Supply Voltage	V_{DD}	–	3.0	–	18	3.0	–	16	Vdc
Output Voltage (V_{in} = V_{DD} or V_{SS}) "0" Level	V_{out}	–	–	–	V_{SS} +0.01	–	–	V_{SS} +0.01	Vdc
"1" Level		–	V_{DD} -0.01	–	–	V_{DD} -0.01	–	–	
Noise Immunity* "0" Level	V_{NL}	–	30% V_{DD}	45% V_{DD}	–	30% V_{DD}	45% V_{DD}	–	Vdc
"1" Level	V_{NH}	–	30% V_{DD}	45% V_{DD}	–	30% V_{DD}	45% V_{DD}	–	Vdc
Output Drive Current									
P-Channel (I_{source})	I_{OH}								mAdc
(V_{OH} = 2.5 Vdc)		5.0	-0.5	-1.7	–	-0.2	-1.7	–	
(V_{OH} = 9.5 Vdc)		10	-0.5	-0.9	–	-0.2	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	–	-3.5	–	–	-3.5	–	
N-Channel (I_{sink})	I_{OL}								mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.4	0.8	–	0.2	0.8	–	
(V_{OL} = 0.5 Vdc)		10	0.9	1.2	–	0.5	1.2	–	
(V_{OL} = 1.5 Vdc)		15	–	7.8	–	–	7.8	–	
Input Current ($V_{SS} \leq V_{in} \leq V_{DD}$)	I_{in}	–	–	10	–	–	10	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	5.0	–	–	5.0	–	pF
Quiescent Dissipation	P_D								mW
Gates		5.0	–	0.000025	0.00025	–	0.000025	0.0025	
		10	–	0.00010	0.0010	–	0.00010	0.010	
		15	–	0.00025	–	–	0.00025	–	
Dual Flip-Flops		5.0	–	0.000025	0.005	–	0.000025	0.05	
		10	–	0.00010	0.02	–	0.00010	0.2	
		15	–	0.00025	–	–	0.00025	–	
Output Rise and Fall Times (10-90%)	t_r,t_f								ns
(C_L = 15 pF)		5.0	–	70	175	–	70	200	
		10	–	35	75	–	35	110	
		15	–	25	–	–	25	–	
Gate Turn-On Delay, Turn-Off Delay (50% of input waveform to 50% of output waveform) (C_L = 15 pF)	t_{PHL},t_{PLH}	5.0	–	60	75	–	60	100	ns
		10	–	25	50	–	25	160	
		15	–	12	–	–	12	–	
Clock Repetition Rate (C_L = 15 pF)	PRF								MHz
Flip-Flops		5.0	2.5	4.0	–	1.0	4.0	–	
		10	7.0	10	–	5.0	10	–	
		15	–	13	–	–	13	–	
Counters, Registers		5.0	1.5	3.0	–	1.0	3.0	–	
		10	3.0	5.0	–	2.0	5.0	–	
		15	–	8.0	–	–	8.0	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level, that the circuit will withstand before producing an output state change.

TYPICAL McMOS GATE CHARACTERISTICS

Figures 5-1 through 5-11 illustrate typical McMOS family gate characteristics.

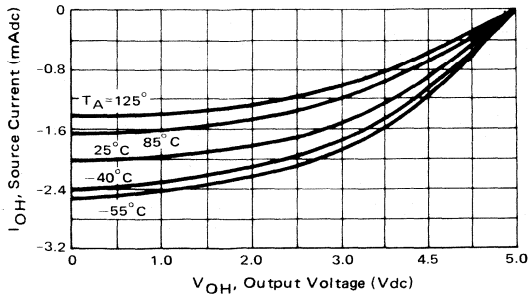

FIGURE 5-1 – V_{GS} = -5.0 Vdc, V_{DD} = 5.0 Vdc

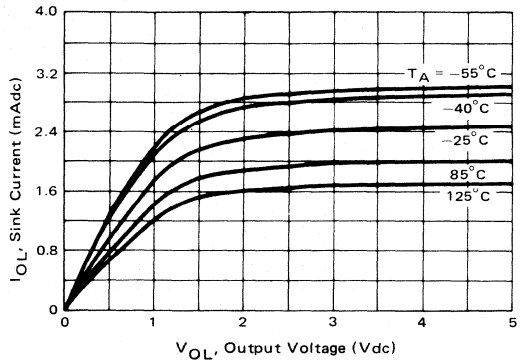

FIGURE 5-4 – V_{GS} = 5.0 Vdc, V_{DD} = 5.0 Vdc

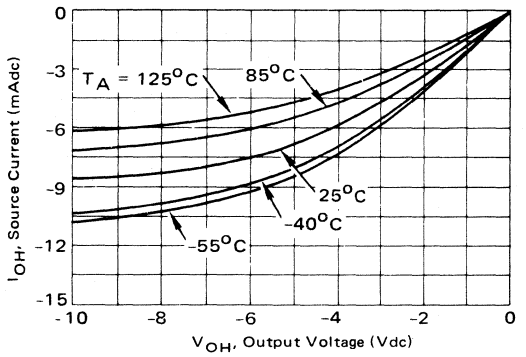

FIGURE 5-2 – V_{GS} = -10 Vdc, V_{DD} = 10 Vdc

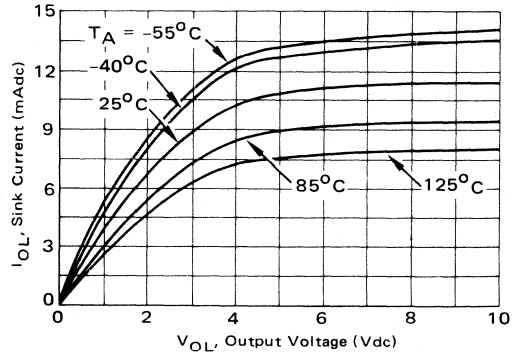

FIGURE 5-5 – V_{GS} = 10 Vdc, V_{DD} = 10 Vdc

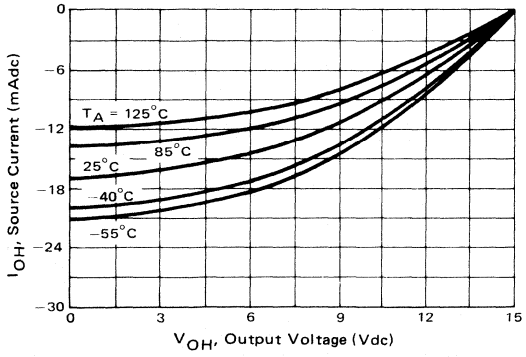

FIGURE 5-3 – V_{GS} = -15 Vdc, V_{DD} = 15 Vdc

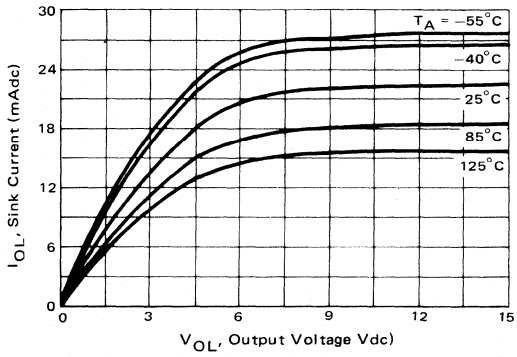

FIGURE 5-6 – V_{GS} = 15 Vdc, V_{DD} = 15 Vdc

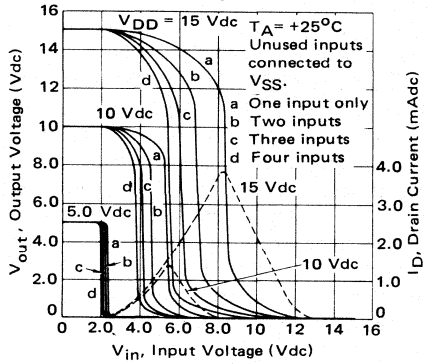

FIGURE 5-7 – VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS OF FOUR-INPUT NOR GATE

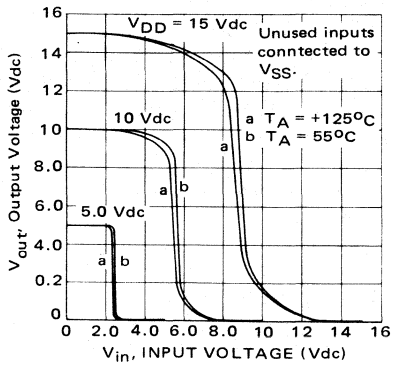

FIGURE 5-8 – VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

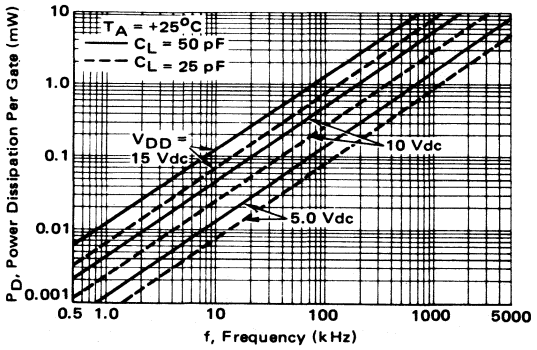

FIGURE 5-9 – GATE POWER DISSIPATION CHARACTERISTICS

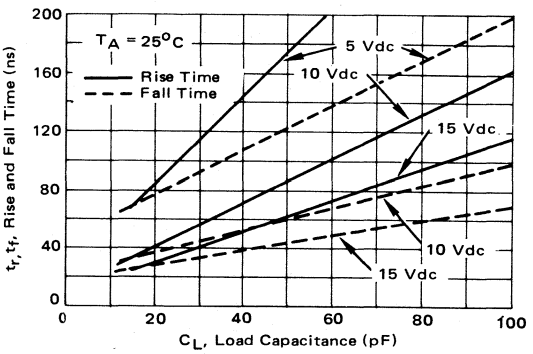

FIGURE 5-10 – RISE AND FALL TIME versus LOAD CAPACITANCE

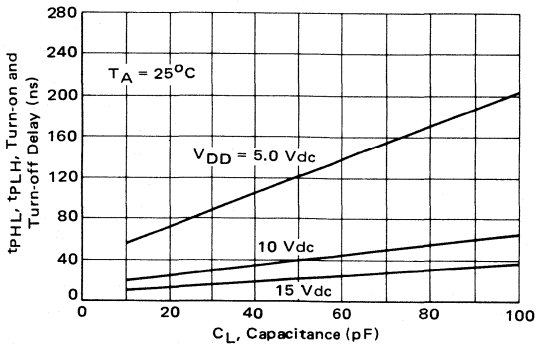

FIGURE 5-11 – TURN-ON AND TURN-OFF DELAY CHARACTERISTICS

FAMILY DEFINITIONS, CONCEPTS, AND CONVENTIONS

The following information provides detailed explanations, concepts, and conventions found in the McMOS data sheets. The basic topics covered are family characteristics and maximum ratings, distinct part characteristics (power dissipation, timing parameters, and three-state parameters), and logic symbols and conventions.

With few exceptions, the typical parameter values and their associated limits follow the industry standard guidelines recommended by the EIA. Any parameter has a statistical distribution with a statistical mean or typical value. A limit-window, consisting of minimum and maximum limit values surrounds the typical value of the parameter. The standard (see Figure 5-12) is such that the minimum limit values are below the typical value and the maximum limit values are above the typical value.

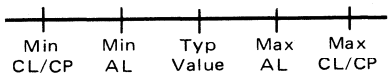

FIGURE 5-12 – McMOS FAMILY LIMIT-WINDOW

In the majority of cases, only one pair of limits are specified (the minimum pair or the maximum pair); this gives a half limit-window for a given parameter. Certain parameters may require a prefix of minimum or maximum attached to the name. These prefixes should not be confused with minimum and maximum designations used on value limits. For example, a dynamic shift register can have a minimum clock frequency as well as a maximum clock frequency. For both parameters, half-window-limits are specified. Thus, the minimum clock frequency will have maximum limit values and the maximum clock frequency will have minimum limit values.

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FAMILY CHARACTERISTICS AND MAXIMUM RATINGS

Maximum ratings are absolute values that constrain the integrated circuit devices within ranges where reliable operation still occurs. The maximum rating parameters are supply and input voltages, current flowing through any pin, operating and storage temperatures, and power dissipation.

DC SUPPLY VOLTAGE RANGE (V_{DD})

The range of voltages applied between the V_{DD} supply pin and the V_{SS} supply pin cover the full temperature range of a specific category. For the AL category, the working operating range varies from 3 to 18 volts. The maximum range for preventing damage to this category unit varies from −0.5 to 18 volts. For the CL/CP category, the working operating range varies from 3 to 16 volts. The maximum range for preventing damage to these categories vary from −0.5 to 16 volts.

INPUT VOLTAGE RANGE (ALL INPUTS) (V_{IN})

For either of the AL or CL/CP category devices, the input voltage should not exceed the V_{SS} and V_{DD} supply voltages by more than 0.5 volts [i.e., $(V_{SS}-0.5\ V) \leq V_{IN} \leq (V_{DD}+0.5\ V)$]. Exceeding the supply voltages for an excessive period of time may damage the input protection diode structure (since the diodes are forward-biased), or initiate a latch-up (SCR) condition. Fast overshoot or undershoot transients usually will not cause problems, since the cumulative energy content is too small to initiate any action. Refer to the section entitled Input Protection and Handling in this chapter for more details.

DC CURRENT DRAIN PER PIN (I)

For either of the AL or CL/CP category devices, the maximum current that can flow into or out of any input, output, or supply pin is 10 mA maximum over the full temperature range. A few special McMOS integrated circuits will have higher current values for certain pins and will be designated as such on their data sheets.

OPERATING TEMPERATURE RANGE (T_A)

The maximum ambient temperature range with the device operating is −55°C to 125°C for the AL category, and −40°C to +85°C for the CL/CP categories. A few special McMOS integrated circuits will have power derating curves which may reduce the working temperature range depending upon the device power dissipation. The section entitled Maximum Power Dissipation in this chapter will provide additional details.

STORAGE TEMPERATURE RANGE (T_{stg})

The temperature range at which the units can be stored without electrical connection is −65°C to 150°C for the AL and CL categories, and −65°C to 125°C for the CP category.

MAXIMUM POWER DISSIPATION (P_{OH}max, P_{OL}max and P_{DD}max)

Maximum power dissipation is defined either on a per output basis or on a total package basis depending on the special McMOS device that requires this rating. The majority of McMOS devices do not need this rating, since the 10 mA maximum current rating for the V_{DD} and V_{SS} supply pins prevents any device from dissipating the maximum rating of the package and integrated circuit die. On a per pin basis, P_{OH}max and P_{OL}max can be used to determine the required source and sink conditions given by I_{OH} $(V_{OH} - V_{DD})$ and I_{OL} $(V_{OL} - V_{SS})$, respectively. On a per package basis, P_{DD}max can be used to determine the required supply conditions given by I_{XX}, $(V_{DD} - V_{SS})$, where V_{DD} and V_{SS} are the supply voltages, and I_{XX} is the associated supply current I_{DD} or I_{SS}, whichever is the largest in absolute magnitude. In addition to this rating, power/temperature derating curves may be given. A more detailed discussion is given in Chapter 2.

FAMILY DATA AND CHARACTERISTICS

Family characteristics are parameters whose limits are common and consistent from one McMOS device to another McMOS device, with only minor exceptions. These characteristics assure the user that each device will be consistent in terms of fan-out, not only in driving other McMOS devices, but in driving other logic families, such as HTL and Low Power TTL. The specific parameters covered are output voltage, dc noise immunity, output drive and input currents, input capacitance, and transition times.

OUTPUT VOLTAGE (V_{out})

This is the voltage that appears at any output under a very high impedance load (no load). This parameter is guaranteed for supply voltages of 5 and 10 volts to fall within a range of 10 mV from either V_{SS} or V_{DD} supply voltages for temperatures of 25°C, -45°C, and -55°C, and within a range of 50 mV for temperatures of +85°C and 125°C.

DC NOISE IMMUNITY (V_{NL} AND V_{NH})

The dc noise immunity is defined as the input voltage range from an ideal "1" or "0" input level (assuming the previous McMOS driving stage is unloaded) which does not produce output state (combination) change(s). McMOS devices are guaranteed not to produce state change(s) provided the levels (or transients) are within a range of 30% of V_{DD} minus V_{SS}. Typically, the range is as large as 45% of V_{DD} minus V_{SS}. The outputs are considered not to have changed their states if the voltage output levels are within a range of 30% of V_{DD} minus V_{SS} from the supply voltages V_{DD} and V_{SS}. Figure 5-13 illustrates typical McMOS family inverting and non-inverting functions.

OUTPUT DRIVE CURRENTS (I_{OH} AND I_{OL})

The output drive current is the sourcing current (I_{OH}) with the output high, or the sinking current (I_{OL}) with the output low, that flows into or out of a load having a specific voltage value. For a supply voltage of 5 volts, the current values will drive over the full temperature range of a single, low-power TTL load. For a supply voltage of 10 volts, the current values reflect a general CMOS industry load condition of 0.5 volt from either supply voltage (i.e., V_{SS} and V_{DD}). For a supply voltage of 15 volts, the current values are designed to drive a standard HTL load over the specified temperature range. The limits over a temperature range are selected to reflect the 3% current decrease with every degree of Centigrade temperature increase (with respect to 25°C) that occurs with all CMOS devices.

INPUT CURRENT (I_{in})

Input current is defined as the current that flows with the application of a V_{SS} or V_{DD} voltage level at the input. The main contribution of this current, typically 10 pA (corresponding to a 10^{12} ohm resistor with 10 volts in parallel), corresponds with the diode protection circuit used at the device input.

INPUT CAPACITANCE (C_{in})

The input capacitance is defined and measured as the ac capacity under zero bias conditions (V_{SS} = 0) as applied to any input. This capacitance is typically 5 pF.

RISE AND FALL TRANSITION TIMES (t_r AND t_f)

The output rise and fall transition times are defined as the low-to-high and high-to-low transi-

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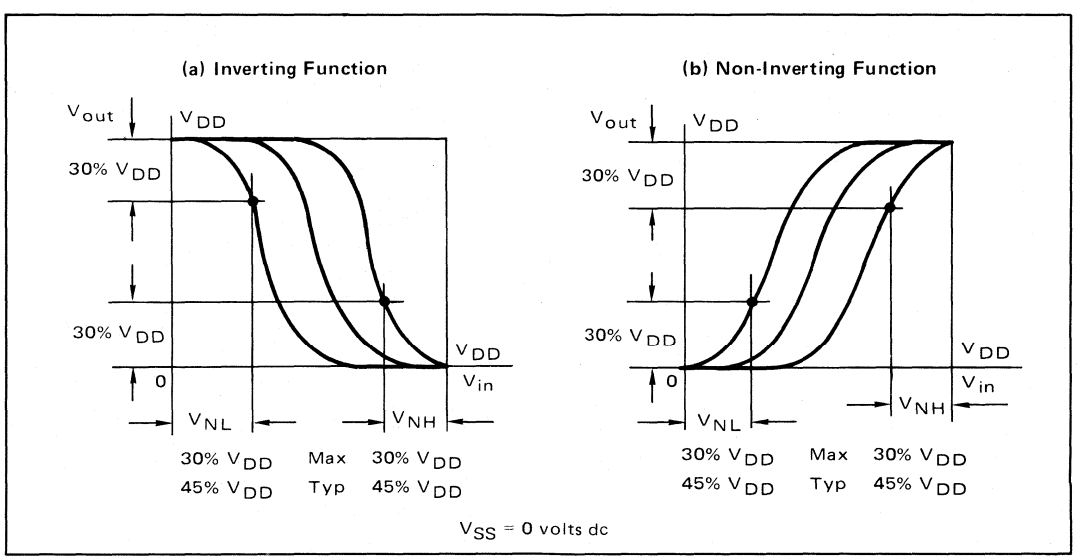


FIGURE 5-13 – TYPICAL McMOS INVERTING AND NON-INVERTING FUNCTIONS

tion times, respectively. These times are specifically measured from the 10% to the 90% points of the waveform. The guaranteed maximum limits are measured with a capacitive load of 15 pF, and are 75 ns for the AL category, and 110 ns for the CL/CP categories at a supply voltage of 10 volts, and 175 ns for the AL category and 200 ns for the CL/CP categories at a supply voltage of 5 volts. Typical values are given for 5, 10, and 15 volts for a capacitive load of 15 pF, and an equation is always given for other capacitive values. Rise and fall times have been found to vary inversely with the average device current; thus, transition times increase with increasing temperature in a manner dictated by the device current.

DISTINCT PART CHARACTERISTICS

Distinct device characteristics deal with parameters which may occur from one data sheet to another. However, in general, parameters have unique values associated with one device or with special parameters that deal only with a specific device. Three general categories are covered: power dissipation, timing parameters, and three-state parameters. It has been the practice to identify and define as many parameters as possible, but a few special ones have been reserved for definition on the individual data sheets involved.

QUIESCENT POWER DISSIPATION (P_Q)

The quiescent dissipation (the circuit contribution with no load on the output) is defined as the product of the steady state current flowing into the V_{DD} supply device pin multiplied by the supply voltage (V_{DD} minus V_{SS}). The supply current is measured under various input combinations to ensure the integrity of all possible reverse-biased junctions (contributing to this current) is maintained. Since the current is a result of a surface-junction phenomenon that is process sensitive, the resulting limits are wider than any other parameter found on any particular data sheet. The current has been found to increase almost linearly with supply voltage until avalanche breakdown occurs and approximately doubles with every 11°C increase in temperature.

TOTAL POWER DISSIPATION (P_D AND $P_T[CL]$)

The total power disipation consists of two components, the dynamic ac contribution due to transient currents flowing through the MOS devices with inputs alternating at specific frequencies and the quiescent dc component previously mentioned. Total power dissipation is defined as the product of the average transient and dc currents flowing into the device V_{DD} supply pin times the supply voltage ($V_{DD} - V_{SS}$). The transient nature of the current occurs since the P-channel and N-channel MOS devices of CMOS are never on simultaneously, except for a brief transition period. During the transition period, the current flowing through the MOS devices are diverted to charge and discharge the internal nodal and external load capacitors of the circuit, rather than flowing directly through the P-channel/N-channel device paths from the V_{DD} to V_{SS} supply pins. It has been previously shown that the total dissipation is given by the formula:

$$P_T(C_L) = (C_{ckt} + C_{loads})\, V_{DD}{}^2 f + P_Q,$$

where: C_{ckt} is the total effective capacitance of the internal circuit, C_{loads} is the total effective external load capacitances, V_{DD} is the supply voltage (V_{SS} = 0 V dc), f is the highest frequency (usually the system clock), and P_Q is the quiescent dissipation.

A McMOS data sheet shows the above equation in two forms. The first, designated P_D, is for the case where all external capacitors have 15 pF values and the supply voltage V_{DD} has specific values (5, 10, and 15 volts). It can be seen by the equation that:

$$P_D = (S\ mW/mHz)\, f + P_Q,$$

where: S is the power frequency slope value for a given supply voltage and represents a lump sum value of both internal circuit and external load (15 pF) capacitances. The second form is given for load capacitances that differ from 15 pF but are equal in value as shown by the equation:

$$P_T(CL) = P_D + N \times 10^{-3}\, (CL - 15\ pF)\, V_{DD}{}^2 f,$$

where: $P_T(CL)$ is the total dissipation with load values of CL, P_D is the first equation for 15 pF values which must be substituted for $P_T(CL)$ at the appropriate supply voltage, and N is a constant that accounts for the number of outputs having loads and the frequency at which the loads toggle. Note that the −15 pF term cancels the 15 pF load contributions given by P_T.

PROPAGATION DELAYS (t_{PLH} AND t_{PHL})

Propogation delay pairs are usually specified on all data sheets. The turn-off (t_{PLH}) and turn-on (t_{PHL}) designations refer to the N-channel MOS device turning OFF and charging the load capacitor from low-to-high, and the N-channel turning ON and discharging the load from high-to-low, respectively. For non-synchronous circuits, the delay is measured from the edge (50% point) of the input signal to the resulting edge (50% point) of the output signal. For synchronous circuits (having a clock signal), the delay is measured from the edge (50% point) of the clock signal associated with the input level to the resulting edge (50% point) of the output signal. The propagation delay limit and typical values are measured with a 15 pF load capacitor. Equations for the typical propagation delays for different capacitive loads are given for supply voltages of 5, 10, and 15 volts. Propagation delays are typically found to increase with increasing temperatures proportional to the rise and fall times.

MINIMUM (CLOCK) PULSE WIDTHS (PW_Lmin AND PW_Hmin)

The minimum pulse widths, as with propagation delays, are usually given as pairs, although they may be defined equal in value. PW_Lmin is that portion of the logical low clock pulse and is the interval measured from the 50% points of one edge to the other edge of that pulse. PW_Hmin is identical with PW_L min with the exception that it applies to that portion of the clock pulse when it is a logical high. It is primarily a measure of how fast information (data or control) signals can be shifted in a synchronous circuit without development of system problems. Pulse widths may also be specified for non-synchronous circuits such as non-clocked RS flip-flops and latches. The maximum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK FREQUENCY (PRFmax)

The maximum clock frequency is the rate at which information can toggle and transfer through a synchronous circuit without developing system problems. Above this frequency, the circuit propagation delays become comparable to the reciprocal of this rate so that informational signals may not be properly entered into the various clocked flip-flops of the circuit. The reciprocal of the sum of the low and high minimum pulse widths equals this rate [PRFmax = 1/ (PW_Lmin + PW_Hmin)]. Thus, only two of the three parameters are usually specified. The minimum limit is specified for this parameter on the individual data sheet.

MINIMUM CLOCK FREQUENCY (PRFmin)

The minimum clock frequency is specified on dynamic (i.e., non-static) synchronous circuits where information is held in part or entirely on the capacitors of the circuit. Below this frequency, the information will be dissipated and lost by leakages in the circuit. The reciprocal of the sum of the low and high maximum pulse widths equals this rate [PRFmin = 1/ (PW_Lmax + PW_Hmax)]. The maximum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK PULSE WIDTHS (PW_Lmax AND PW_Hmax)

PW_Lmax is the low portion of the clock pulse and is the interval measured from the 50% points of one pulse edge to the other. PW_Hmax is identical to PW_Lmax with the exception that it applies to the high portion of the clock pulse. Below those maximum pulse widths, the information stored on the circuit holding capacitors will be lost. The minimum limit is specified for this parameter on the individual data sheet.

MAXIMUM CLOCK PULSE RISE AND FALL TIMES ($t_r$max AND $t_f$max)

Transition times refer to the rise and fall times of the signal waveshapes applied to the inputs (usually the clock input). Above their guaranteed minimum limits, the rise and fall time transitions are so slow that data states in the synchronous circuit may interact with states in previous flip-flop stages rather than toggle to the proper next state.

MINIMUM SETUP TIME (t_{setup})

Setup time is the minimum time required between the information (data or control) signal edge and the clock (or strobe) signal edge to guarantee that information will be validly entered or acted upon by the first rank of flip-flop stage(s). The time is measured between the 50% points of the edges stated. The maximum limit is specified on the individual data sheet.

MINIMUM HOLD TIME (t_{hold})

Hold time is the minimum time required between the information signal edge and the clock (or strobe) signal edge to guarantee that invalid information will not be entered or acted upon while valid information is held in the first rank of flip-flop stage(s). The time is measured between the 50% points of the edges described. The maximum limit is specified on the individual data sheet.

RELEASE TIME (t_{rel})

See Minimum Setup Time.

REMOVAL TIME (t_{rem})

See Minimum Setup Time.

ACCESS TIME (t_{acc})

A term used in memories (RAMs or ROMs) and analogous to the definition of propagation delay where the information input is the address information. Once this propagation delay occurs, data may be validly written into or read out of a memory location.

CYCLE TIME (t_{cyc})

A term used in memories and includes the access time, the data transfer time to another system location, and if needed, the time required to refresh any data within a dynamic memory. The term is analogous to the reciprocal of the maximum clock frequency parameter.

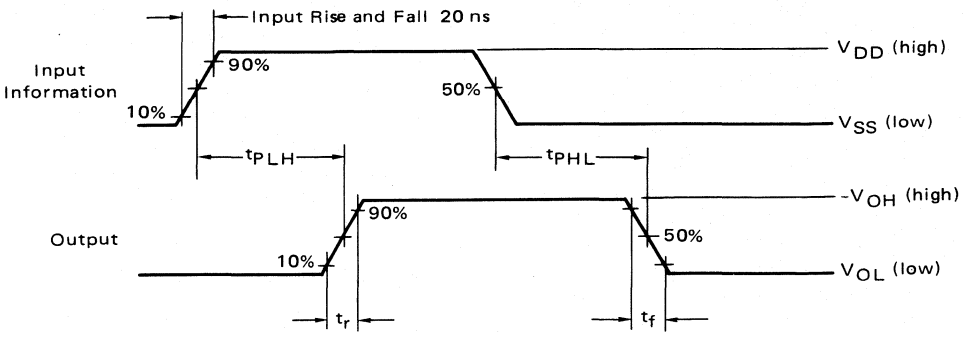
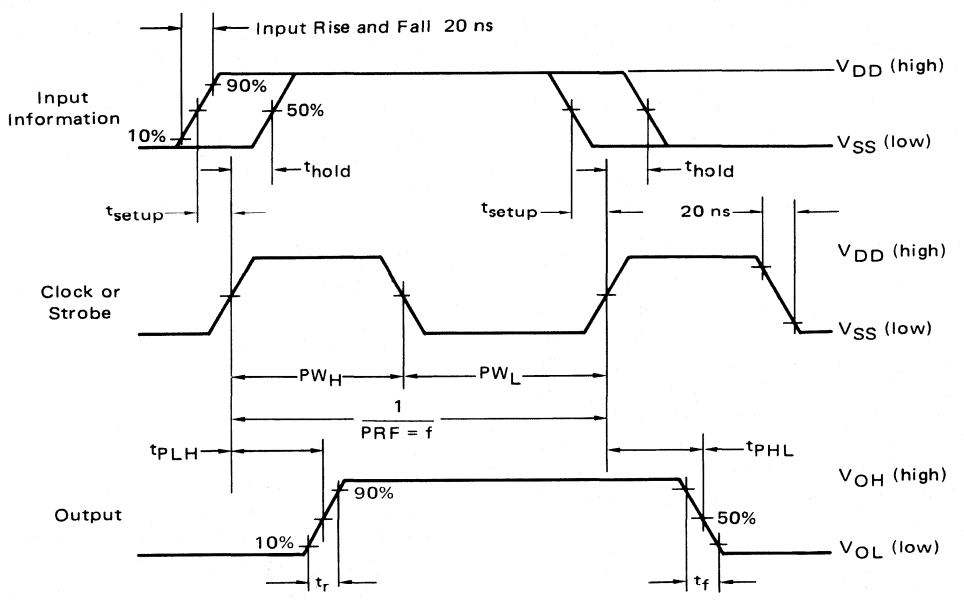


FIGURE 5-14 – NON-SYNCHRONOUS CIRCUIT WAVESHAPES AND TIMING PARAMETERS



Note: Information is accepted during each positive clock signal transition in this case.

FIGURE 5-15 – SYNCHRONOUS CIRCUIT WAVESHAPES AND TIMING PARAMETERS

THREE-STATE PARAMETERS

The three-state output capability on an integrated circuit provides that device with the added flexibility of being connected to systems having common input/output busses. When the component is not enabled to send information, the output structure becomes a high impedance or a third logical state which does not overload the bus lines. When it is enabled, the inputs exhibit regular McMOS family output characteristics.

THREE-STATE PROPAGATION DELAYS ($t_{"0"H}$, $t_{H"0"}$, $t_{"1"H}$, AND $t_{H"1"}$)

The $t_{"0"H}$ and $t_{H"0"}$ (designating low to three-state, and three-state to low output transition edges) propagation delays are measured from the 50% points of the disable signal to the 10% points of the rising edge and the 90% point of the falling edge of the output, respectively. The output for this case is loaded with a 15 pF capacitor connected to V_{SS} and a 1 k ohm resistor connected in series with V_{DD}. The $t_{"1"H}$ and $t_{H"1}$ (designating high to three-state, and three-state to high output transition edges) propagation delays are measured from the 50% points of the disable signal to the 90% point of the falling edge and the 10% point of the rising edge, respectively. The output for this case is loaded with a 15 pF capacitor connected to V_{SS}, and a 1 k ohm resistor connected in series with V_{SS}. Figure 5-16 illustrates typical three-state propagation delay waveshapes and a corresponding circuit.

THREE-STATE LEAKAGES (I_{TL})

Leakage currents at the output pin with the three-state activation is measured under two worst case conditions. The first condition is with a voltage of V_{DD} applied to the output and with input combinations applied to the circuit that would normally force the output low. The second condition is with a voltage of V_{SS} applied to the output and the input combinations applied to the circuit that would normally force the output high. Both conditions are performed under V_{DD} supply voltages of 5 and 10 volts.

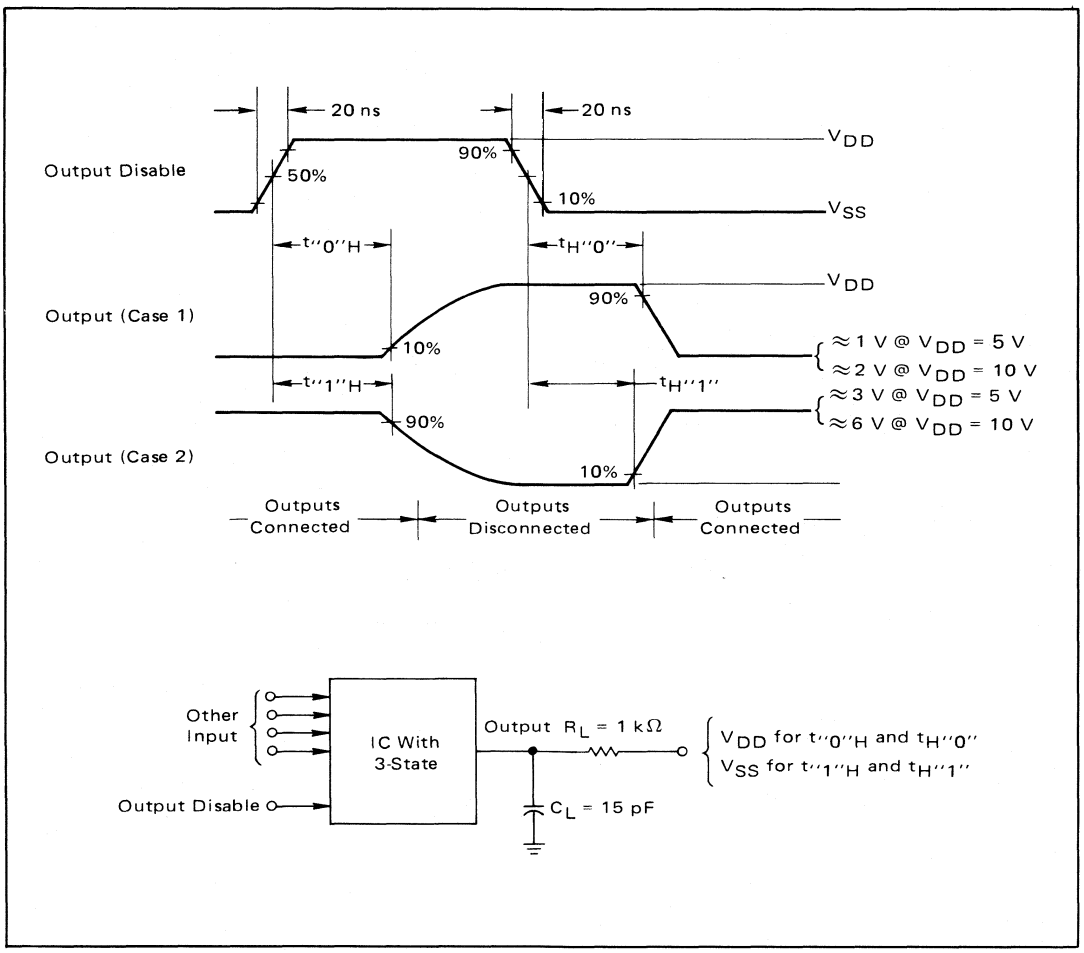
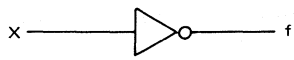
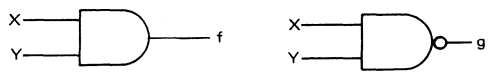
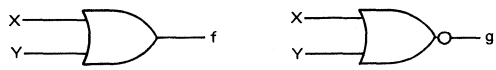
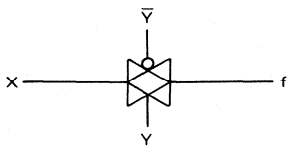


FIGURE 5-16 – THREE-STATE PROPAGATION DELAY WAVESHAPE AND CIRCUIT

LOGIC SYMBOLS AND CONVENTIONS

The block and logic diagrams presented in the McMOS data sheets are logic symbols and conventions based upon the military standard logic specification MIL-STD-806(c). Table 5-4 lists and illustrates the McMOS logic functions, symbols, and their truth tables. In addition, Table 5-4 also contains a logic element which is particular to CMOS technology called the transmission gate. This symbol is not defined in MIL-STD-806(c) and was derived from the military amplifier symbol placed back-to-back to indicate the bidirectional and non-inverting gate nature. The transmission gate is analogous to a single-pole, single-throw switch which is electrically controlled by two control lines. The circle on the upper control line indicates the gate of the P-channel MOS device, and the lower control line indicates the gate of the N-channel MOS device. The horizontal transmission lines are connected to the drains and sources of those two MOS devices.

TABLE 5-4 – McMOS LOGIC FUNCTION, SYMBOLS AND TRUTH TABLES

Logic Function	Logic Symbols	Truth Tables
Inverter		X | f 0 | 1 1 | 0
AND and NAND Gates		Y X | f 0 0 | 0 0 1 | 0 1 0 | 0 1 1 | 1 Y X | f 0 0 | 1 0 1 | 1 1 0 | 1 1 1 | 0
OR and NOR Gates		Y X | f 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 1 Y X | g 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 0
Exclusive OR and NOR Gates		Y X | f 0 0 | 0 0 1 | 1 1 0 | 1 1 1 | 0 Y X | g 0 0 | 1 0 1 | 0 1 0 | 0 1 1 | 1
D Flip-Flops (Clocked Delay)		C D | Q 0 0 | 0 1 1 | 1 X Y C̄ D | Q 0 0 | 0 1 1 | 1 X Y X = Don't Care Y = No Change
Transmission Gate		Y X | f 0 0 | Z } Bidirectional Open 0 1 | Z 1 0 | 0 } Bidirectional Short 1 1 | 1 Z = Three-State

McMOS
INTEGRATED CIRCUITS

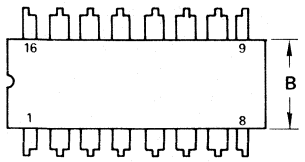
Chapter 6

MECHANICAL DATA

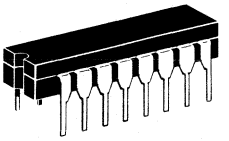
MECHANICAL DATA

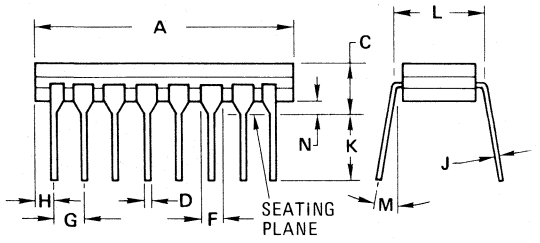
The packaging availability for each device is indicated on the individual data sheets and on the Selector Guide. Dimensions for the packages are given in this section. Pin assignment drawings are also included for convenient reference.

L SUFFIX
CERAMIC PACKAGE
CASE 620



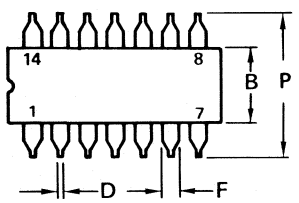
NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSTIION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.

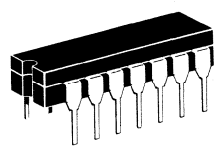


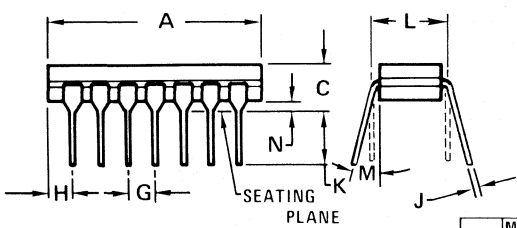


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

L SUFFIX
CERAMIC PACKAGE
CASE 632







NOTES:
1. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL. (632-02).
2. DIM "A" AND "B" (632-04) DO NOT INCLUDE GLASS RUN-OUT.
3. DIM "L" TO INSIDE OF LEADS (MEASURED 0.51 mm (0.020) BELOW BODY) (632-04)

Devices packaged in Case 632 fall within one of the given sets of dimensions. Further identification is available upon request.

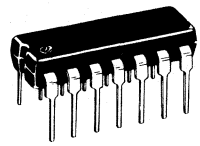
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

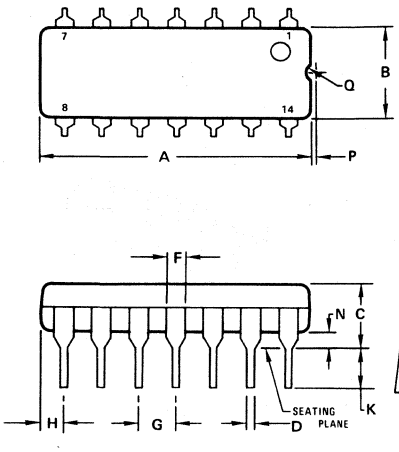
CASE 632-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.10	7.49	0.240	0.295
C	–	5.08	–	0.200
D	0.38	0.58	0.015	0.023
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	1.91	2.29	0.075	0.090
J	0.20	0.38	0.008	0.015
K	2.54	–	0.100	–
L	7.49	8.89	0.295	0.350
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 632-04

P SUFFIX
PLASTIC PACKAGE
CASE 646

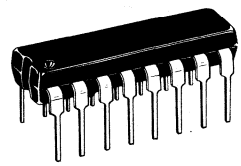


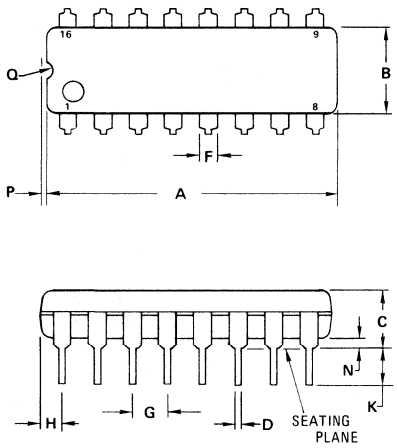


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

P SUFFIX
PLASTIC PACKAGE
CASE 648

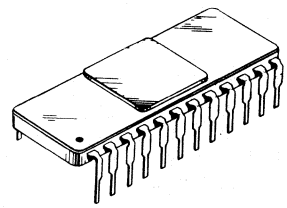


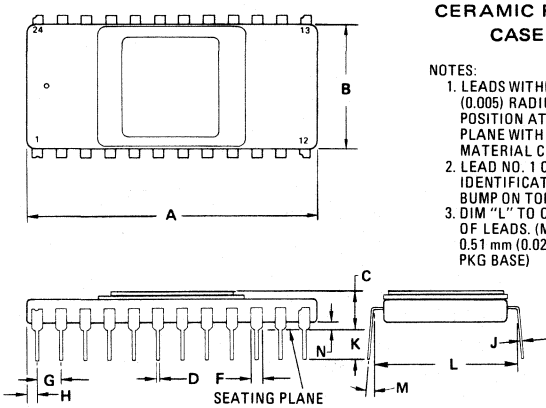


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

L SUFFIX
CERAMIC PACKAGE
CASE 684



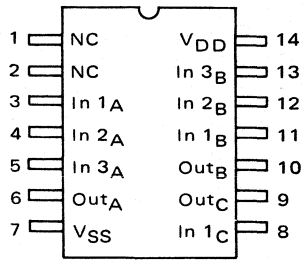


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO CENTER OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

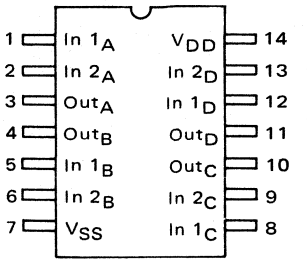
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	29.34	30.86	1.155	1.215
B	12.70	14.22	0.500	0.560
C	3.05	3.94	0.120	0.155
D	0.38	0.51	0.015	0.020
F	0.89	1.40	0.035	0.055
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	2.92	3.68	0.115	0.145
L	14.86	15.62	0.585	0.615
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

PIN ASSIGNMENTS

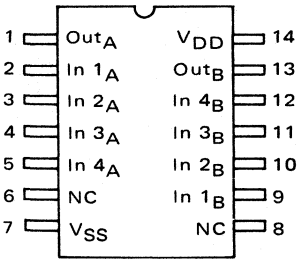
MC14000
Dual 3-Input NOR Gate Plus Inverter



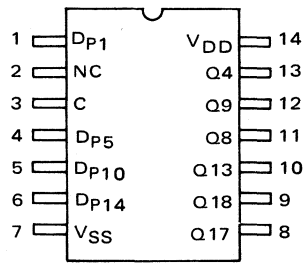
MC14001
Quad 2-Input NOR Gate



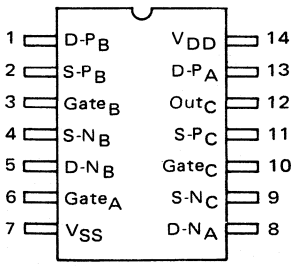
MC14002
Dual 4-Input NOR Gate



MC14006
18-Bit Static Shift Register

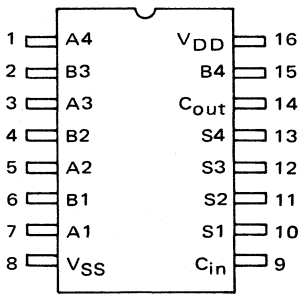


MC14007
Dual Complementary Pair Plus Inverter

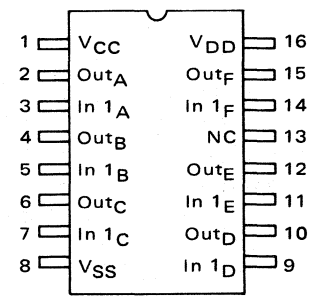


D = Drain
S = Source

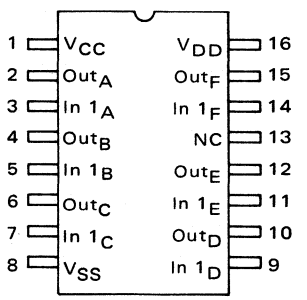
MC14008
4-Bit Full Adder



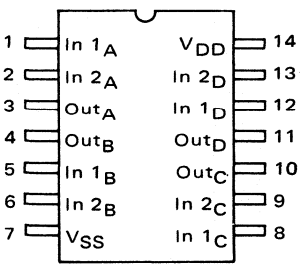
MC14009
Hex Inverter/Buffer



MC14010
Hex Buffer



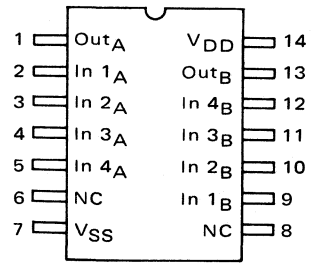
MC14011
Quad 2-Input NAND Gate



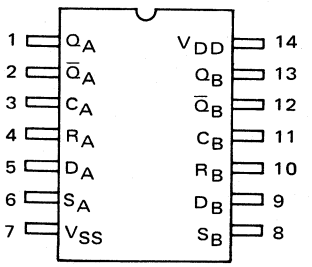
NC = No Connection

PIN ASSIGNMENTS (continued)

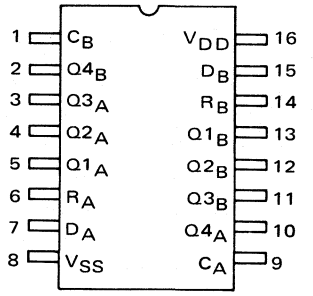
MC14012
Dual 4-Input NAND Gate



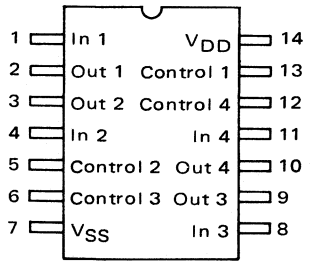
MC14013
Dual Type D Flip-Flop



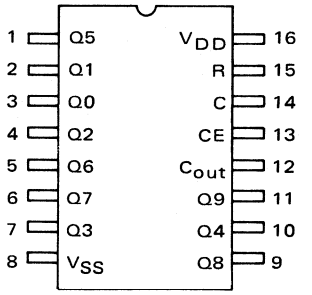
MC14015
Dual 4-Bit Static Shift Register



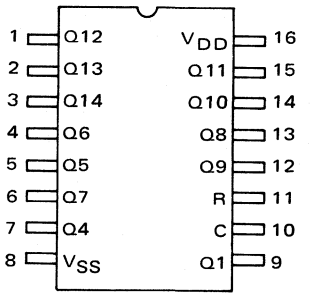
MC14016
Quad Analog Switch/Quad Multiplexer



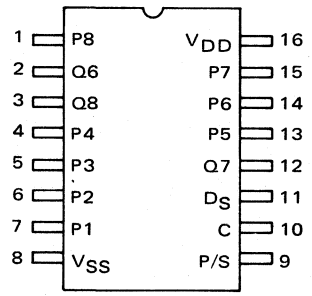
MC14017
Decade Counter/Divider



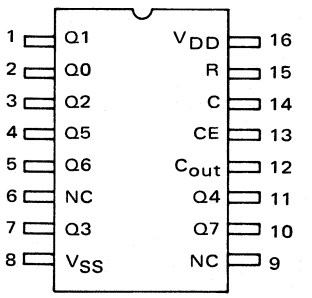
MC14020
14-Bit Binary Counter



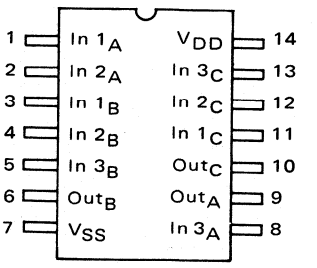
MC14021
8-Bit Static Shift Register



MC14022
Octal Counter/Divider



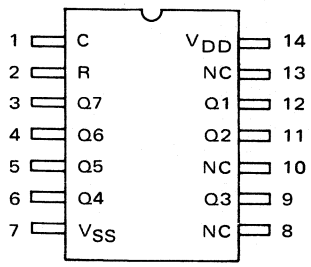
MC14023
Triple 3-Input NAND Gate



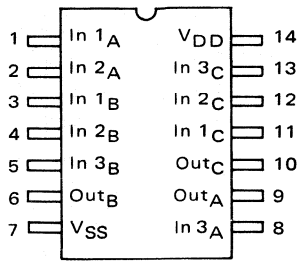
NC = No Connection

PIN ASSIGNMENTS (continued)

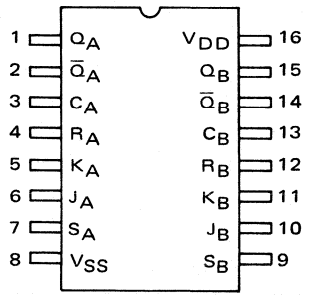
MC14024
Seven-Stage Ripple Counter



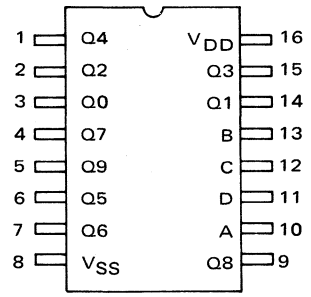
MC14025
Triple 3-Input NOR Gate



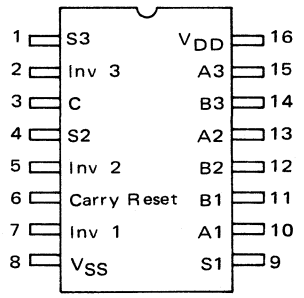
MC14027
Dual J-K Flip-Flop



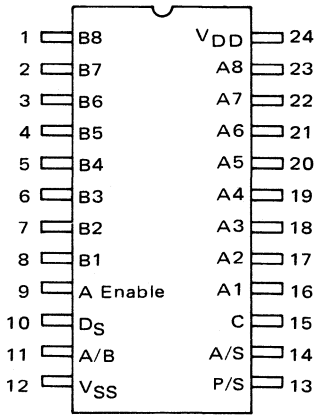
MC14028
BCD-To-Decimal Decoder/
Binary-To-Octal Decoder



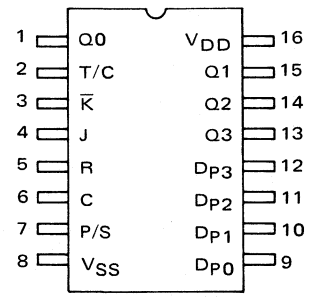
MC14032
Triple Serial Adder
(Positive Logic)



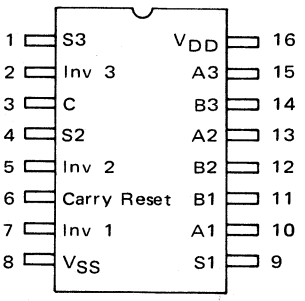
MC14034
8-Bit Universal Bus Register



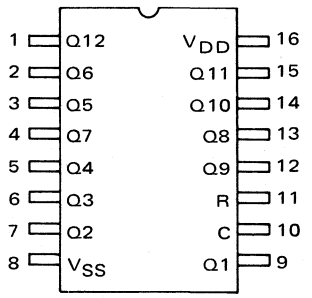
MC14035
4-Bit Parallel-In/Parallel Out
Shift Register



MC14038
Triple Serial Adder
(Negative Logic)



MC14040
12-Bit Binary Counter

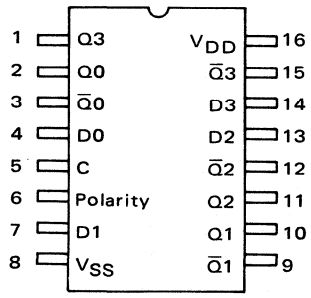


NC = No Connection

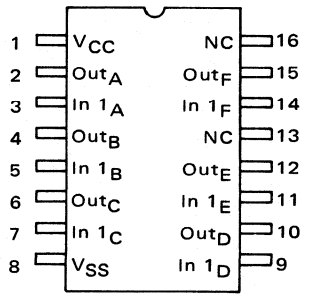
6

PIN ASSIGNMENTS (continued)

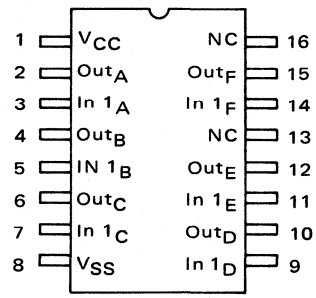
MC14042
Quad Latch



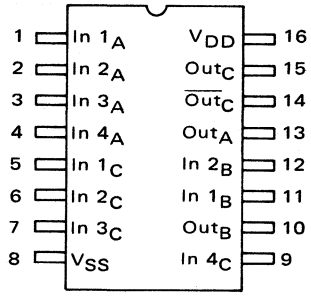
MC14049
Hex Inverter/Buffer



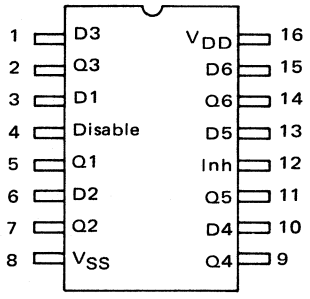
MC14050
Hex Buffer



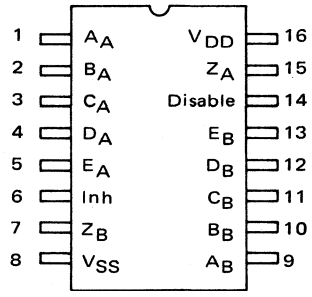
MC14501
Triple Gate



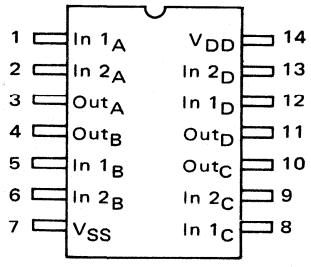
MC14502
Strobed Hex Inverter/Buffer



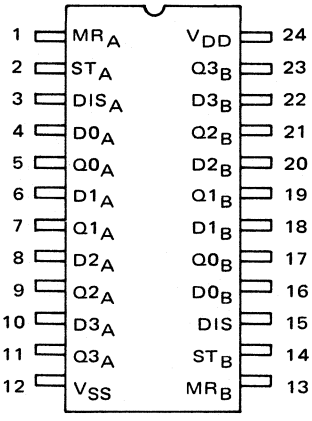
MC14506
Dual Expandable AND-OR-INVERT Gate



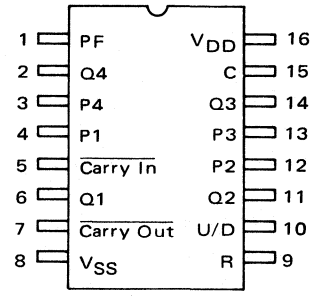
MC14507
Quad Exclusive OR Gate



MC14508
Dual 4-Bit Latch



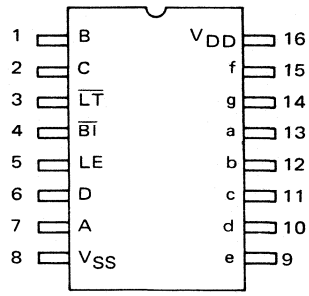
MC14510
BCD Up/Down Counter



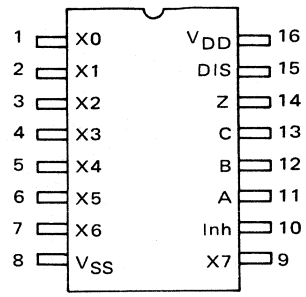
NC = No Connection

PIN ASSIGNMENTS (continued)

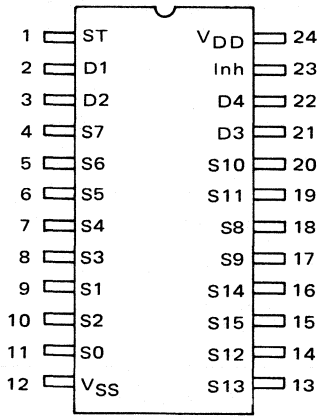
MC14511
BCD-To-Seven Segment Latch/Decoder/Driver



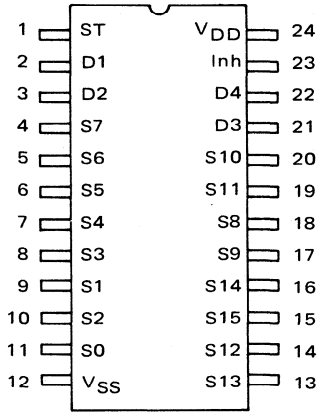
MC14512
8-Channel Data Selector



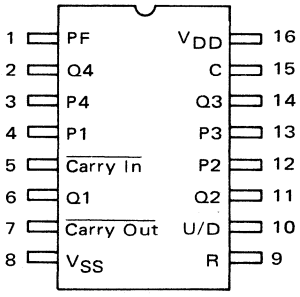
MC14514
4-Bit Latch/4-To-16 Line Decoder



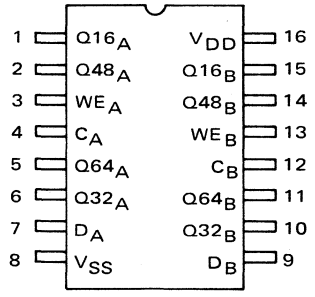
MC14515
4-Bit Latch/4-To-16 Line Decoder



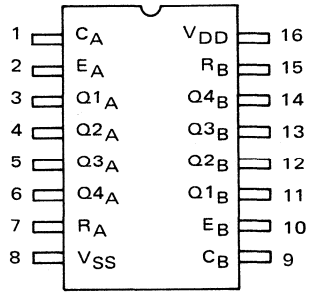
MC14516
Binary Up/Down Counter



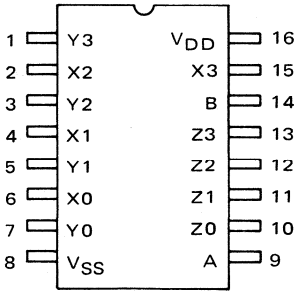
MC14517
Dual 64-Bit Static Shift Register



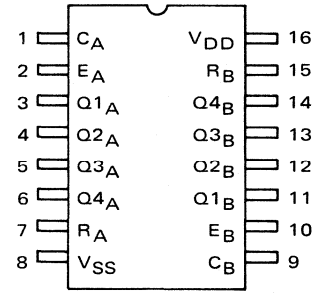
MC14518
Dual BCD Up Counter



MC14519
4-Bit AND/OR Selector



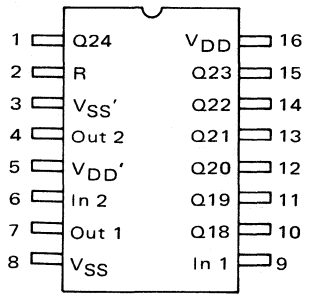
MC14520
Dual Binary Up Counter



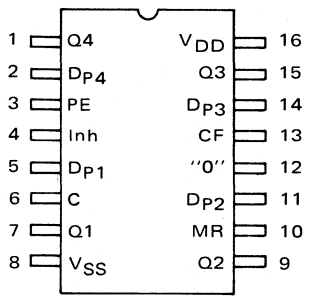
NC = No Connection

PIN ASSIGNMENTS (continued)

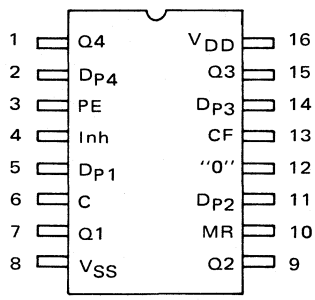
MC14521
24-Stage Frequency Divider



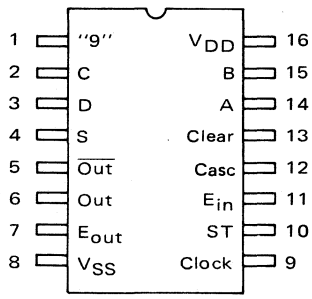
MC14522
Programmable Divide-By-N-4-Bit BCD Counter



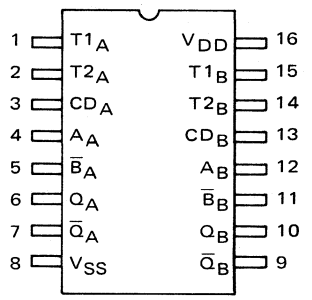
MC14526
Programmable Divide-By-N-4-Bit Binary Counter



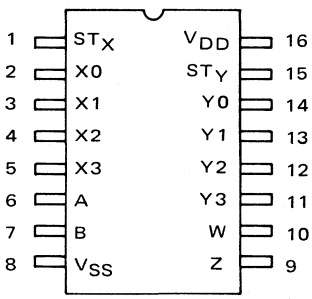
MC14527
BCD Rate Multiplier



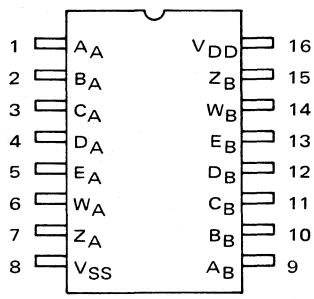
MC14528
Dual Retriggerable/Resettable Monostable Multivibrator



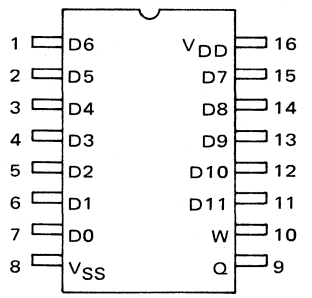
MC14529
Dual 4-Channel Analog Data Selector



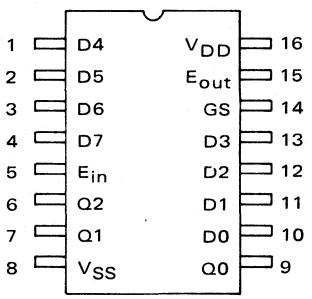
MC14530
Dual 5-Input Majority Logic Gate



MC14531
12-Bit Parity Tree



MC14532
8-Bit Priority Encoder

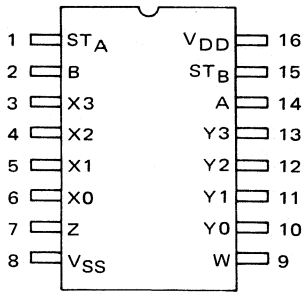


NC = No Connection

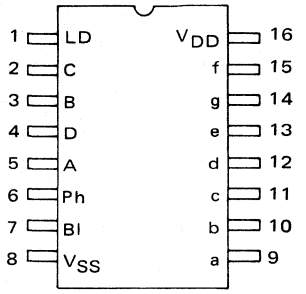
6

PIN ASSIGNMENTS (continued)

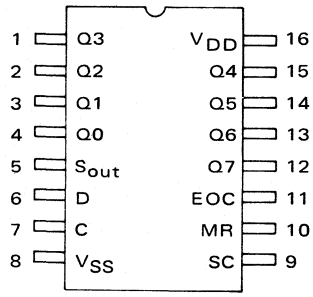
MC14539
Dual 4-Channel Data Selector/Multiplexer



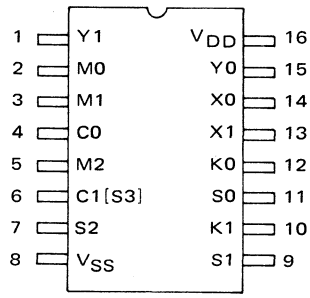
MC14543
BCD-To-Seven Segment Latch/ Decoder/Driver



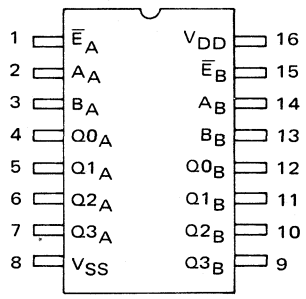
MC14549
Successive Approximation Register



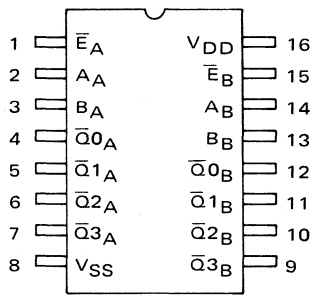
MC14554
2 x 2-Bit Parallel Binary Multiplier



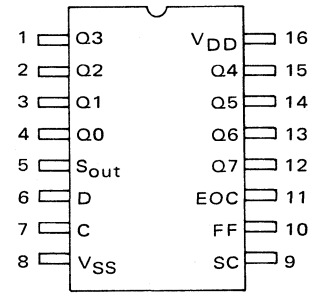
MC14555
Dual Binary to 1-of-4 Decoder/ Demultiplexer



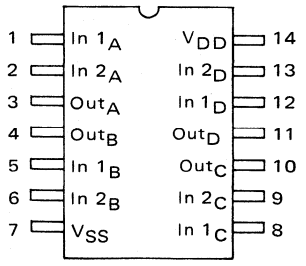
MC14556
Dual Binary to 1-of-4 Decoder/ Demultiplexer



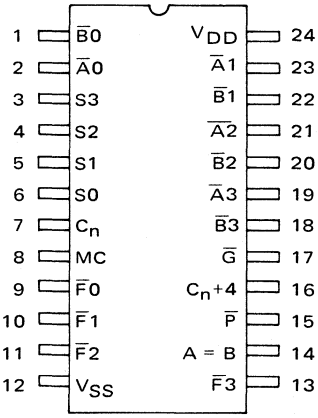
MC14559
Successive Approximation Register



MC14570
Quad 2-Input OR Gate



MC14581
4-Bit Arithmetic Logic Unit

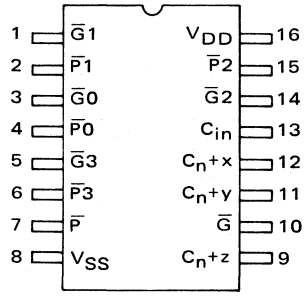


NC = No Connection

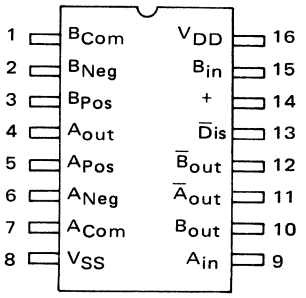
6

PIN ASSIGNMENTS (continued)

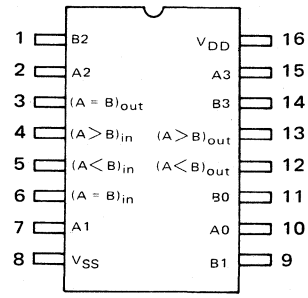
MC14582
Look-Ahead Carry Block



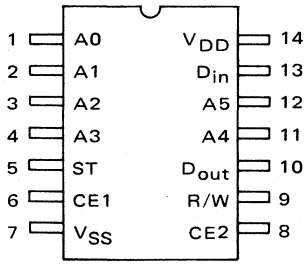
MC14583
Dual Schmitt Trigger



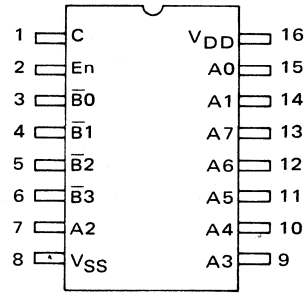
MC14585
4-Bit Magnitude Comparator



MCM14505
64-Bit Random Access
Read Write Memory



MCM14524
1024-Bit Read Only Memory



NC = No Connection

McMOS

INTEGRATED CIRCUITS

Chapter 7
DATA SHEETS

MC14000AL
MC14000CL
MC14000CP

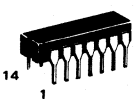
DUAL 3-INPUT "NOR" GATE PLUS INVERTER

The MC14000 dual 3-input NOR gate plus inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

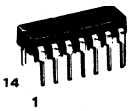
- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14000AL)
  = 3.0 Vdc to 16 Vdc (MC14000CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 750 ohms typical
- Pin-for-Pin Replacement for CD4000A

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL 3-INPUT "NOR" GATE PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

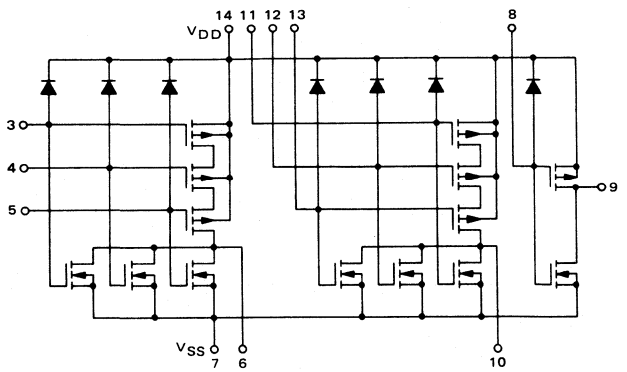
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14000AL – MC14000CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14000AL – MC14000CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

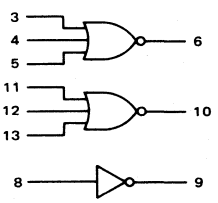
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
(Positive Logic)



$6 = 3+4+5$
$9 = \overline{8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14000AL -55°C Min	MC14000AL -55°C Max	MC14000AL +25°C Min	MC14000AL +25°C Typ	MC14000AL +25°C Max	MC14000AL +125°C Min	MC14000AL +125°C Max	MC14000CL/CP -40°C Min	MC14000CL/CP -40°C Max	MC14000CL/CP +25°C Min	MC14000CL/CP +25°C Typ	MC14000CL/CP +25°C Max	MC14000CL/CP +85°C Min	MC14000CL/CP +85°C Max	Unit
Output Voltage	"0" Level	1,2,3	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																			
($V_{out} \geq 3.5$ Vdc)		–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																			
(V_{OH} = 2.5 Vdc)	Source	4	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)				10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	5	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)				10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		7,8	P_D	5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	μW
(C_L = 50 pF)				10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
				15	–	–	–	0.05	–	–	–	–	–	–	0.25	–	–	–	
Output Rise Time**		6	t_r																ns
(C_L = 15 pF), t_r = (2.5 ns/pF) C_L + 62 ns				5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**		6	t_f																ns
(C_L = 15 pF) t_f = (2.0 ns/pF) C_L + 70 ns				5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_f = (1.0 ns/pF) C_L + 20 ns				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.9 ns/pF) C_L + 11 ns				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On Delay Time**		6	t_{PHL}																ns
(C_L = 15 pF) t_{PHL} = (1.0 ns/pF) C_L + 45 ns				5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
t_{PHL} = (0.5 ns/pF) C_L + 16 ns				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
t_{PHL} = (0.4 ns/pF) C_L + 12 ns				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	
Turn-Off Delay Time**		6	t_{PLH}																ns
(C_L = 15 pF) t_{PLH} = (1.0 ns/pF) C_L + 45 ns				5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
t_{PLH} = (0.5 ns/pF) C_L + 16 ns				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
t_{PLH} = (0.4 ns/pF) C_L + 12 ns				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

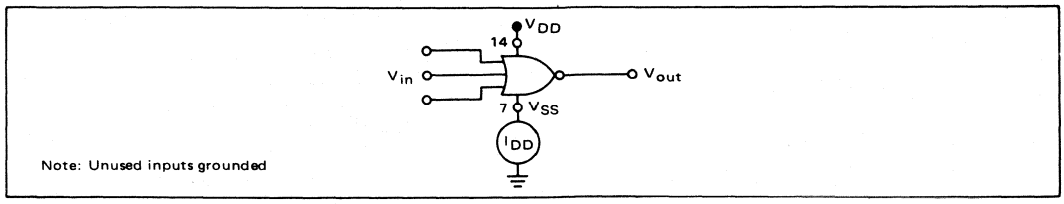


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

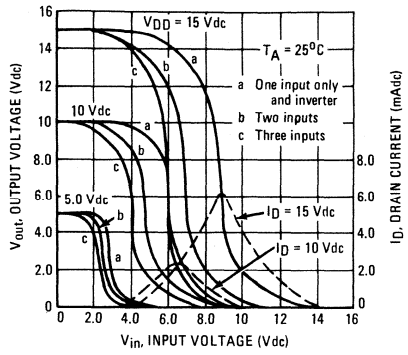


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

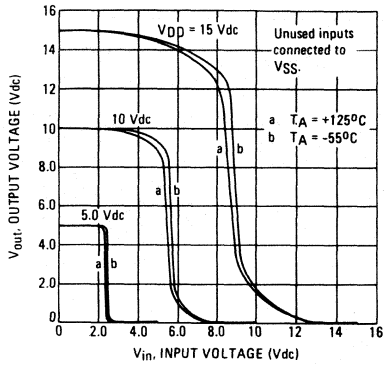


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

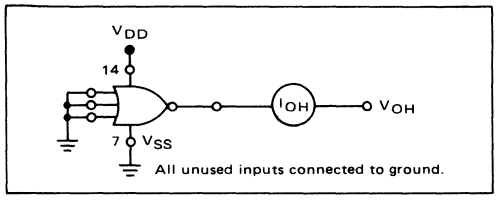


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

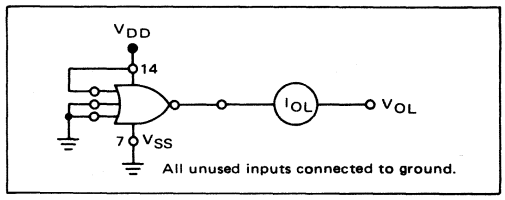


FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

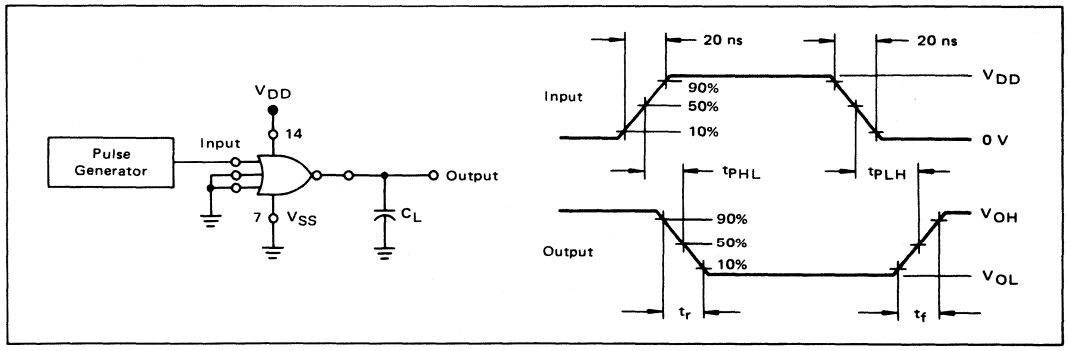


FIGURE 7 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

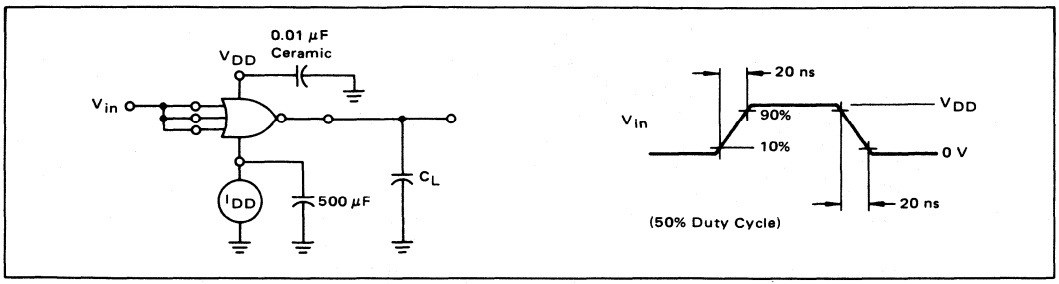
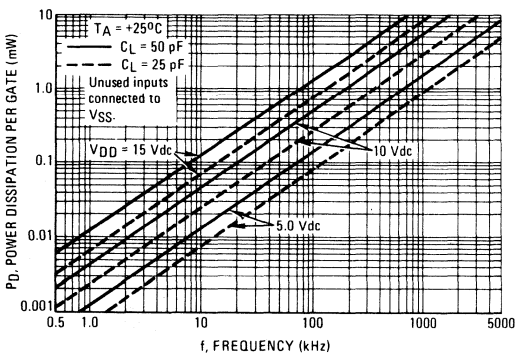


FIGURE 8 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS



NOTE: All unused inputs should be returned to V_{DD} or V_{SS} as appropriate for circuit application.

7

MC14001AL
MC14001CL
MC14001CP

QUAD 2-INPUT "NOR" GATE

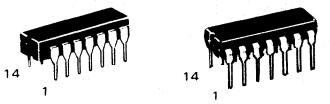
The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhnacement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14001AL)
  = 3.0 Vdc to 16 Vdc (MC14001CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

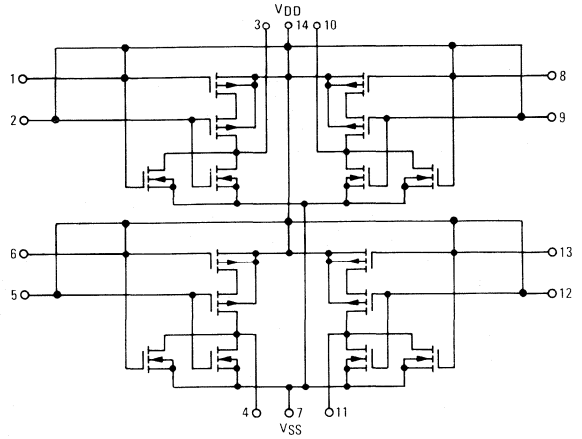
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14001AL MC14001CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14001AL —MC14001CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

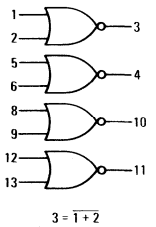
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1 + 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14001AL -55°C Min	MC14001AL -55°C Max	MC14001AL +25°C Min	MC14001AL +25°C Typ	MC14001AL +25°C Max	MC14001AL +125°C Min	MC14001AL +125°C Max	MC14001CL/CP -40°C Min	MC14001CL/CP -40°C Max	MC14001CL/CP +25°C Min	MC14001CL/CP +25°C Typ	MC14001CL/CP +25°C Max	MC14001CL/CP +85°C Min	MC14001CL/CP +85°C Max	Unit
Output Voltage "0" Level	1,2,3	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation ** Per Package	4	P_Q																mW
			5.0	–	0.00025	–	0.000025	0.00025	–	0.015	–	0.0025	–	0.000025	0.0025	–	0.075	
			10	–	0.001	–	0.0001	0.001	–	0.060	–	0.01	–	0.0001	0.01	–	0.30	
			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Total Power Dissipation (Dynamic Plus Quiescent) (C_L = 15 pF) Per Package	4	P_D																mW
			5.0	$P_D = (2.0\ mW/MHz)\ f + 0.000025\ mW$														
			10	$P_D = (8.0\ mW/MHz)\ f + 0.00010\ mW$														
			15	$P_D = (18\ mW/MHz)\ f + 0.00023\ mW$														
Output Rise Time** (C_L = 15 pF)	5	t_r																ns
$t_r = (3.0\ ns/pF)\ C_L + 25\ ns$			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
$t_r = (1.5\ ns/pF)\ C_L + 12\ ns$			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
$t_r = (1.1\ ns/pF)\ C_L + 8.0\ ns$			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time** (C_L = 15 pF)	5	t_f																ns
$t_f = (1.5\ ns/pF)\ C_L + 47\ ns$			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
$t_f = (0.75\ ns/pF)\ C_L + 24\ ns$			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
$t_f = (0.55\ ns/pF)\ C_L + 17\ ns$			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off, Turn-On Delay Time (C_L = 15 pF)	5	t_{PLH}, t_{PHL}																ns
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 33\ ns$			5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
$t_{PLH}, t_{PHL} = (0.73\ ns/pF)\ C_L + 14\ ns$			10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
$t_{PLH}, t_{PHL} = (0.60\ ns/pF)\ C_L + 10\ ns$			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refer to corresponding formula: $P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}^2 f$

Where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

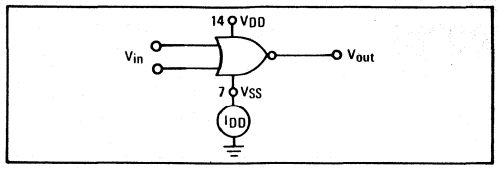


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

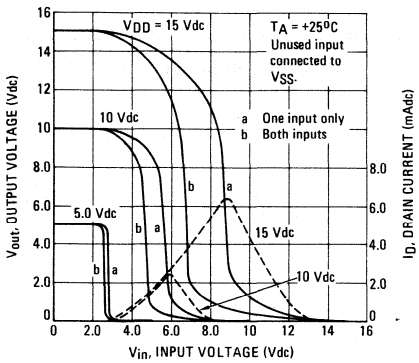


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

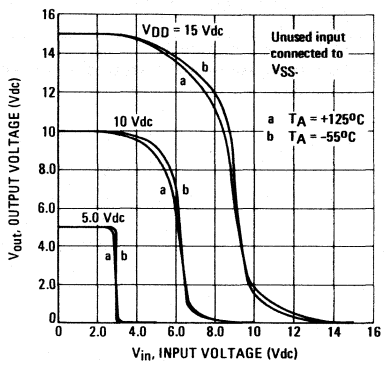


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

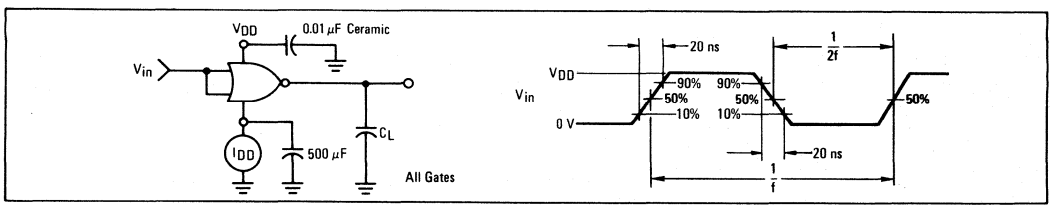
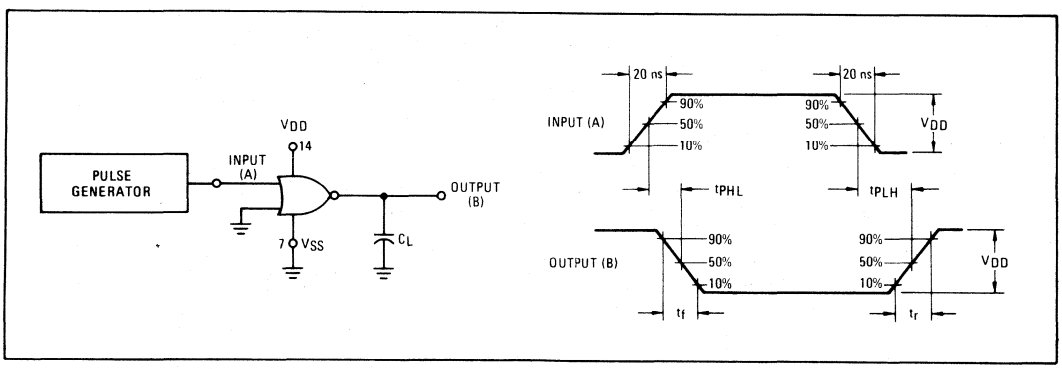


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14002AL
MC14002CL
MC14002CP

DUAL 4-INPUT "NOR" GATE

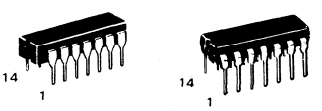
The MC14002 dual 4-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14002AL)
  = 3.0 Vdc to 16 Vdc (MC14002CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4002A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

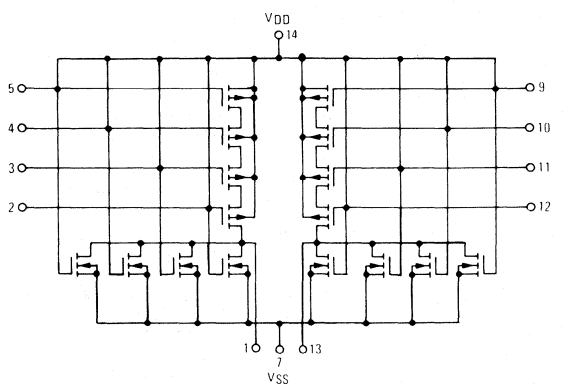
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14002AL	V_{DD}	+18 to -0.5	Vdc
	– MC14002CL/CP		+16 to -0.5	
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14002AL	T_A	-55 to +125	°C
	– MC14002CL/CP		-40 to +85	
Storage Temperature Range		T_{stg}	-65 to +150	°C

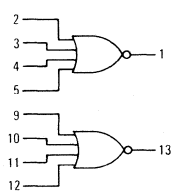
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$1 = \overline{2+3+4+5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14002AL -55°C Min	MC14002AL -55°C Max	MC14002AL +25°C Min	MC14002AL +25°C Typ	MC14002AL +25°C Max	MC14002AL +125°C Min	MC14002AL +125°C Max	MC14002CL/CP -40°C Min	MC14002CL/CP -40°C Max	MC14002CL/CP +25°C Min	MC14002CL/CP +25°C Typ	MC14002CL/CP +25°C Max	MC14002CL/CP +85°C Min	MC14002CL/CP +85°C Max	Unit
Output Voltage "0" Level	1,2,3	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	1.7	–	0.35	–	0.23	–	0.20	1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
		I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation **	4	P_Q																mW
(C_L = 15 pF, f = 0 Hz)																		
			5.0	–	0.00025	–	0.000025	0.00025	–	0.015	–	0.0025	–	0.000025	0.0025	–	0.075	
			10	–	0.001	–	0.0001	0.001	–	0.060	–	0.01	–	0.0001	0.01	–	0.30	
Per Package			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Total Power Dissipation (Dynamic Plus Quiescent) (C_L = 15 pF)	4	P_D																mW
			5.0	$P_D = (1.0\ mW/MHz)\ f + 0.000025\ mW$														
			10	$P_D = (4.0\ mW/MHz)\ f + 0.0001\ mW$														
Per Package			15	$P_D = (9.0\ mW/MHz)\ f + 0.00023\ mW$														
Output Rise Time**	5	t_r																ns
(C_L = 15 pF)																		
$t_r = (3.0\ ns/pF)\ C_L + 25\ ns$			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
$t_r = (1.5\ ns/pF)\ C_L + 12\ ns$			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
$t_r = (1.1\ ns/pF)\ C_L + 8.0\ ns$			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	5	t_f																ns
(C_L = 15 pF)																		
$t_f = (1.5\ ns/pF)\ C_L + 47\ ns$			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
$t_f = (0.75\ ns/pF)\ C_L + 24\ ns$			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
$t_f = (0.55\ ns/pF)\ C_L + 17\ ns$			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off, Turn-On Delay Time	5	t_{PLH}, t_{PHL}																ns
(C_L = 15 pF)																		
$t_{PLH}, t_{PHL} = (1.8\ ns/pF)\ C_L + 33\ ns$			5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
$t_{PLH}, t_{PHL} = (0.73\ ns/pF)\ C_L + 14\ ns$			10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
$t_{PLH}, t_{PHL} = (0.60\ ns/pF)\ C_L + 10\ ns$			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refere to corresponding formula:

$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc and f in MHz

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

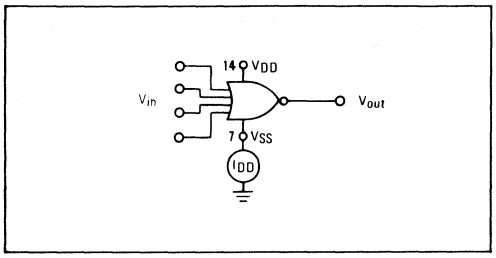


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

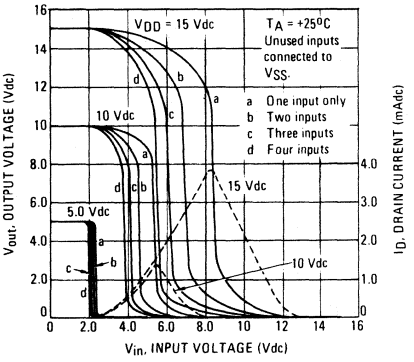
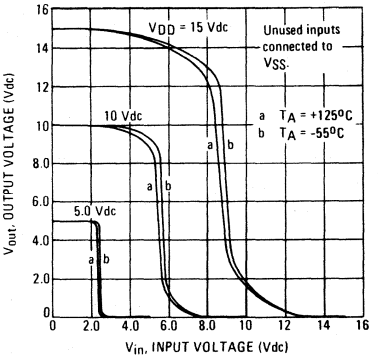


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



7

FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

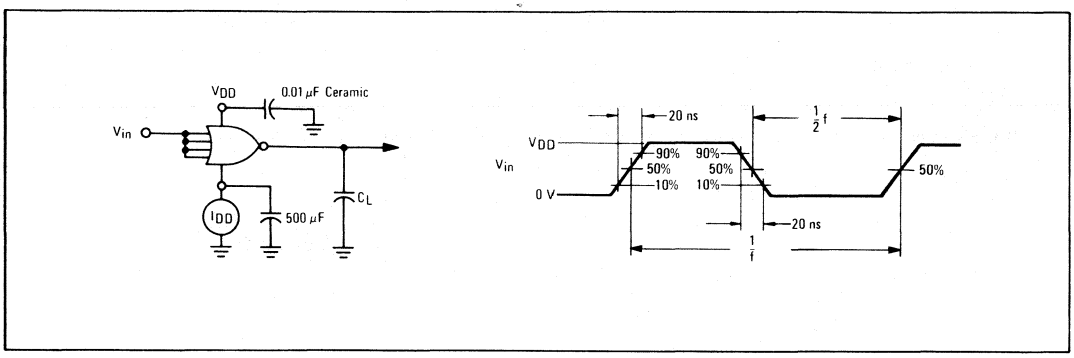
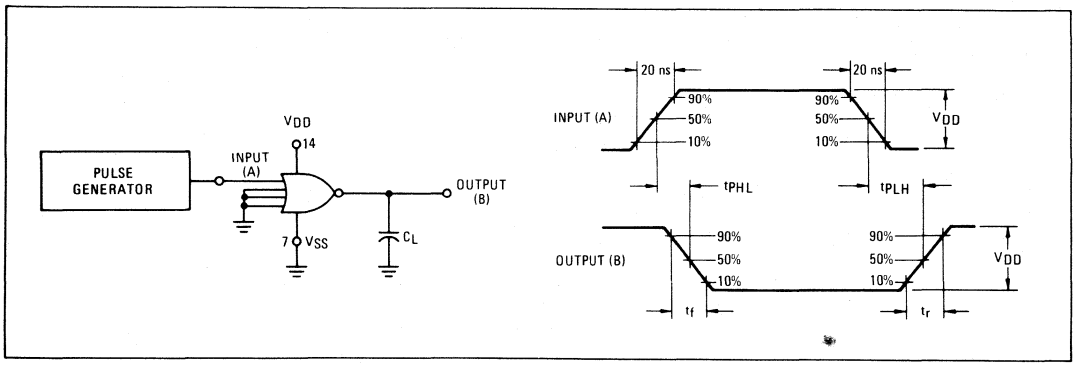


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14006AL
MC14006CL
MC14006CP

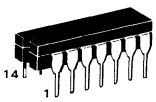
18-BIT STATIC SHIFT REGISTER

The MC14006 shift register is comprised of four separate shift register sections sharing a common clock: two sections have four stages, and two sections have five stages with an output tap on both the fourth and fifth stages. This makes it possible to obtain a shift register of 4, 5, 8, 9, 10, 12, 13, 14, 16, 17, or 18 bits by appropriate selection of inputs and outputs. This part is particularly useful in serial shift registers and time delay circuits.

- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Quiescent Power Dissipation = 0.05 μW/package typical
- Fully Static Operation
- 8-MHz Shift Rate typical
- Can be Cascaded to Provide Longer Shift Register Lengths
- Pin-for-Pin Replacement for CD4006A

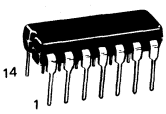
McMOS
(LOW-POWER COMPLEMENTARY MOS)

18-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

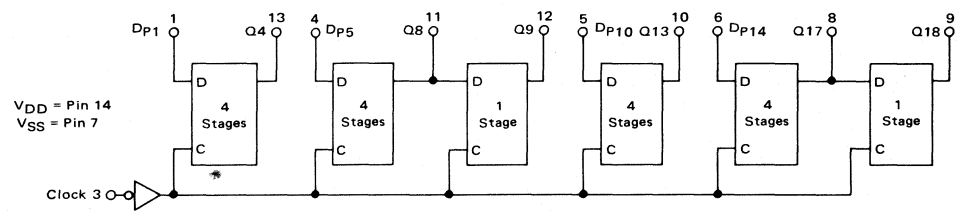
Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14006AL —MC14006CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14006AL —MC14006CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE
(Single Stage)

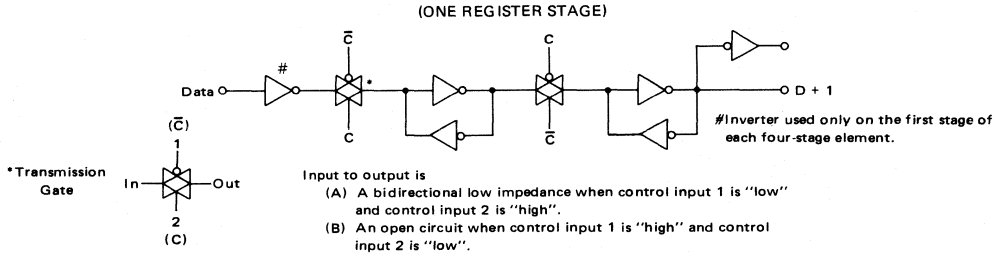
D_n	C	Q_{n+1}
0	⌐¯	0
1	¯⌐	1
X	⌐_	Q_n

X = Don't Care

BLOCK DIAGRAM



LOGIC DIAGRAM
(ONE REGISTER STAGE)



#Inverter used only on the first stage of each four-stage element.

*Transmission Gate

Input to output is
(A) A bidirectional low impedance when control input 1 is "low" and control input 2 is "high".
(B) An open circuit when control input 1 is "high" and control input 2 is "low".

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14006AL -55°C Min	MC14006AL -55°C Max	MC14006AL +25°C Min	MC14006AL +25°C Typ	MC14006AL +25°C Max	MC14006AL +125°C Min	MC14006AL +125°C Max	MC14006CL/CP -40°C Min	MC14006CL/CP -40°C Max	MC14006CL/CP +25°C Min	MC14006CL/CP +25°C Typ	MC14006CL/CP +25°C Max	MC14006CL/CP +85°C Min	MC14006CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	3,4	P_D	5.0	–	2.5	–	0.025	2.5	–	150	–	25	–	0.05	25	–	350	μW
			10	–	10	–	0.05	10	–	600	–	100	–	0.2	100	–	1400	
			15	–	–	–	0.35	–	–	–	–	–	–	0.70	–	–	–	
Output Rise and Fall Times** (C_L = 15 pF)	5	t_r, t_f																ns
t_r, t_f = (4.8 ns/pF) C_L + 28 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (2.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (2.2 ns/pF) C_L + 2.0 ns			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Turn-Off and Turn-On Delay Times** (C_L = 15 pF)	5	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (5.0 ns/pF) C_L + 175 ns			5.0	–	–	–	250	400	–	–	–	–	–	250	500	–	–	
t_{PLH}, t_{PHL} = (2.4 ns/pF) C_L + 44 ns			10	–	–	–	80	145	–	–	–	–	–	80	250	–	–	
t_{PLH}, t_{PHL} = (2.0 ns/pF) C_L + 30 ns			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Minimum Clock Pulse Width		PW_C	5.0	–	–	–	100	200	–	–	–	–	–	100	250	–	–	ns
			10	–	–	–	60	70	–	–	–	–	–	60	125	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)		PRF	5.0	–	–	2.5	5.0	–	–	–	–	–	2.0	5.0	–	–	–	MHz
			10	–	–	7.0	8.3	–	–	–	–	–	4.0	8.3	–	–	–	
			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Maximum Clock Pulse Rise and Fall Time# (C_L = 15 pF)		t_f, t_f	5.0	–	–	15	–	–	–	–	–	–	15	–	–	–	–	μs
			10	–	–	15	–	–	–	–	–	–	15	–	–	–	–	
Setup Time (C_L = 15 pF)	5	t_{setup}	5.0	–	–	–	-50	-15	–	–	–	–	–	-50	0	–	–	ns
			10	–	–	–	-15	-5.0	–	–	–	–	–	-15	0	–	–	
			15	–	–	–	-8.0	–	–	–	–	–	–	-8.0	–	–	–	
Hold Time (C_L = 15 pF)	5	t_{hold}	5.0	–	–	–	75	180	–	–	–	–	–	75	220	–	–	ns
			10	–	–	–	25	90	–	–	–	–	–	25	110	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.
When shift register sections are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the rise and fall times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

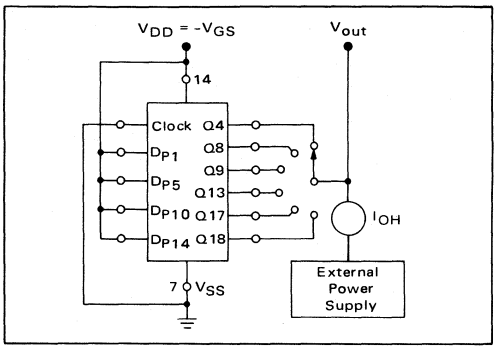


FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT

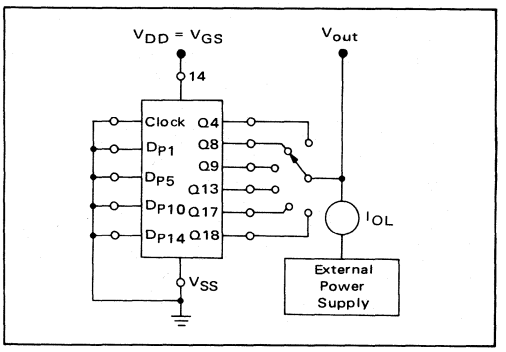


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

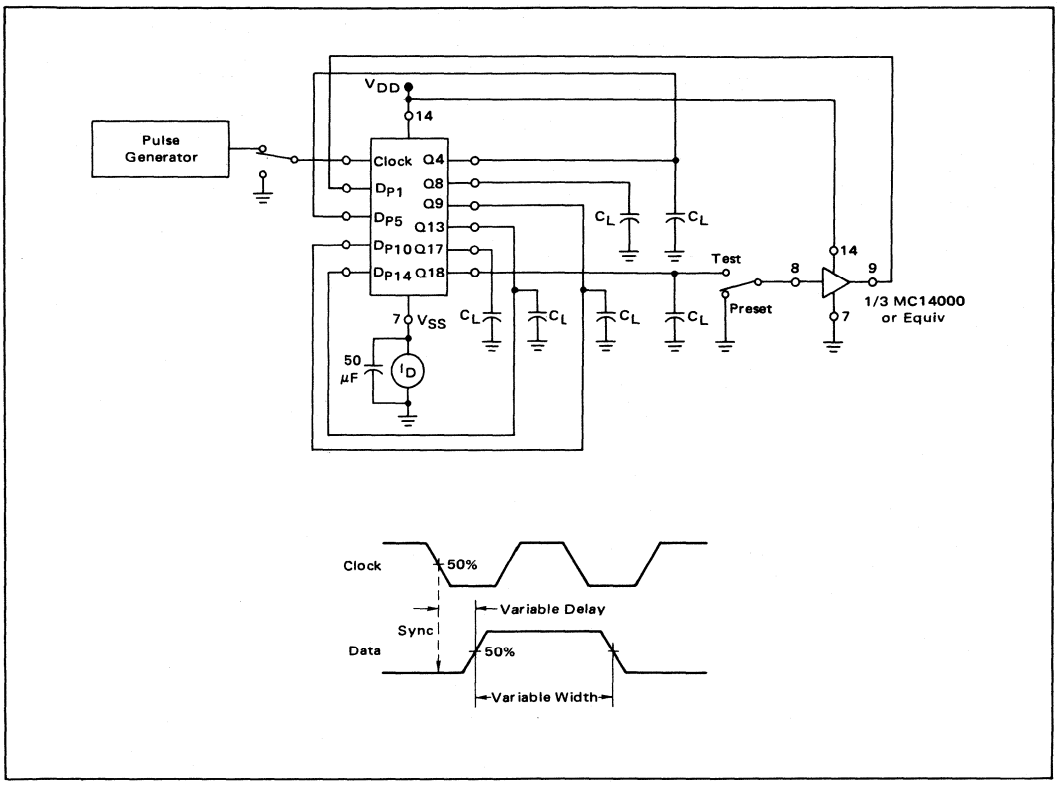
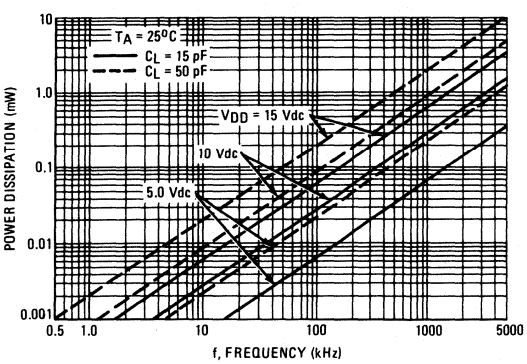


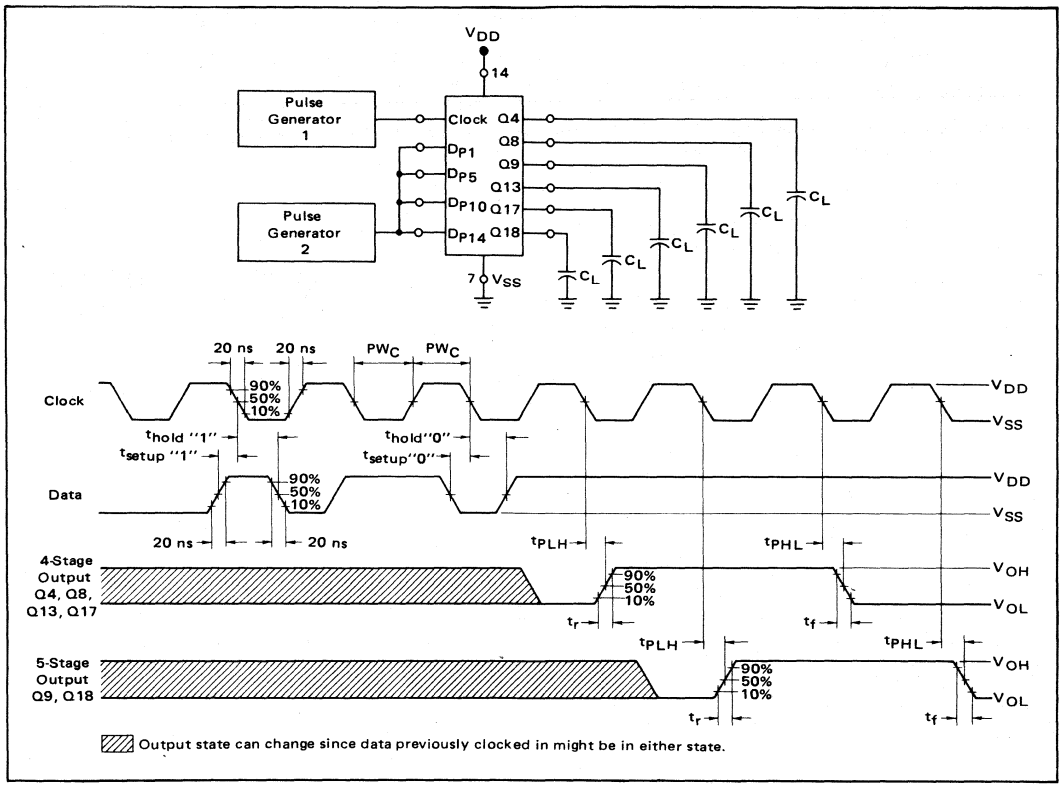
FIGURE 4 – TYPICAL POWER DISSIPATION versus CLOCK FREQUENCY CHARACTERISTICS PER STAGE



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: All unused inputs should be returned to V_{DD} or V_{SS} as appropriate for circuit application.

MC14007AL
MC14007CL
MC14007CP

DUAL COMPLEMENTARY PAIR PLUS INVERTER

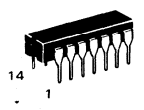
The MC14007 multi-purpose device consists of three N-channel and three P-channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse-shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14007AL)
  3.0 Vdc to 16 Vdc (MC14007CL/CP)
- Single Supply Operation = Positive or Negative
- Symmetrical Output Impedance — 200 ohms typical @ 10 Vdc
- Pin-for-Pin Replacement for CD4007A

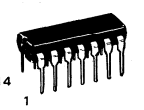
McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL COMPLEMENTARY PAIR PLUS INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

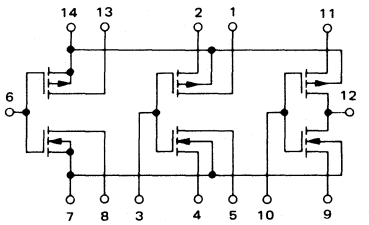


P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

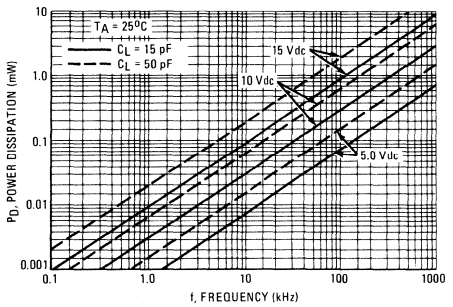
Rating	Symbol	Value	Unit
DC Supply Voltage — MC14007AL — MC14007CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14007AL — MC14007CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

SCHEMATIC



V_{DD} = Pin 14
V_{SS} = Pin 7

FIGURE 1 — TYPICAL POWER DISSIPATION CHARACTERISTICS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14007AL -55°C Min	MC14007AL -55°C Max	MC14007AL +25°C Min	MC14007AL +25°C Typ	MC14007AL +25°C Max	MC14007AL +125°C Min	MC14007AL +125°C Max	MC14007CL/CP -40°C Min	MC14007CL/CP -40°C Max	MC14007CL/CP +25°C Min	MC14007CL/CP +25°C Typ	MC14007CL/CP +25°C Max	MC14007CL/CP +85°C Min	MC14007CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	0.05	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
(V_{out} = 3.5 Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} = 7.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} = 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} = 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} = 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source	2		5.0	-1.75	–	-1.4	-4.0	–	-1.0	–	-1.3	–	-1.1	-4.0	–	-0.9		
(V_{OH} = 9.5 Vdc)			10	-1.35	–	-1.1	-2.5	–	-0.75	–	-0.65	–	-0.55	-2.5	–	-0.45	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-9.0	–	–	–	–	–	–	-9.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	3	I_{OL}	5.0	0.75	–	0.6	1.0	–	0.4	–	0.35	–	0.3	1.0	–	0.24	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.5	–	0.95	–	1.2	–	1.0	2.5	–	0.8	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = +15 pF)																		
P_D = (1000 μW/MHz) f + 0.005 μW	1,4	P_D	5.0	–	0.25	–	0.005	0.25	–	15	–	2.5	–	0.025	2.5	–	75	μW
P_D = (4000 μW/MHz) f + 0.01 μW			10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
P_D = (9000 μW/MHz) f + 0.025 μW			15	–	–	–	0.025	–	–	–	–	–	–	0.25	–	–	–	
Output Rise Time**	4	t_r																ns
(C_L = 15 pF)																		
t_r = (1.2 ns/pF) C_L + 17 ns			5.0	–	–	–	35	75	–	–	–	–	–	35	100	–	–	
t_r = (0.5 ns/pF) C_L + 12.5 ns			10	–	–	–	20	40	–	–	–	–	–	20	50	–	–	
t_r = (0.4 ns/pF) C_L + 11 ns			15	–	–	–	16	–	–	–	–	–	–	16	–	–	–	
Output Fall Time**	4	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF)C_L + 12.5 ns			5.0	–	–	–	35	75	–	–	–	–	–	35	100	–	–	
t_f = (0.5 ns/pF) C_L + 12.5 ns			10	–	–	–	20	40	–	–	–	–	–	20	50	–	–	
t_f = (0.4 ns/pF) C_L + 9.0 ns			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Turn-On Delay Time**	4	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (1.0 ns/pF) C_L + 15 ns			5.0	–	–	–	30	60	–	–	–	–	–	30	75	–	–	
t_{PHL} = (0.3 ns/pF) C_L + 10.5 ns			10	–	–	–	15	40	–	–	–	–	–	15	50	–	–	
t_{PHL} = (0.2 ns/pF) C_L + 9.5 ns			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Turn-Off Delay Time**	4	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (0.5 ns/pF) C_L + 22.5 ns			5.0	–	–	–	30	60	–	–	–	–	–	30	75	–	–	
t_{PLH} = (0.2 ns/pF) C_L + 12 ns			10	–	–	–	15	40	–	–	–	–	–	15	50	–	–	
t_{PLH} = (0.15 ns/pF) C_L + 9.0 ns			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level, that the circuit will withstand before producing an output state change.

**The formula given is for the typical characteristics only.

Note: All unused inputs must be returned to either V_{DD} or V_{SS} as appropriate for the circuit application.

FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

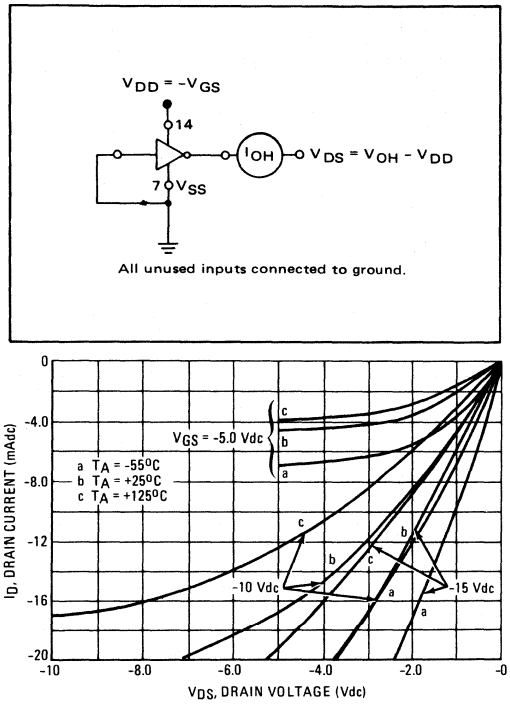


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS

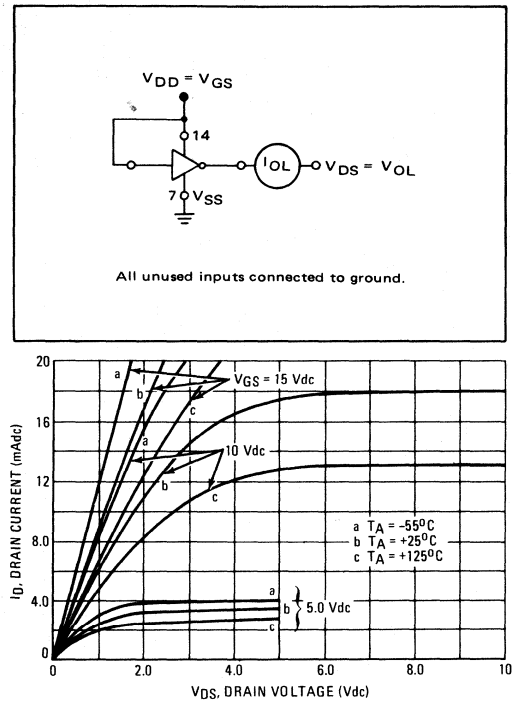
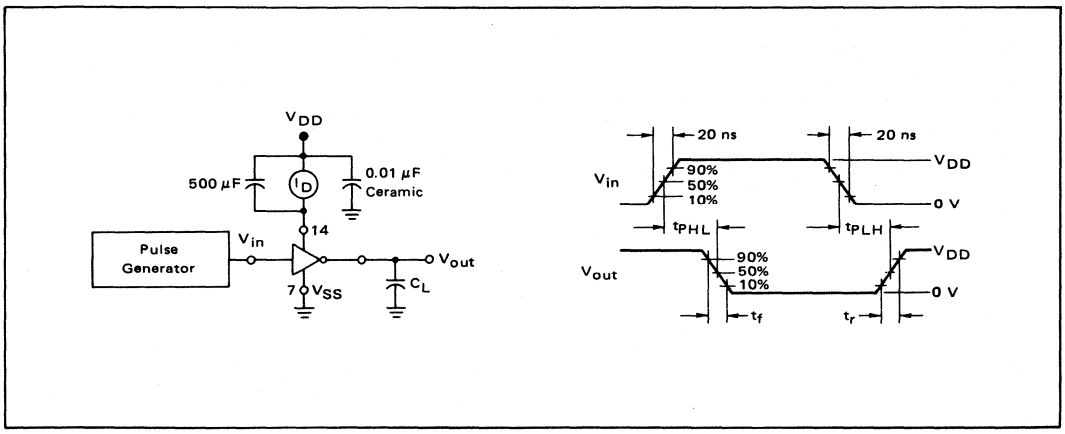


FIGURE 4 – SWITCHING TIME AND POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

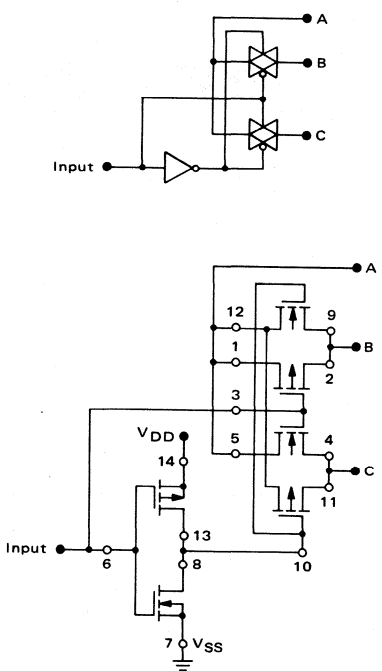


7

APPLICATIONS

The MC14007 dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Shown are a few examples of the device flexibility.

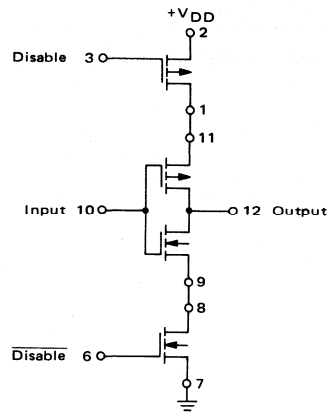
FIGURE 5 – 2-INPUT ANALOG MULTIPLEXER



INPUT	OUTPUT CONDITION
1	A = C, B = Open
0	A = B, C = Open

Substrates of P-channel devices internally connected to V_{DD};
Substrates of N-channel devices internally connected to V_{SS}.

FIGURE 6 – 3-STATE BUFFER



INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	Open

X = Don't Care

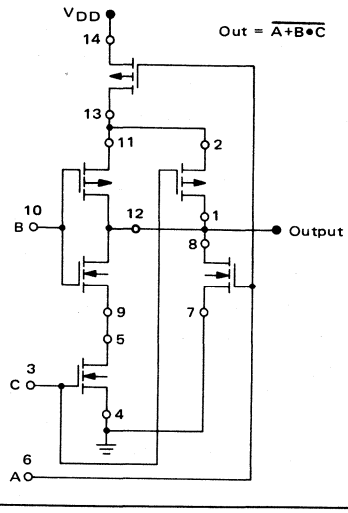


FIGURE 7 – AOI FUNCTIONS USING TREE LOGIC

MC14008AL
MC14008CL
MC14008CP

4-BIT FULL ADDER

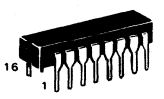
The MC14008 4-bit full adder is constructed with MOS P–channel and N-channel enhancement mode devices in a single monolithic structure. This device consists of four full adders with fast internal look-ahead carry output. It is useful in binary addition and other arithmetic applications. The fast parallel carry output bit allows high-speed operation when used with other adders in a system.

- Look-Ahead Carry Output
- High-Speed Operation – 150 ns typical from Sum_{in} to Sum_{out}
- Low Power Dissipation – 1.0 μW typical @ 10 V
- Diode Protection on All Inputs
- All Outputs Buffered
- Pin-for-Pin Replacement for CD4008A

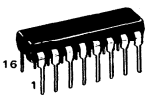
McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT FULL ADDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

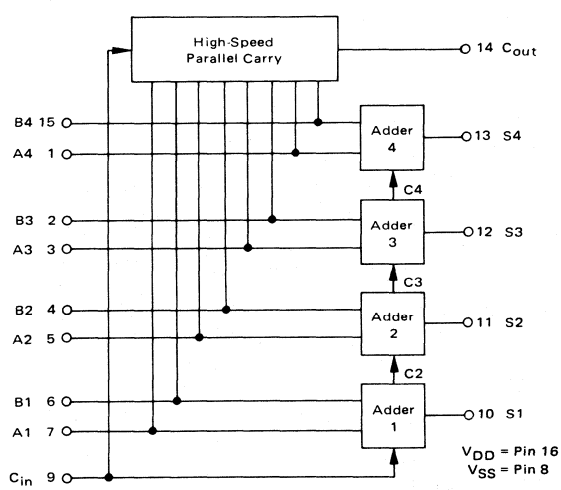


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14008AL -MC14008CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14008AL -MC14008CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE
(One Stage)

C_{in}	B	A	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14008AL -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC14008CL/CP -40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	1																	
(V_{OH} = 2.5 Vdc) Source		I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.6	–	0.28	–	0.23	–	0.2	0.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.6	–	0.65	–	0.6	–	0.5	1.6	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}																
C_{in} Input			–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pF
All other inputs			–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation	–	P_D	5.0	–	25	–	0.25	25	–	1500	–	250	–	0.25	250	–	3500	μW
			10	–	100	–	1.0	100	–	6000	–	1000	–	1.0	1000	–	14000	
			15	–	–	–	4.0	–	–	–	–	–	–	4.0	–	–	–	
Output Rise and Fall Time**	5	t_r,t_f																ns
(C_L = 15 pF)																		
t_r,t_f = (2.9 ns/pF) C_L + 57 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r,t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r,t_f = (1.0 ns/pF) C_L + 10 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Sum In to Sum Out Delay Time**		t_{PHL},t_{PLH}																ns
(C_L = 15 pF)	5																	
t_{PHL},t_{PLH} = (1.8 ns/pF) C_L + 398 ns			5.0	–	–	–	425	750	–	–	–	–	–	425	1200	–	–	
t_{PHL},t_{PLH} = (0.8 ns/ pF)C_L + 158 ns			10	–	–	–	170	250	–	–	–	–	–	170	400	–	–	
t_{PHL},t_{PLH} = (0.6 ns/pF) C_L + 116 ns			15	–	–	–	125	–	–	–	–	–	–	125	–	–	–	
Sum In to Carry Out Delay Time**	5	t_{PHL},t_{PLH}																ns
(C_L = 15 pF)																		
t_{PHL},t_{PLH} = (1.8 ns/pF) C_L + 223 ns			5.0	–	–	–	250	500	–	–	–	–	–	250	800	–	–	
t_{PHL},t_{PLH} = (0.8 ns/pF) C_L + 103 ns			10	–	–	–	115	200	–	–	–	–	–	115	240	–	–	
t_{PHL},t_{PLH} = (0.6 ns/pF) C_L + 81 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Carry In to Sum Out Delay Time**	5	t_{PHL},t_{PLH}																ns
(C_L = 15 pF)																		
t_{PHL},t_{PLH} = (1.8 ns/pF) C_L + 293 ns			5.0	–	–	–	320	650	–	–	–	–	–	320	1000	–	–	
t_{PHL},t_{PLH} = (0.8 ns/pF) C_L+113 ns			10	–	–	–	125	225	–	–	–	–	–	125	300	–	–	
t_{PHL},t_{PLH} = (0.6 ns/pF) C_L +86 ns			15	–	–	–	95	–	–	–	–	–	–	95	–	–	–	
Carry In to Carry Out Delay Time**	5	t_{PHL},t_{PLH}																ns
(C_L = 15 pF)																		
t_{PHL},t_{PLH} = (1.8 ns/pF) C_L + 88 ns			5.0	–	–	–	115	175	–	–	–	–	–	115	200	–	–	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L +33 ns			10	–	–	–	45	75	–	–	–	–	–	45	90	–	–	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 26 ns			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum boltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT

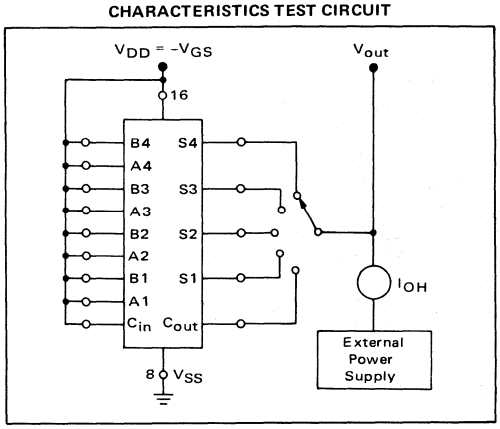


FIGURE 2 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT

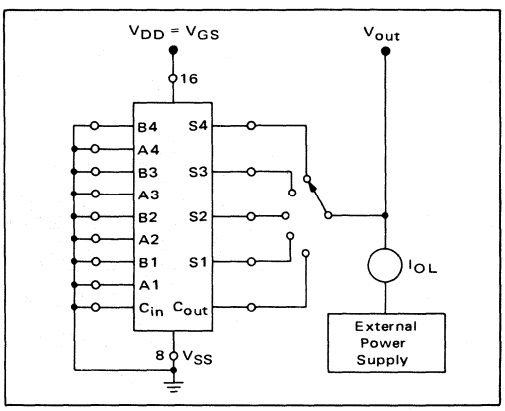


FIGURE 3 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

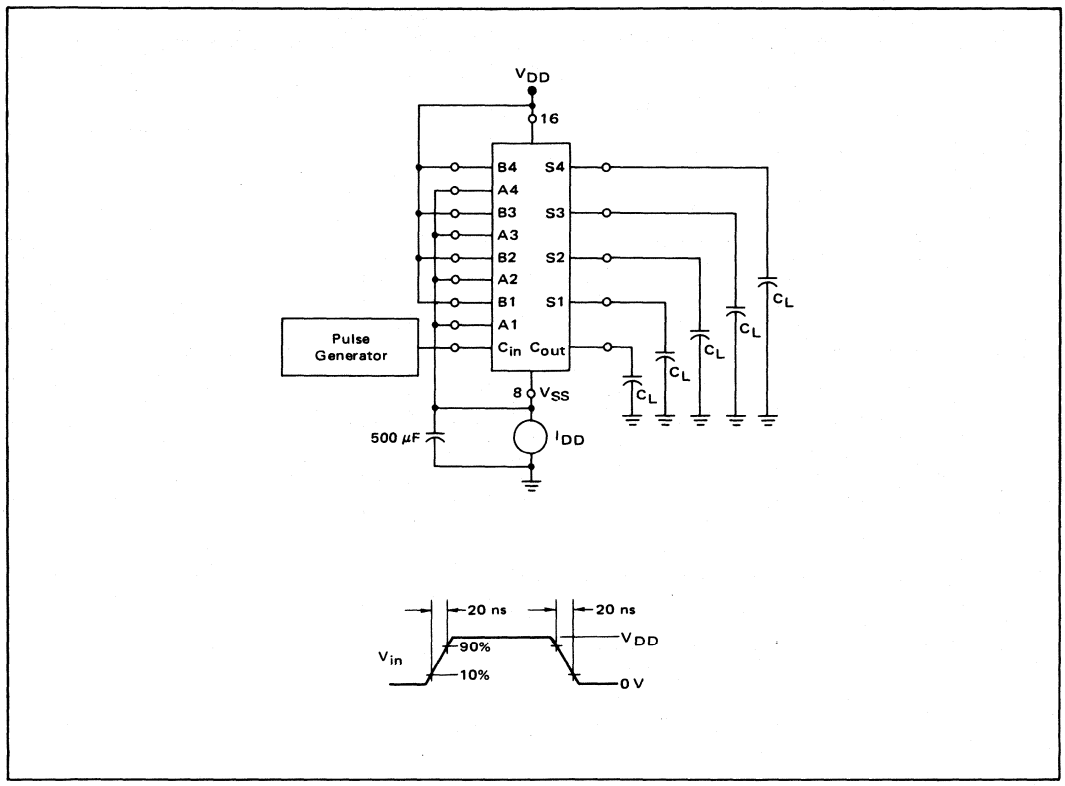


FIGURE 4 – TYPICAL POWER DISSIPATION CHARACTERISTICS

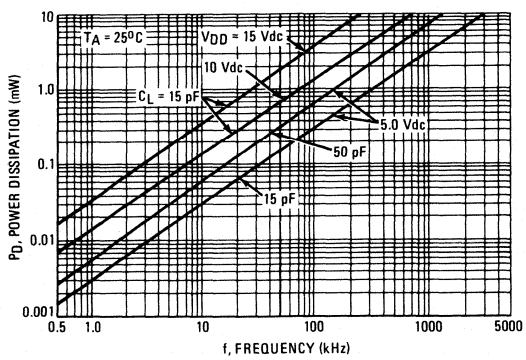


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

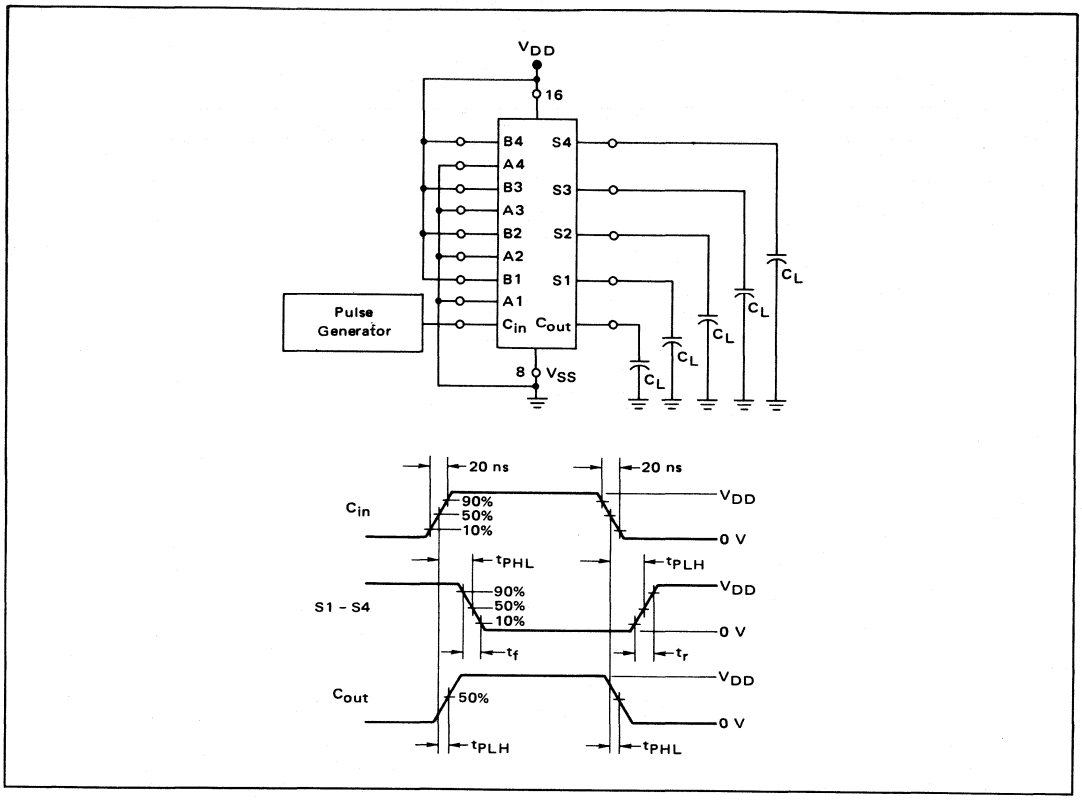
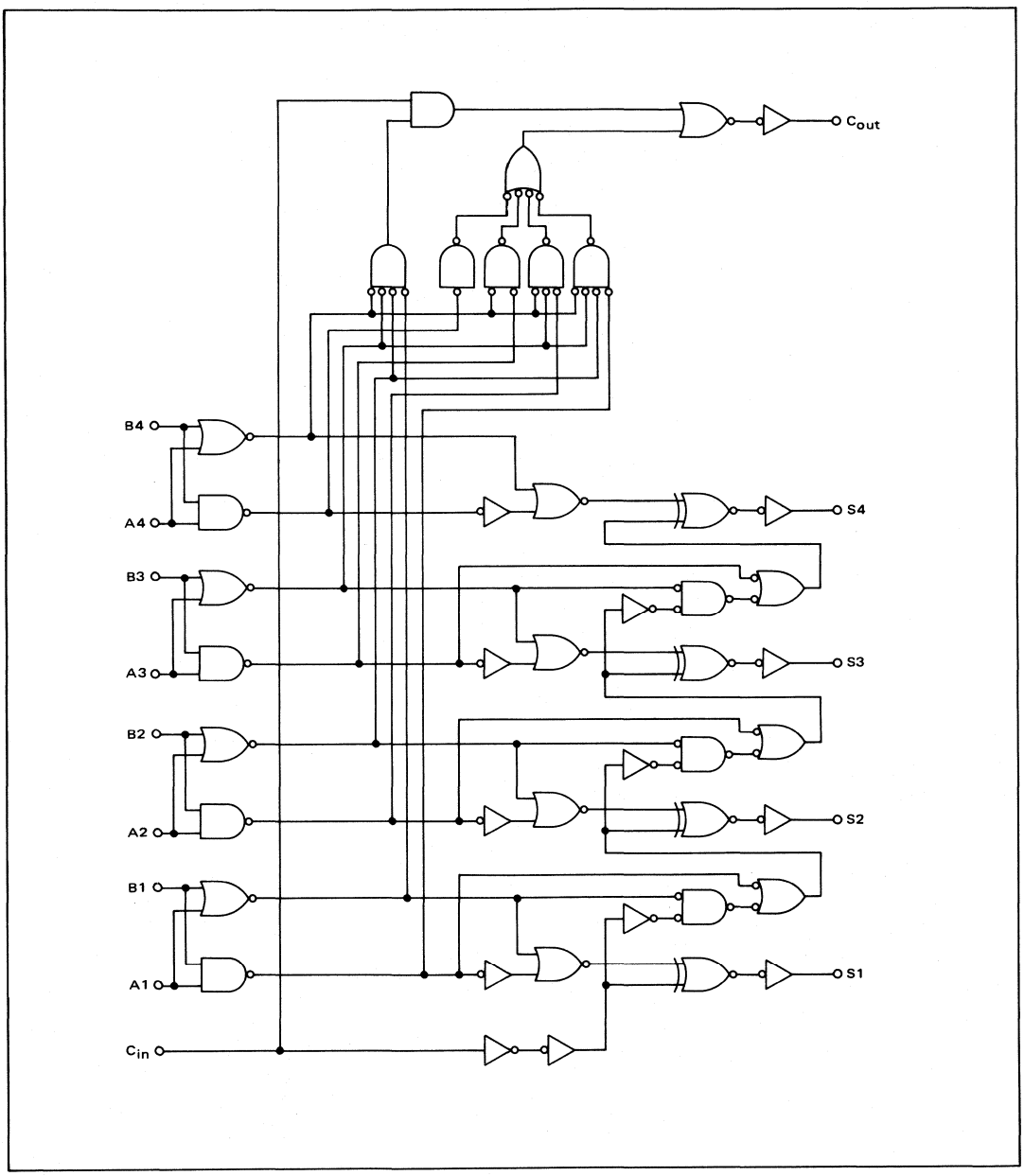
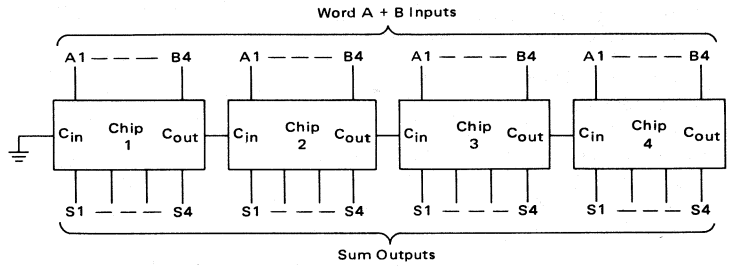


FIGURE 6 – LOGIC DIAGRAM



TYPICAL APPLICATION

FIGURE 7 – USING THE MC14008 IN A 16-BIT ADDER CONFIGURATION



Calculation of 16-bit adder speed:

t_p total = t_p (Sum to Carry) + t_p (Carry to Sum) + 2 t_p (Carry to Carry)

Typically, the overall 16-bit adder speed at 10 V is:

t_p total = 115 + 125 + 90 = 330 ns typ

MC14009AL
MC14009CL
MC14009CP
MC14010AL
MC14010CL
MC14010CP

HEX BUFFERS

The MC14009 hex inverter/buffer and MC14010 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. Both devices can be used as current "sink" or "source" drivers, as CMOS-to-CMOS or CMOS-to-bipolar (TTL or DTL) logic level converters, or as multiplexers (1-to-6). The MC14009 also provides the invert function.

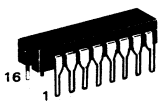
- Quiescent Power Dissipation = 50 nW/package typical
- High Current Sinking Capability
  8.0 mA minimum @ V_{OL} = 0.5 V and V_{DD} = 10 V
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14009/10 AL)
  3.0 Vdc to 16 Vdc (MC14009/10CL/CP)
- Wide CMOS-to-Bipolar Conversion Range –
  From MCMOS operating with specified supply voltage range to TTL or DTL operating with +3.0 V to +6.0 V supply. Conversion with logic output levels > 6.0 V is permitted if $V_{CC} \leqslant V_{DD}$.
- Pin for Pin Replacement for CD4009A – MC14009
  CD4010A – MC14010

McMOS

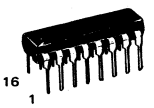
(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14009AL/CL/CP
Noninverting – MC14010AL/CL/CP



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

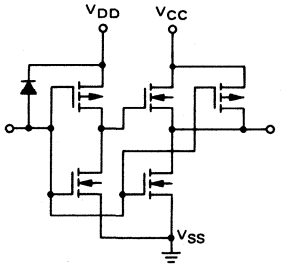
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage ($V_{CC} \leqslant V_{DD}$) –AL Version	V_{DD}	+18 to -0.5	Vdc
CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin*	I	10	mAdc
Operating Temperature Range –AL Version	T_A	-55 to +125	°C
CL,CP Version		-40 to +85	
Storage Temperature Range	T_{stg}	-65 to +150	°C

*Buffered Outputs may supply higher current.

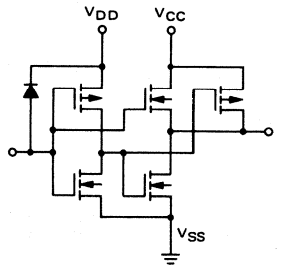
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

MC14009



All P-Channel substrates = V_{DD}

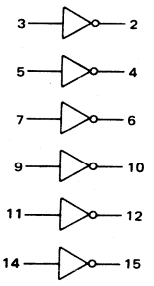
MC14010



All N-Channel substrates = V_{SS}

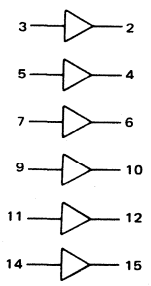
LOGIC DIAGRAMS

MC14009



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

MC14010



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

See Mechanical Data Section for package dimensions.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	V_{CC} Vdc	MC14009/10AL -55°C Min	MC14009/10AL -55°C Max	MC14009/10AL +25°C Min	MC14009/10AL +25°C Typ	MC14009/10AL +25°C Max	MC14009/10AL +125°C Min	MC14009/10AL +125°C Max	MC14009/10CL/CP -40°C Min	MC14009/10CL/CP -40°C Max	MC14009/10CL/CP +25°C Min	MC14009/10CL/CP +25°C Typ	MC14009/10CL/CP +25°C Max	MC14009/10CL/CP +85°C Min	MC14009/10CL/CP +85°C Max	Unit
Output Voltage	1,2,3	V_{out}																	Vdc
MC14009																			
(V_{in} = 5.0 Vdc)			5.0	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 10 Vdc)			10	10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 15 Vdc)			15	–	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14010 "0" Level																			
(V_{in} = 0 Vdc)			5.0	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			10	10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			15	–	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14009																			Vdc
(V_{in} = 0 Vdc)			5.0	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 0 Vdc)			10	10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 0 Vdc)			15	–	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
MC14010 "1" Level																			
(V_{in} = 5.0 Vdc)			5.0	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 10 Vdc)			10	10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 15 Vdc)			15	–	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																	Vdc
MC14009																			
(V_{out} ≥3.5 Vdc)			5.0	5.0	1.0	–	1.0	2.0	–	0.9	–	1.0	–	1.0	2.0	–	0.9	–	
(V_{out} ≥7.0 Vdc)			10	10	2.0	–	2.0	3.0	–	1.2	–	2.0	–	2.0	3.0	–	1.9	–	
(V_{out} ≥10.5 Vdc)			15	15	–	–	–	4.5	–	–	–	–	–	–	4.5	–	–	–	
(V_{out} ≤1.5 Vdc)		V_{NH}	5.0	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)			10	10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≤4.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
MC14010		V_{NL}																	Vdc
(V_{out} ≤1.5 Vdc)			5.0	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤3.0 Vdc)			10	10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{out} ≤4.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≥3.5 Vdc)		V_{NH}	5.0	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥7.0 Vdc)			10	10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≥10.5 Vdc)			15	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																			
	5	I_{OH}																	mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	5.0	-1.85	–	-1.25	-1.75	–	-0.9	–	-1.5	–	-1.25	-1.75	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	10	-0.9	–	-0.6	-0.8	–	-0.4	–	-0.72	–	-0.6	-0.8	–	-0.48	–	
(V_{OH} = 13.5 Vdc)			15	15	–	–	–	-5.0	–	–	–	–	–	–	-5.0	–	–	–	
	6	I_{OL}																	mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	5.0	3.75	–	3.0	4.0	–	2.1	–	3.6	–	3.0	4.0	–	2.4	–	
(V_{OL} = 0.5 Vdc)			10	10	10	–	8.0	10	–	5.6	–	9.6	–	8.0	10	–	6.4	–	
(V_{OL} = 1.5 Vdc)			15	15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Input Current	–	I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance MC14009	–	C_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pF
(V_{in} = 0) MC14010			–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation	7	P_D	5.0	–	–	1.5	–	0.05	1.5	–	100	–	15	–	0.15	15	–	210	μW
			10	–	–	5.0	–	0.1	5.0	–	300	–	50	–	0.5	50	–	700	
			15	–	–	–	–	0.15	–	–	–	–	–	–	0.85	–	–	–	
Turn-On Delay Time**	4	t_{PHL}																	ns
(C_L = 15 pF)																			
MC14009																			
t_{PHL} = (0.16 ns/pF) C_L + 12 ns			5.0	5.0	–	–	–	15	55	–	–	–	–	–	15	70	–	–	
t_{PHL} = (0.10 ns/pF) C_L + 8.0 ns			10	10	–	–	–	9.0	30	–	–	–	–	–	9.0	40	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 6.0 ns			15	15	–	–	–	7.0	–	–	–	–	–	–	7.0	–	–	–	
t_{PHL} = (0.05 ns/pF) C_L + 7.0 ns			10	5.0	–	–	–	8.0	25	–	–	–	–	–	8.0	35	–	–	
t_{PHL} = (0.03 ns/pF) C_L + 5.0 ns			15	5.0	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
MC14010																			
t_{PHL} = (0.38 ns/pF) C_L + 19 ns			5.0	5.0	–	–	–	25	55	–	–	–	–	–	25	70	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 19 ns			10	10	–	–	–	20	30	–	–	–	–	–	20	40	–	–	
t_{PHL} = (0.06 ns/pF) C_L + 14 ns			15	15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
t_{PHL} = (0.08 ns/pF) C_L + 14 ns			10	5.0	–	–	–	15	25	–	–	–	–	–	15	35	–	–	
t_{PHL} = (0.09 ns/pF) C_L + 9.0 ns			15	5.0	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
Turn-Off Delay Time**	4	t_{PLH}																	ns
(C_L = 15 pF)																			
MC14009/10																			
t_{PLH} = (1.0 ns/pF) C_L + 35 ns			5.0	5.0	–	–	–	50	80	–	–	–	–	–	50	100	–	–	
t_{PLH} = (0.40 ns/pF) C_L + 19 ns			10	10	–	–	–	25	55	–	–	–	–	–	25	70	–	–	
t_{PLH} = (0.34 ns/pF) C_L + 15 ns			15	15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
t_{PLH} = (0.36 ns/pF) C_L + 20 ns			10	5.0	–	–	–	25	30	–	–	–	–	–	25	40	–	–	
t_{PLH} = (0.16 ns/pF) C_L + 18 ns			15	5.0	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Output Rise Time**	4	t_r																	ns
(C_L = 15 pF)																			
MC14009																			
t_r = (2.4 ns/pF) C_L + 44 ns			5.0	5.0	–	–	–	80	125	–	–	–	–	–	80	160	–	–	
t_r = (1.0 ns/pF) C_L + 20 ns			10	10	–	–	–	35	100	–	–	–	–	–	35	120	–	–	
t_r = (0.62 ns/pF) C_L + 20 ns			15	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
MC14010																			
t_r = (1.6 ns/pF) C_L + 56 ns			5.0	5.0	–	–	–	80	125	–	–	–	–	–	80	160	–	–	
t_r = (0.76 ns/pF) C_L + 39 ns			10	10	–	–	–	50	100	–	–	–	–	–	50	120	–	–	
t_r = (0.6 ns/pF) C_L + 21 ns			15	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Output Fall Time **	4	t_f																	ns
(C_L = 15 pF)																			
MC14009																			
t_f = (0.22 ns/pF) C_L + 9.0 ns			5.0	5.0	–	–	–	13	45	–	–	–	–	–	13	60	–	–	
t_f = (0.10 ns/pF) C_L + 7.0 ns			10	10	–	–	–	9.0	40	–	–	–	–	–	9.0	50	–	–	
t_f = (0.07 ns/pF) C_L + 6.0 ns			15	15	–	–	–	7.0	–	–	–	–	–	–	7.0	–	–	–	
MC14010																			
t_f = (0.20 ns/pF) C_L + 22 ns			5.0	5.0	–	–	–	25	45	–	–	–	–	–	25	60	–	–	
t_f = (0.07 ns/pF) C_L + 15 ns			10	10	–	–	–	16	40	–	–	–	–	–	16	50	–	–	
t_f = (0.07 ns/pF) C_L + 9.0 ns			15	15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

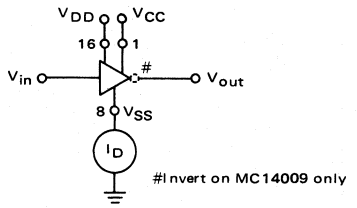


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS versus TEMPERATURE

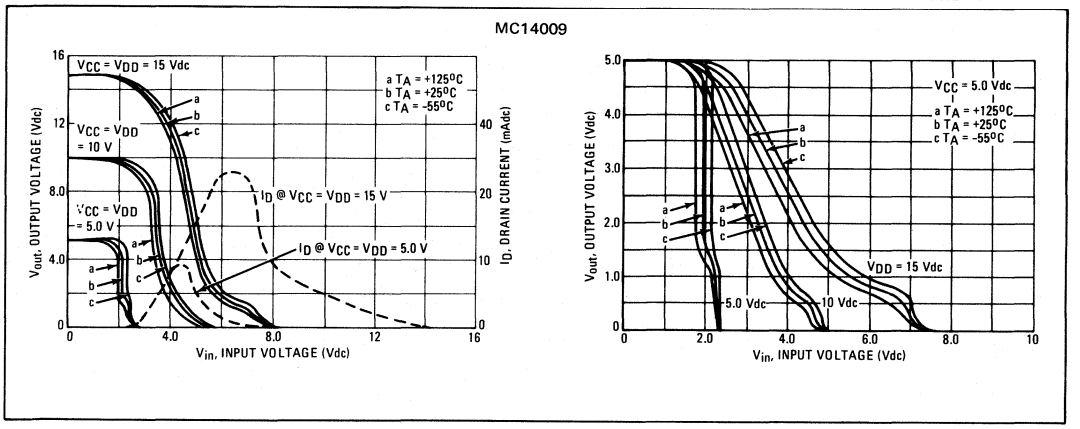


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

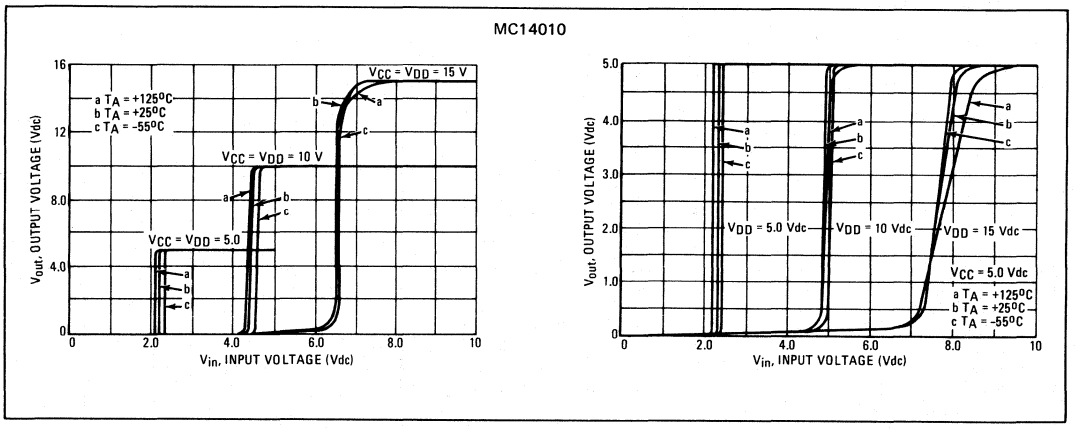


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

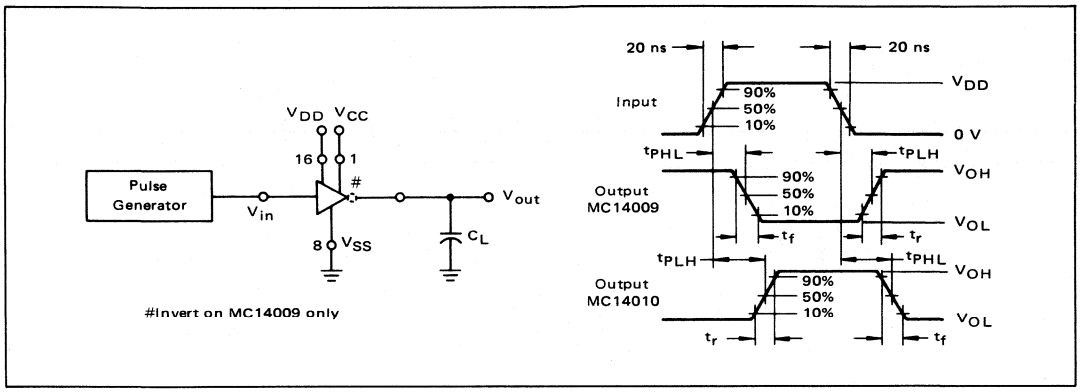


FIGURE 5 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

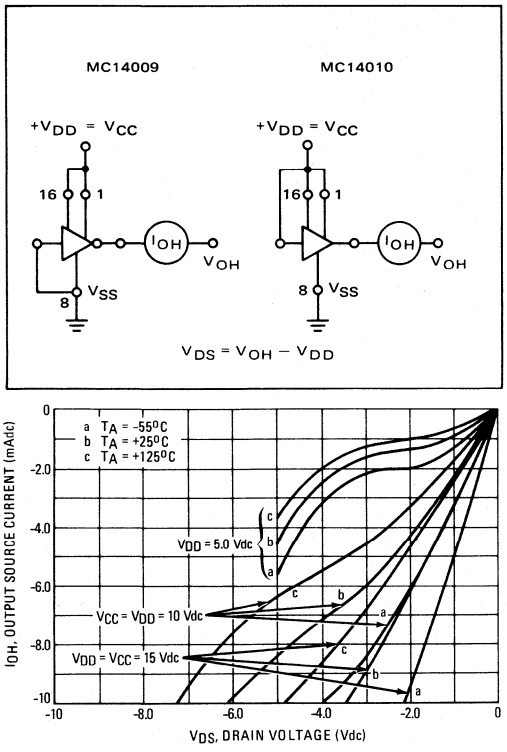
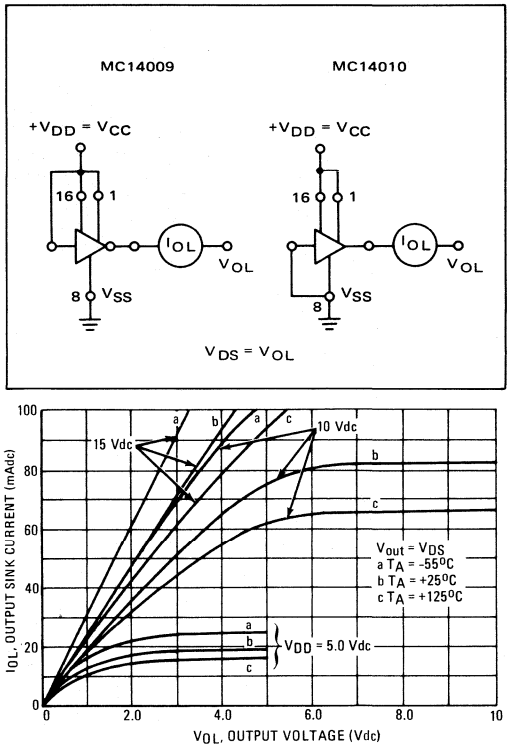
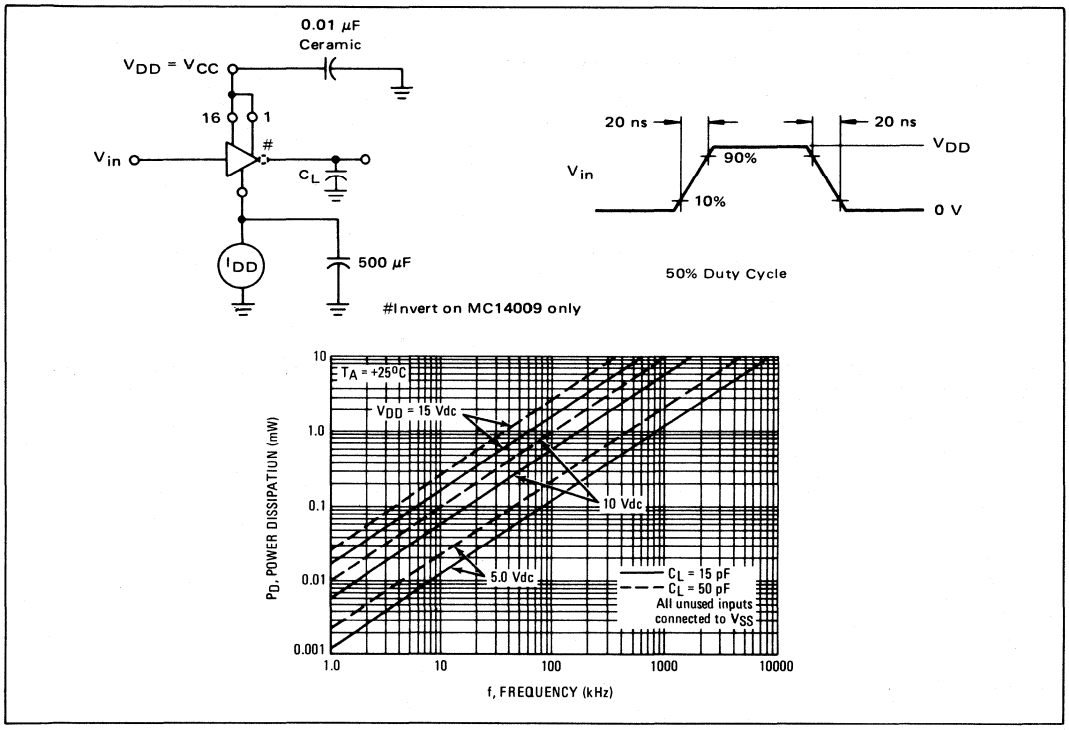


FIGURE 6 – TYPICAL OUTPUT SINK CHARACTERISTICS



7

FIGURE 7 – TYPICAL DYNAMIC POWER DISSIPATION CHARACTERISTICS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

7

MC14011AL
MC14011CL
MC14011CP

QUAD 2-INPUT "NAND" GATE

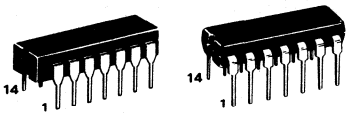
The MC14011 quad 2-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14011AL)
  3.0 Vdc to 16 Vdc (MC14011CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 750 ohms typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

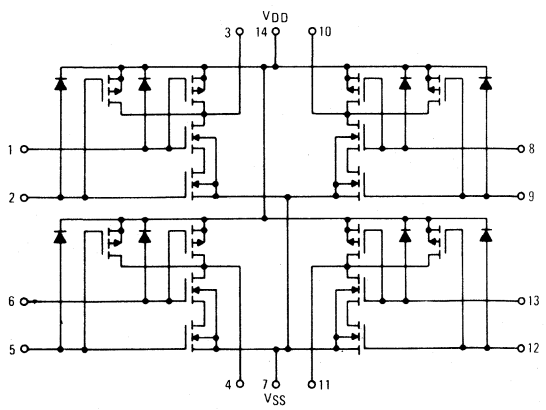
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14011AL MC14011CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14011AL –MC14011CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

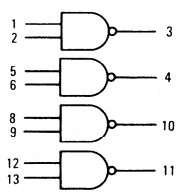
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$3 = \overline{1 \bullet 2}$

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14011AL -55°C Min	MC14011AL -55°C Max	MC14011AL +25°C Min	MC14011AL +25°C Typ	MC14011AL +25°C Max	MC14011AL +125°C Min	MC14011AL +125°C Max	MC14011CL/CP -40°C Min	MC14011CL/CP -40°C Max	MC14011CL/CP +25°C Min	MC14011CL/CP +25°C Typ	MC14011CL/CP +25°C Max	MC14011CL/CP +85°C Min	MC14011CL/CP +85°C Max	Unit
Output Voltage	"0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*																			
($V_{out} \geqslant 3.5$ Vdc)			V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geqslant 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \leqslant 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leqslant 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current																			
(V_{OH} = 2.5 Vdc)	Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)				10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)				10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
Input Current			I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)			C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF)			P_D																μW
				5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	
				10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
Output Rise and Fall Time (C_L = 15 pF)		3	t_r, t_f																ns
				5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Turn-On, Turn-Off Delay Time (C_L = 15 pF)		3	t_{PHL}, t_{PLH}																ns
				5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

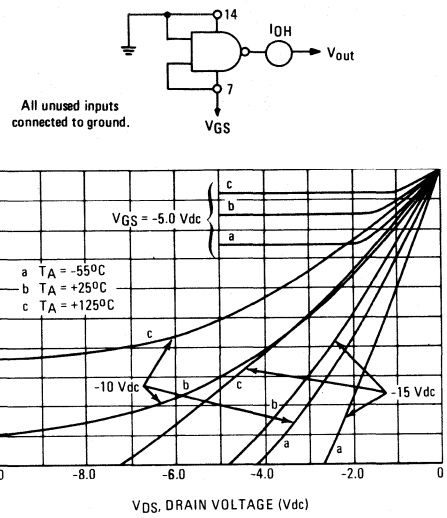


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

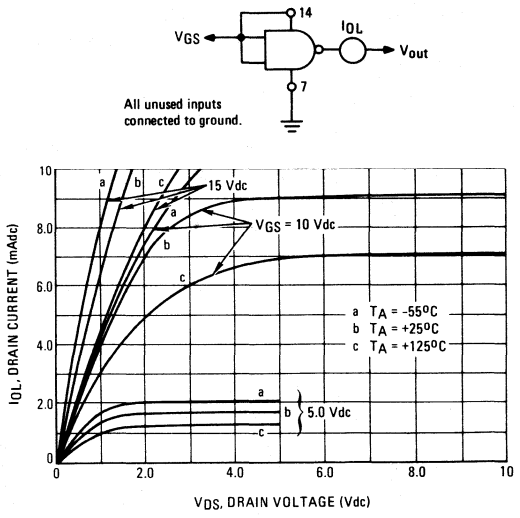
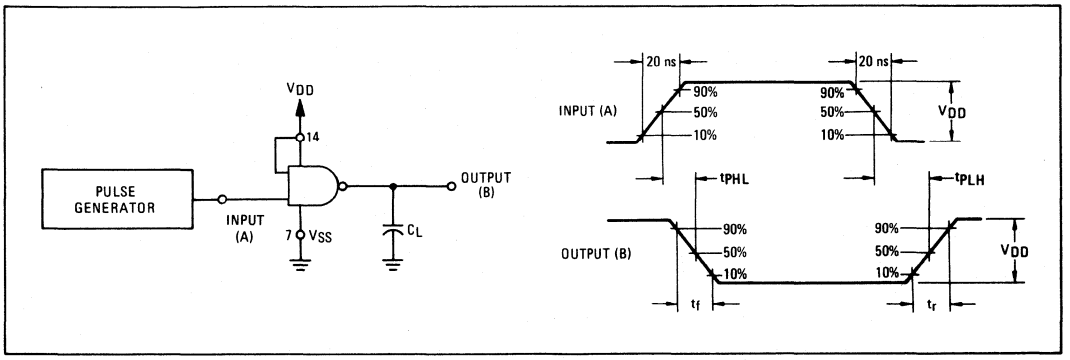


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14012AL
MC14012CL
MC14012CP

DUAL 4-INPUT "NAND" GATE

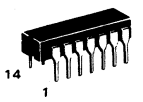
The MC14012 dual 4-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14012AL)
  = 3.0 Vdc to 16 Vdc (MC14012CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 750 ohms typical

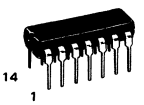
McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

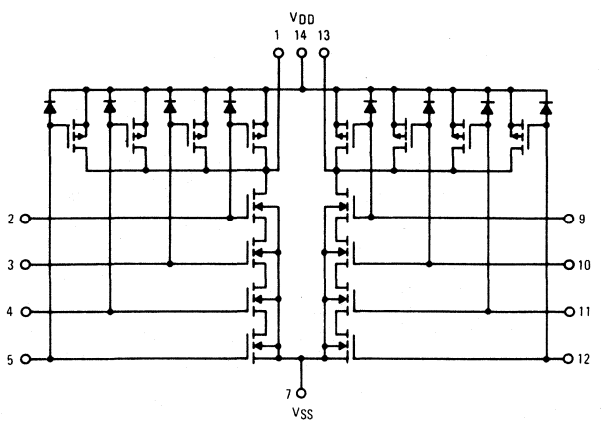
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

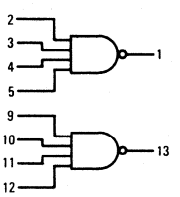
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14012AL MC14012CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14012AL MC14012CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

CIRCUIT SCHEMATIC



LOGIC DIAGRAM
POSITIVE LOGIC



$1 = \overline{2 \cdot 3 \cdot 4 \cdot 5}$

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14012AL							MC14012CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*																		
(V_{out} ≧ 3.5 Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} ≧ 7.0 Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{out} ≦ 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≦ 3.0 Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
Input Current		I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance		C_{in}	–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	3	P_D																μW
(C_L = 15 pF)			5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	
			10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
Output Rise and Fall Time	4	t_r,t_f																ns
(C_L = 15 pF)			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Turn-On, Turn-Off Delay Time	4	t_{PHL},t_{PLH}																ns
(C_L = 15 pF)			5.0	–	–	–	60	75	–	–	–	–	–	60	75	–	–	
			10	–	–	–	25	50	–	–	–	–	–	25	50	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

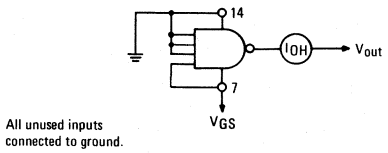
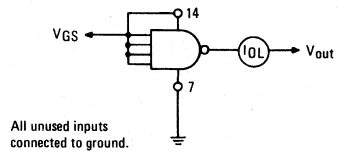
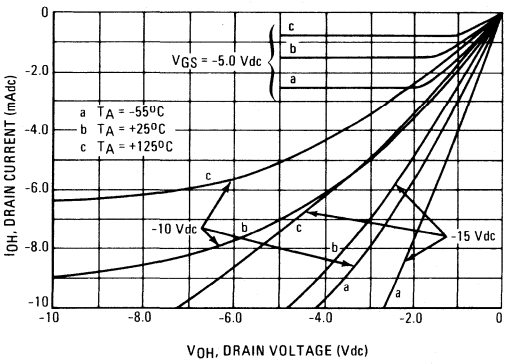


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT





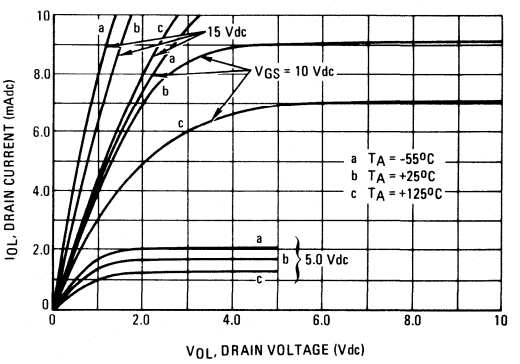


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

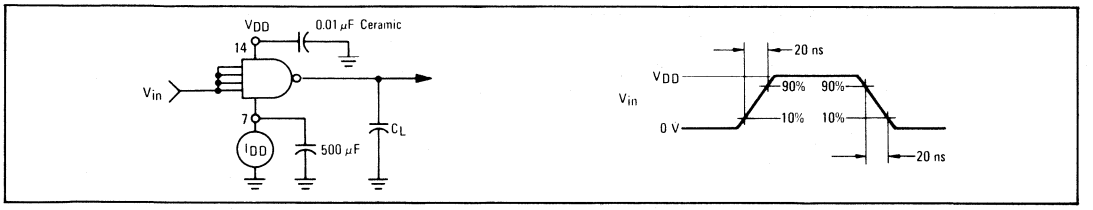
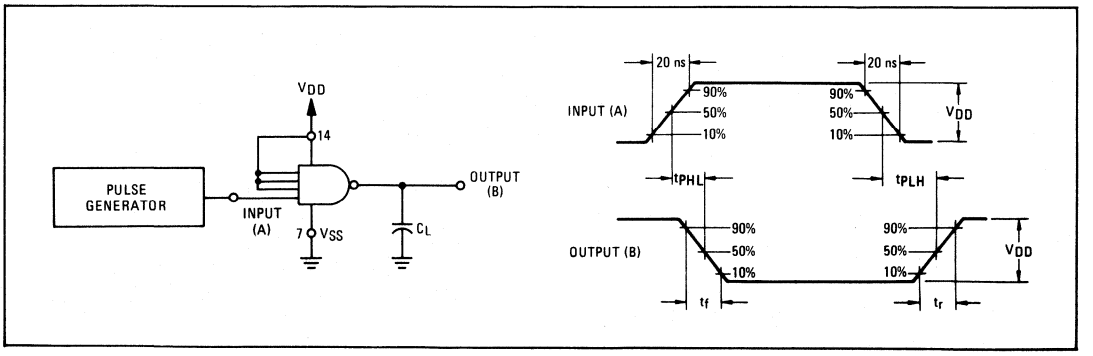


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14013AL
MC14013CL
MC14013CP

DUAL TYPE D FLIP-FLOP

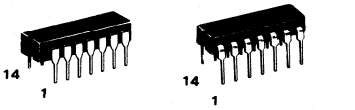
The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 25 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14013AL)
  = 3.0 Vdc to 16 Vdc (MC14013CL/CP)
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

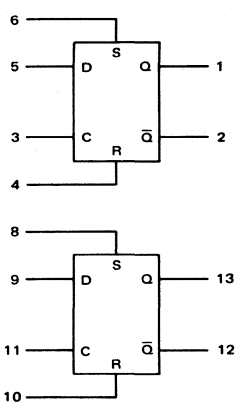
Rating	Symbol	Value	Unit
DC Supply Voltage MC14013AL MC14013CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14013AL – MC14013CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
↑	0	0	0	0	1	
↑	1	0	0	1	0	
↓	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	*	*	

X = Don't Care
† = Level Change
* = Invalid Condition

BLOCK DIAGRAM



V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Fig.	Symbol	Vdc	MC14013AL −55°C Min	MC14013AL −55°C Max	MC14013AL +25°C Min	MC14013AL +25°C Typ	MC14013AL +25°C Max	MC14013AL +125°C Min	MC14013AL +125°C Max	MC14013CL/CP −40°C Min	MC14013CL/CP −40°C Max	MC14013CL/CP +25°C Min	MC14013CL/CP +25°C Typ	MC14013CL/CP +25°C Max	MC14013CL/CP +85°C Min	MC14013CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)	–	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.5	-1.7	–	-0.35	–	-0.23	–	-0.2	-1.7	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.0	–	0.65	–	0.6	–	0.5	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**†	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (2.0 mW/MHz) f = 0.000025 mW			5.0	–	0.005	–	0.000025	0.005	–	0.3	–	0.05	–	0.000025	0.05	–	0.7	
P_D = (8.0 mW/MHz) f = 0.00010 mW			10	–	0.02	–	0.00010	0.02	–	1.2	–	0.2	–	0.00010	0.2	–	2.8	
P_D = (18 mW/MHz) f = 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	1	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	1	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time** (C to Q)	1	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (6.0 ns/pF) C_L + 10 ns			5.0	–	–	–	100	300	–	–	–	–	–	100	350	–	–	
t_{PLH} = (2.4 ns/pF) C_L + 4.0 ns			10	–	–	–	40	110	–	–	–	–	–	40	125	–	–	
t_{PLH} = (1.8 ns/pF) C_L + 3.0 ns			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Turn-On Delay Time** (C to Q)	1	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (6.5 ns/pF) C_L + 27 ns			5.0	–	–	–	125	300	–	–	–	–	–	125	350	–	–	
t_{PHL} = (2.6 ns/pF) C_L + 11 ns			10	–	–	–	50	110	–	–	–	–	–	50	125	–	–	
t_{PHL} = (2.0 ns/pF) C_L + 10 ns			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Setup Times	1	$t_{setup\ H}$, $t_{setup\ L}$	5.0	–	–	60	40	–	–	–	–	–	120	40	–	–	–	ns
			10	–	–	20	10	–	–	–	–	–	30	10	–	–	–	
			15	–	–	–	7.5	–	–	–	–	–	–	7.5	–	–	–	
Clock Pulse Widths	1	PW_{CH}, PW_{CL}	5.0	–	–	200	125	–	–	–	–	–	500	125	–	–	–	ns
(C_L = 15 pF)			10	–	–	80	50	–	–	–	–	–	100	50	–	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Clock Pulse Frequency	1	PRF																MHz
(C_L = 15 pF)			5.0	–	–	–	4.0	2.5	–	–	–	–	–	4.0	1.0	–	–	
			10	–	–	–	10	7.0	–	–	–	–	–	10	5.0	–	–	
			15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	
Clock Pulse Rise and Fall Times	–	t_r, t_f	5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	μs
			10	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Turn-Off Delay Time (S to Q)	2	t_{PLH}																ns
(C_L = 15 pF)			5.0	–	–	–	90	300	–	–	–	–	–	90	350	–	–	
			10	–	–	–	18	110	–	–	–	–	–	18	125	–	–	
			15	–	–	–	14	–	–	–	–	–	–	14	–	–	–	
Turn-On Delay Time (R to Q)	2	t_{PHL}																ns
(C_L = 15 pF)			5.0	–	–	–	120	300	–	–	–	–	–	120	350	–	–	
			10	–	–	–	30	110	–	–	–	–	–	30	125	–	–	
			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Set and Reset Pulse Widths	2	PW_S, PW_R																ns
(C_L = 15 pF)			5.0	–	–	250	125	–	–	–	–	–	500	125	–	–	–	
			10	–	–	100	50	–	–	–	–	–	125	50	–	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

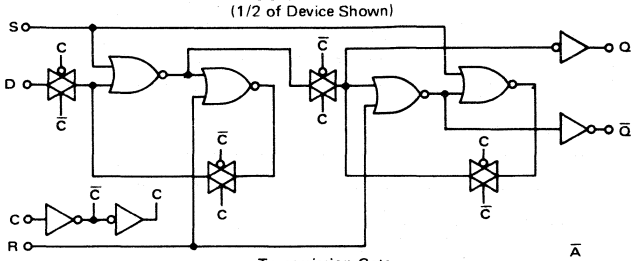
†For dissipation at different external load capacitances refer to corresponding formula:

$P_D(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$

Where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

Dynamic Power dissipation tested under worst case 0-1-0-1 pattern with 15 pF loads on all four outputs

LOGIC DIAGRAM
(1/2 of Device Shown)



Transmission Gate

A	CHARACTERISTICS
0	Bidirectional Open Circuit
1	Bidirectional Short-Circuit

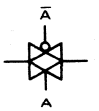


FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS
(Data, Clock, and Output)

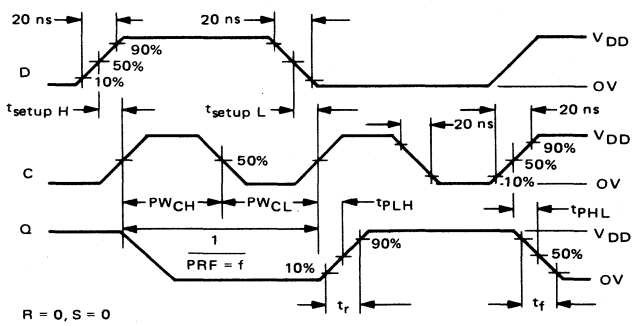
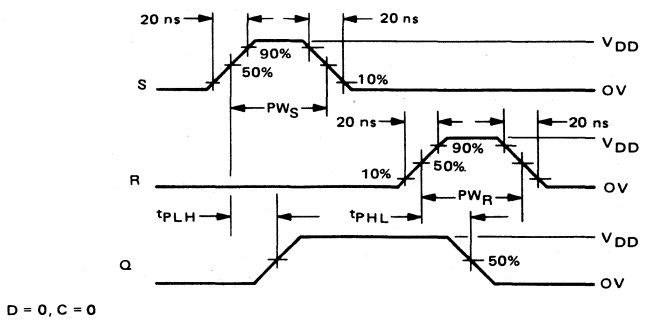


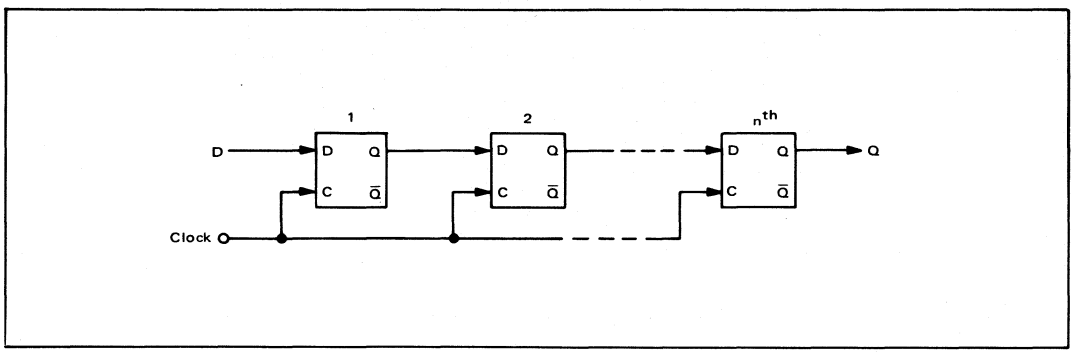
FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, and Output)



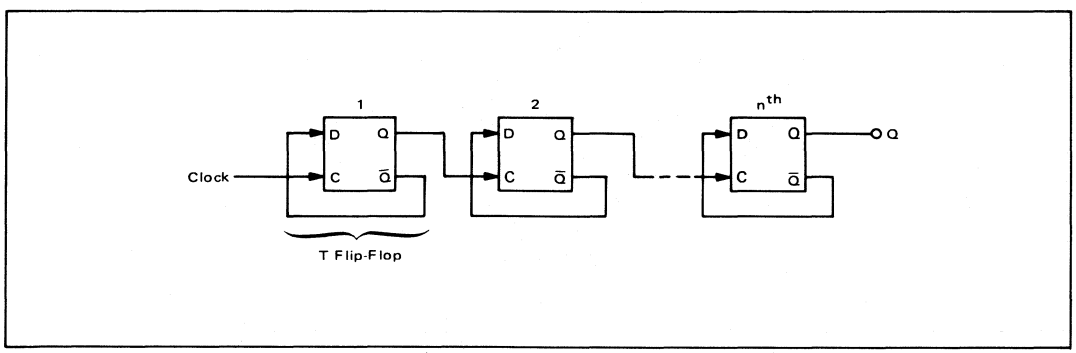
7

APPLICATIONS

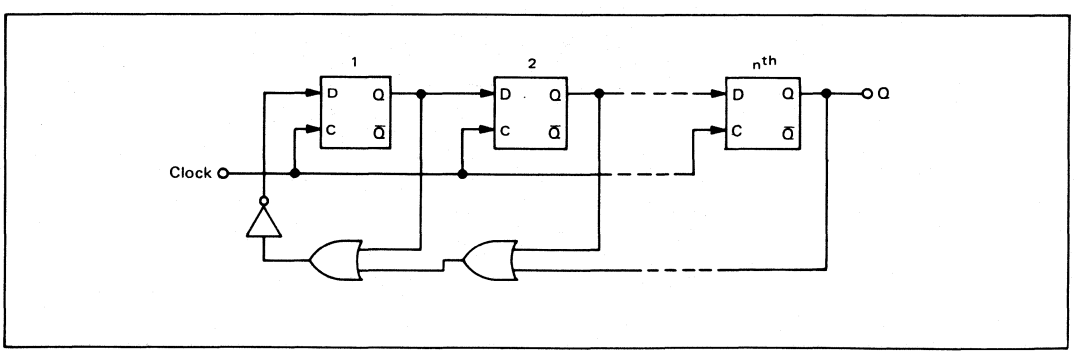
n-STAGE SHIFT REGISTER



BINARY RIPPLE UP-COUNTER (Divide-by-2^n)



MODIFIED RING COUNTER (Divide-by-(n + 1))



7

MC14015AL
MC14015CL
MC14015CP

DUAL 4-BIT STATIC SHIFT REGISTER

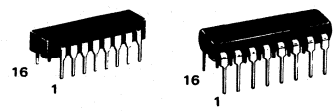
The MC14015 dual 4-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of two identical, independent 4-stage serial-input/parallel-output registers. Each register has independent Clock and Reset inputs with a single serial Data input. The register stages are type D master-slave flip-flops. Data is shifted from one stage to the next during the positive-going clock transition. Each register can be cleared when a high level is applied on the Reset line. These complementary MOS shift registers find primary use in buffer storage and serial-to-parallel conversion where low power dissipation and/or noise immunity is desired.

- Quiescent Power Dissipation = 0.5 μW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14015AL)
  = 3.0 Vdc to 16 Vdc (MC14015CL/CP)
- Single Supply Operation — Positive or Negative
- High Fanout — >50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance — 5.0 pF typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance — 750 ohms typical
- Toggle Rate = 6.0 MHz
- Logic Edge-Clocked Flip-Flop Design —
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14014AL MC14015CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14015AL —MC14015CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLES

CLOCKED OPERATION (SYNCHRONOUS)

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

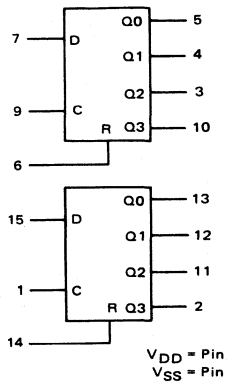
$Q_{n+1} = D_n$, R = 0

DIRECT OPERATION (ASYNCHRONOUS)

R	Q
0	Q
1	0

C = D = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14015AL							MC14015CL/CP							Unit
					-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
					Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*																			
($V_{out} \geq 3.5$ Vdc)			V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \leq 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current																			
(V_{OH} = 2.5 Vdc)	Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	–	–	mAdc
(V_{OH} = 9.5 Vdc)				10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	–	–	mAdc
(V_{OL} = 0.5 Vdc)				10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	–	–	
Input Current			I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)			C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF)		3	P_D																μW
				5.0	–	25	–	2.5	25	–	1500	–	250	–	2.5	250	–	3500	
				10	–	100	–	10	100	–	6000	–	1000	–	10	1000	–	14000	
Output Rise Time (C_L = 15 pF)		4	t_r																ns
				5.0	–	–	–	125	300	–	–	–	–	–	125	400	–	–	
				10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
Output Fall Time (C_L = 15 pF)		4	t_f																ns
				5.0	–	–	–	125	300	–	–	–	–	–	125	400	–	–	
				10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	

(Continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14015AL							MC14015CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Turn-On Delay Time (C_L = 15 pF)	4	t_{PHL}																ns
			5.0	–	–	–	300	750	–	–	–	–	–	300	1000	–	–	
			10	–	–	–	125	225	–	–	–	–	–	125	300	–	–	
Turn-Off Delay Time (C_L = 15 pF)	4	t_{PLH}																ns
			5.0	–	–	–	300	750	–	–	–	–	–	300	750	–	–	
			10	–	–	–	125	225	–	–	–	–	–	125	225	–	–	
Clock Pulse Width (C_L = 15 pF)	4	PW_C																ns
			5.0	–	–	400	300	–	–	–	–	–	500	300	–	–	–	
			10	–	–	175	75	–	–	–	–	–	200	75	–	–	–	
Clock Pulse Frequency	4	PRF																MHz
			5.0	–	–	1.5	2.0	–	–	–	–	–	1.0	2.0	–	–	–	
			10	–	–	3.0	6.0	–	–	–	–	–	2.5	6.0	–	–	–	
Clock Pulse Rise and Fall Times (C_L = 15 pF)	4	t_r, t_f																µs
			5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
			15	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
Set and Reset Propagation Delay Times (C_L = 15 pF)	–	t_{PHL}, t_{PLH}																ns
			5.0	–	–	–	500	750	–	–	–	–	–	500	1000	–	–	
			10	–	–	–	125	225	–	–	–	–	–	125	300	–	–	
Set and Reset Pulse Width (C_L = 15 pF)	–	$PW_{S,R}$																ns
			5.0	–	–	400	100	–	–	–	–	–	500	100	–	–	–	
			10	–	–	100	50	–	–	–	–	–	125	50	–	–	–	
Setup Time (C_L = 15 pF)	5	t_{setup}																ns
			5.0	–	–	–	100	350	–	–	–	–	–	100	500	–	–	
			10	–	–	–	50	80	–	–	–	–	–	50	100	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

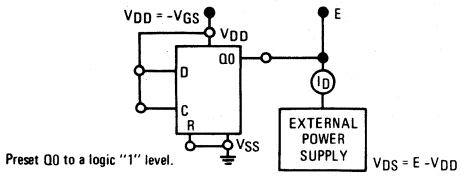
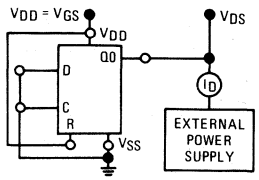
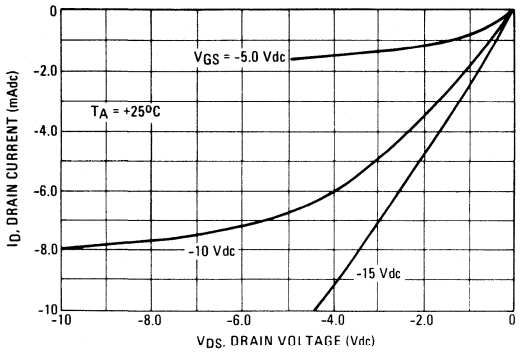


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS





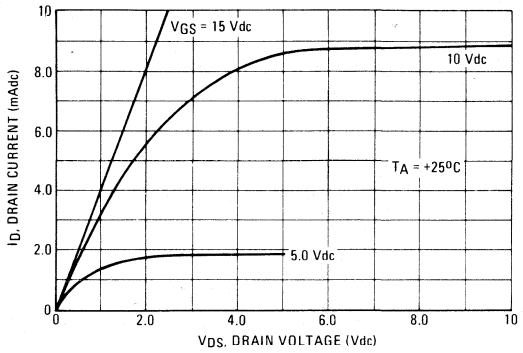


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

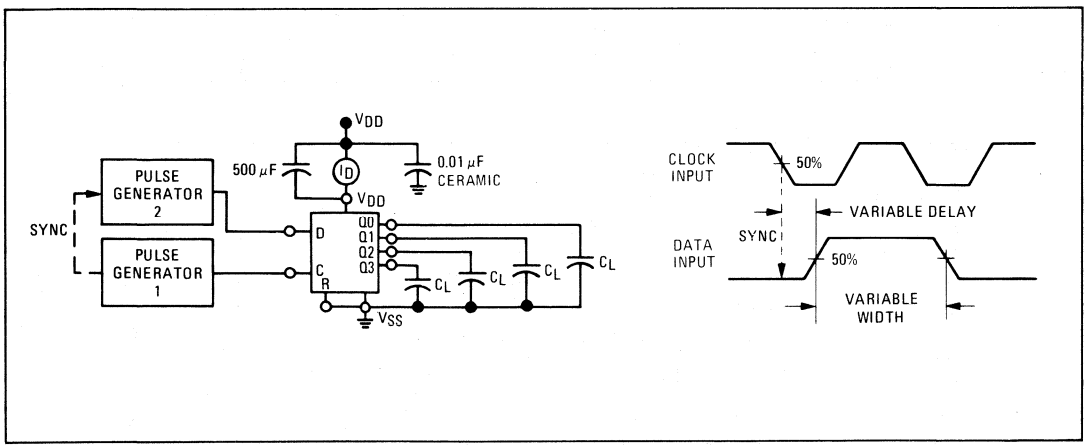


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

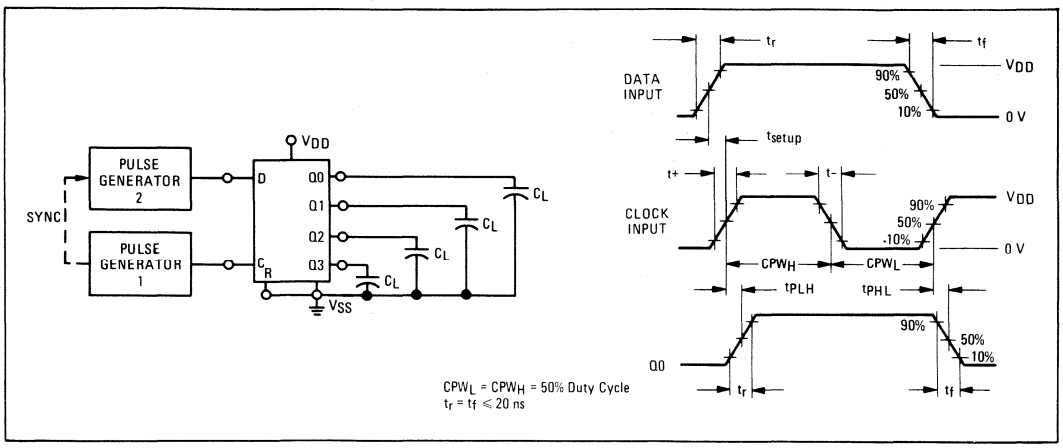
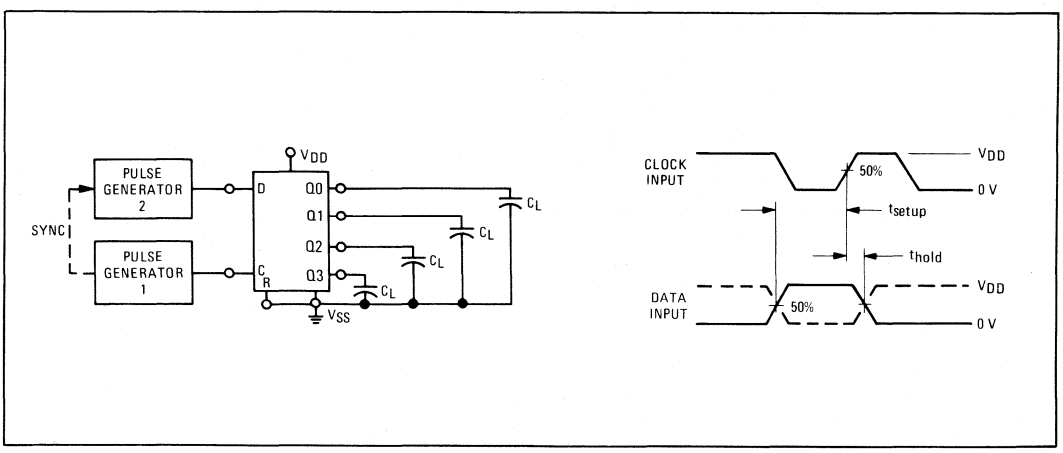
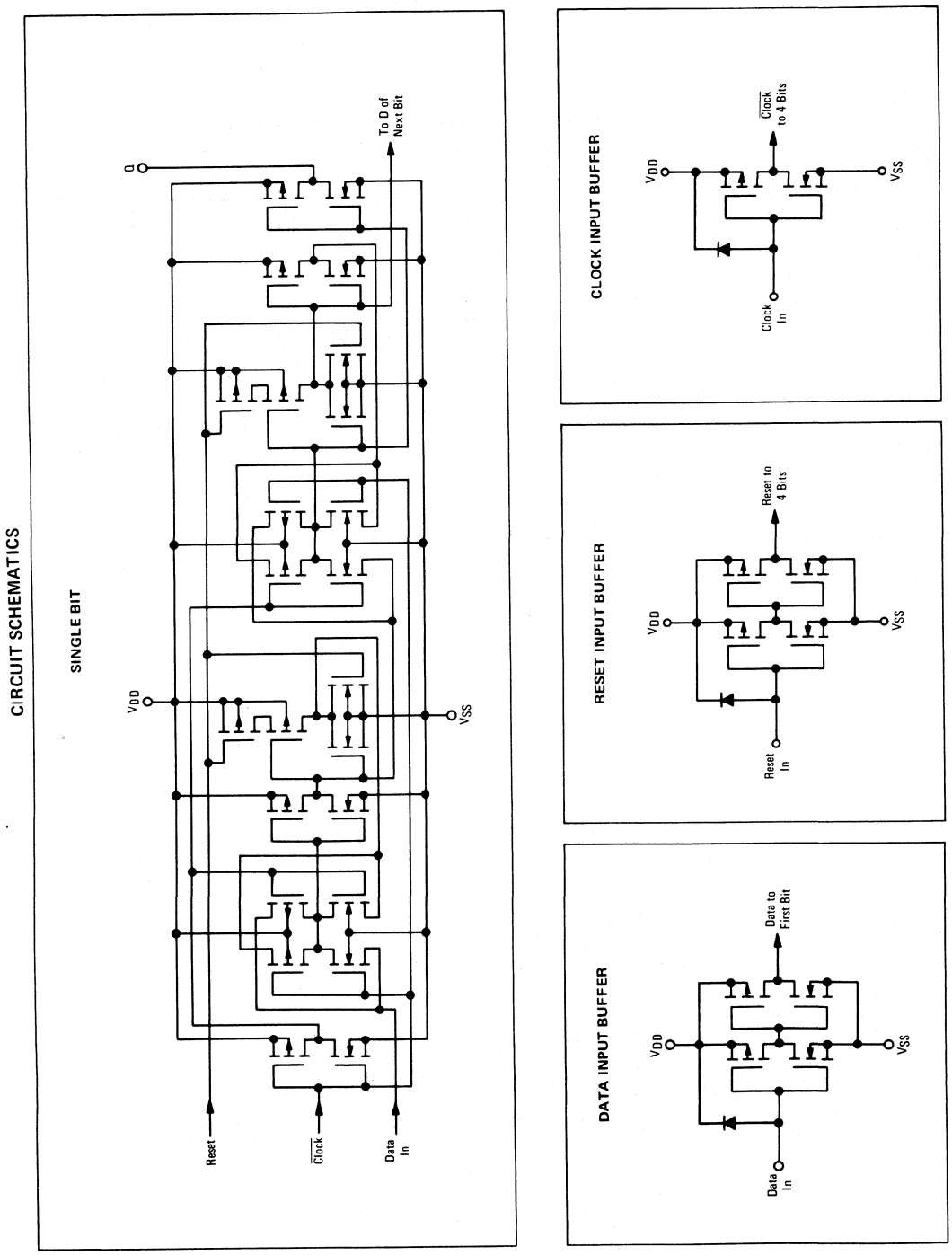


FIGURE 5 – SETUP AND HOLD TIME TEST CIRCUIT AND WAVEFORMS

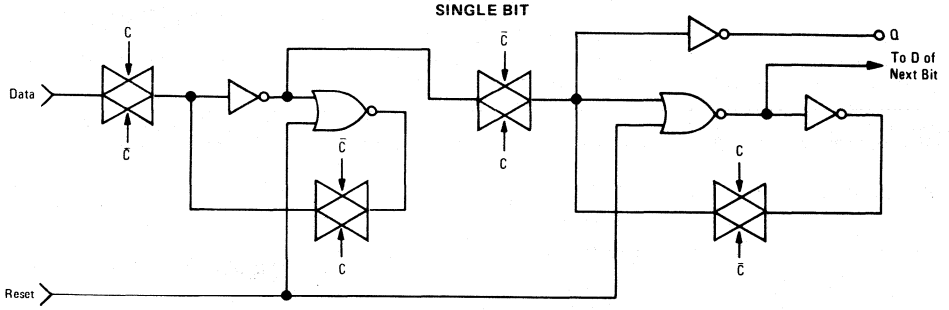


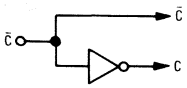
7


CIRCUIT SCHEMATICS
SINGLE BIT
Q
To D of Next Bit
VDD
VSS
Reset
Clock
Data In
CLOCK INPUT BUFFER
VDD
VSS
Clock to 4 Bits
Clock In
RESET INPUT BUFFER
VDD
VSS
Reset to 4 Bits
Reset In
DATA INPUT BUFFER
VDD
VSS
Data to First Bit
Data In

LOGIC DIAGRAMS

SINGLE BIT



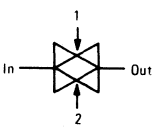


Input to Output is:

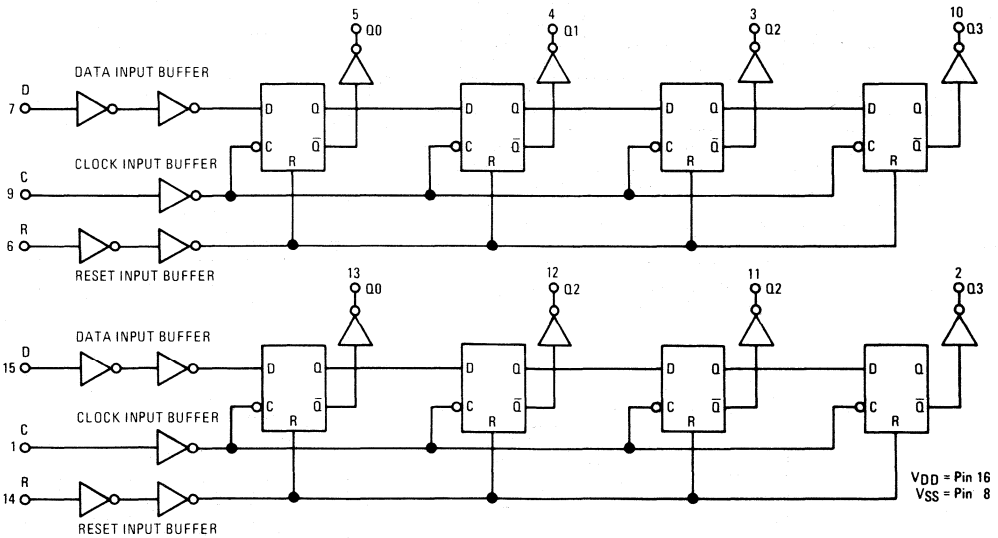
(a) A bidirectional short circuit when control input 1 is "Low" and control input 2 is "High".

(b) An open circuit when control input 1 is "High" and control input 2 is "Low".

T_G = Transmission Gate



COMPLETE DEVICE



7

MC14016AL
MC14016CL
MC14016CP

ANALOG SWITCH/MULTIPLEXER

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

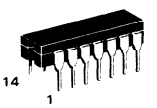
The MC14016 quad bilateral switch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each MC10416 consists of four independent switches capable of controlling either digital or analog signals. The quad bilateral switch is used in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

- High On/Off Output Voltage Ratio – 65 dB typical
- Quiescent Power Dissipation = 0.1 μW/package typical
- Low Crosstalk Between Switches – 80 dB typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14016AL)
  = 3.0 Vdc to 16 Vdc (MC14016CL/CP)
- Transmits Frequencies Up to 50 MHz
- Linearized Transfer Characteristics, $\Delta R_{ON} < 60\ \Omega$ for $V_{in} = V_{DD}$ to V_{SS}
- Low Noise – 12 nV/$\sqrt{\text{Cycle}}$, f ≥ 1 kHz typical
- Pin-for-Pin Replacement for CD4016A

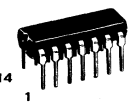
McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD ANALOG SWITCH
QUAD MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 632



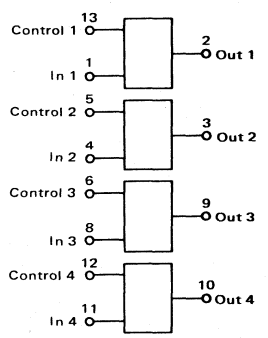
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14016AL – MC14016CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage		V_C V_{in}	V_{DD} to -0.5 V_{DD} to V_{SS}	Vdc Vdc
Output Voltage		V_{out}	V_{DD} to V_{SS}	Vdc
Operating Temperature Range	– MC14016AL – MC14016CL,CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

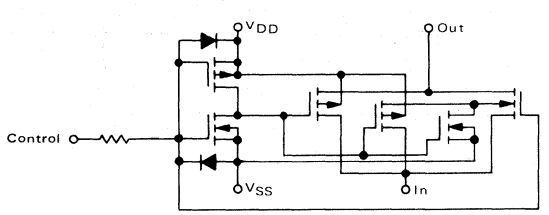
This device contains circuitry to protect the control inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq V_{in}$ or $V_{out} \leq V_{DD}$.

BLOCK DIAGRAM

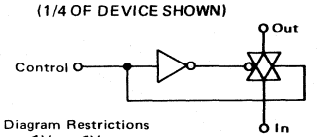


V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)



LOGIC DIAGRAM
(1/4 OF DEVICE SHOWN)



Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} < V_{out} \leq V_{DD}$

$V_{control}$	V_{in} to V_{out} Resistance
V_{SS}	$>10^9$ Ohms typ
V_{DD}	3×10^2 Ohms typ

7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	MC14016AL -55°C Min	MC14016AL -55°C Max	MC14016AL +25°C Min	MC14016AL +25°C Typ	MC14016AL +25°C Max	MC14016AL +125°C Min	MC14016AL +125°C Max	MC14016CL/CP -40°C Min	MC14016CL/CP -40°C Max	MC14016CL/CP +25°C Min	MC14016CL/CP +25°C Typ	MC14016CL/CP +25°C Max	MC14016CL/CP +85°C Min	MC14016CL/CP +85°C Max	Unit
Output Voltage "0" Level	1	V_{out}	0.0	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			0.0	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																			
(V_{out} = 3.5 Vdc)	2	V_{NL}	0.0	5.0	–	–	0.9	1.5	–	–	–	–	–	0.9	1.5	–	–	–	Vdc
(V_{out} = 7.0 Vdc)				10	–	–	0.9	1.5	–	–	–	–	–	0.9	1.5	–	–	–	
(V_{out} = 10.5 Vdc)				15	–	–	–	1.5	–	–	–	–	–	–	1.5	–	–	–	
(V_{out} = 1.5 Vdc)		V_{NH}	0.0	5.0	–	–	2.0	3.0	–	–	–	–	–	2.0	3.0	–	–	–	Vdc
(V_{out} = 3.0 Vdc)				10	–	–	6.0	8.0	–	–	–	–	–	6.0	8.0	–	–	–	
(V_{out} = 4.5 Vdc)				15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	
Output Drive Current	3	I_{OH}	0.0																mAdc
(V_{OH} = 2.5 Vdc) P-Channel				5.0	-0.9	–	-0.7	-2.5	–	-0.5	–	-0.7	–	-0.5	-2.5	–	-0.3	–	
(V_{OH} = 9.5 Vdc)				10	-0.8	–	-0.7	-1.9	–	-0.5	–	-0.8	–	-0.5	-1.9	–	-0.4	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-5.8	–	–	–	–	–	–	-5.8	–	–	–	
(V_{OL} = 0.4 Vdc) N-Channel		I_{OL}		5.0	0.18	–	0.15	0.4	–	0.13	–	0.12	–	0.15	0.4	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)				10	0.8	–	0.7	1.9	–	0.5	–	0.7	–	0.6	1.9	–	0.4	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	5.8	–	–	–	–	–	–	5.8	–	–	–	
Input Current (Control Input)	–	I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance	–	C_{in}	0.0																pF
Control				–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Switch Input				–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Switch Output				–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Feed Through				–	–	–	–	0.2	–	–	–	–	–	–	0.2	–	–	–	
Quiescent Dissipation	4,5																		
(C_L = 15 pF, f = 0)		P_Q	–	5.0	–	5.0	–	0.1	5.0	–	300	–	5.0	–	0.1	25	–	80	µW
				10	–	10	–	0.2	10	–	600	–	10	–	0.2	50	–	–	
				15	–	–	–	0.4	–	–	–	–	–	–	0.4	–	–	–	
Total Dissipation																			
(C_L = 15 pF)†	4,5	P_D	–	5.0	P_D = (0.10 mW/MHz) f + 0.0005 mW														mW
				10	P_D = (0.45 mW/MHz) f + 0.002 mW														
				15	P_D = (0.9 mW/MHz) f + 0.006 mW														
"ON" Resistance	6,7,12	R_{ON}																	ohms
(V_C = V_{DD}, R_L = 10 kΩ)																			
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	600	–	300	660	–	960	–	610	–	300	660	–	840	
(V_{in} = -5.0 Vdc)					–	600	–	300	660	–	960	–	610	–	300	660	–	840	
(V_{in} = ±0.25 Vdc)					–	600	–	280	660	–	960	–	610	–	280	660	–	840	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	360	–	240	400	–	600	–	370	–	240	400	–	520	
(V_{in} = -7.5 Vdc)					–	360	–	240	400	–	600	–	370	–	240	400	–	520	
(V_{in} = ±0.25 Vdc)					–	360	–	180	400	–	600	–	370	–	180	400	–	520	
(V_{in} = +10 Vdc)			0	10	–	600	–	260	660	–	960	–	610	–	260	660	–	840	
(V_{in} = +0.25 Vdc)					–	600	–	260	660	–	960	–	610	–	260	660	–	840	
(V_{in} = +5.6 Vdc)					–	600	–	310	660	–	960	–	610	–	310	660	–	840	
(V_{in} = +15 Vdc)			0	15	–	360	–	260	400	–	600	–	370	–	260	400	–	520	
(V_{in} = +0.25 Vdc)					–	360	–	260	400	–	600	–	370	–	260	400	–	520	
(V_{in} = +9.3 Vdc)					–	360	–	300	400	–	600	–	370	–	300	400	–	520	
Δ "ON" Resistance	–	ΔR_{ON}																	ohms
Between any 2 of 4 circuits in a common package																			
(V_C = V_{DD}, V_{in} = ±5.0 Vdc)			-5.0	5.0	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
(V_C = V_{DD}, V_{in} = ±7.5 Vdc)			-7.5	7.5	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
V_{in} to V_{out} Propagation Delay Time	8	t_{PLH},	0.0	5.0	–	–	–	15	30	–	–	–	–	–	15	45	–	–	ns
(V_C = V_{DD}, C_L = 15 pF,		t_{PHL}		10	–	–	–	7.0	10	–	–	–	–	–	7.0	15	–	–	
R_L = 1.0 kΩ)				15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Turn-On Delay Time, Control to Output	9	t_{PHL},	0.0	5.0	–	–	–	25	60	–	–	–	–	–	30	90	–	–	ns
(V_{in} ≤ 10 Vdc, C_L = 15 pF,		t_{PLH}		10	–	–	–	16	30	–	–	–	–	–	16	30	–	–	
R_L = 1.0 kΩ)				15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Crosstalk, Control to Output	10	–	0.0																mV
(V_C = V_{DD}, C_L = 15 pF,				5.0	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
R_{in} = 1.0 kΩ, R_{out} = 10 kΩ)				10	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
				15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Crosstalk between any two switches	–	–	–	5.0	–	–	–	-80	–	–	–	–	–	–	-80	–	–	–	dB
(R_L = 1.0 kΩ, f = 1.0 MHz, crosstalk = $20\log_{10}\frac{V_{out1}}{V_{out2}}$)																			
Maximum Control Input Pulse Frequency	–	–	0.0																MHz
(C_L = 15 pF, R_L = 1.0 kΩ)				5.0	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
				10	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
				15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level before producing an output state change.

(Continued on next page)

NOTE: All unused control inputs must be returned to V_{DD} or V_{SS} as appropriate for the circuit application.

†For dissipation at different external load capacitances refer to corresponding formula:

$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{pF}) V_{DD}{}^2 f$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc and f in MHz.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{SS} Vdc	V_{DD} Vdc	MC14016AL −55°C Min	MC14016AL −55°C Max	MC14016AL +25°C Min	MC14016AL +25°C Typ	MC14016AL +25°C Max	MC14016AL +125°C Min	MC14016AL +125°C Max	MC14016CL/CP −40°C Min	MC14016CL/CP −40°C Max	MC14016CL/CP +25°C Min	MC14016CL/CP +25°C Typ	MC14016CL/CP +25°C Max	MC14016CL/CP +85°C Min	MC14016CL/CP +85°C Max	Unit
Noise Voltage ($V_C = V_{DD}$, f = 100 Hz)	11,15	–	0.0	5.0	–	–	–	24	–	–	–	–	–	–	24	–	–	–	$nV/\sqrt{cycle}$
				10	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
				15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
($V_C = V_{DD}$, f = 100 kHz)				5.0	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
				10	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Sine Wave (Distortion) (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	14	–	-5.0	5.0	–	–	–	0.16	–	–	–	–	–	–	0.16	–	–	–	%
Input/Output Leakage Current ($V_C = V_{SS}$)	–	–																	nA
(V_{in} = +5.0 Vdc)			-5.0	5.0	–	–	–	±0.001	125	–	–	–	–	–	±0.001	125	–	–	
(V_{in} = -5.0 Vdc)			-5.0	5.0	–	–	–	+0.001	125	–	–	–	–	–	+0.001	125	–	–	
(V_{in} = +7.5 Vdc)			-7.5	7.5	–	–	–	±100	–	–	–	–	–	–	±100	–	–	–	pA
(V_{in} = -7.5 Vdc)			-7.5	7.5	–	–	–	±100	–	–	–	–	–	–	±100	–	–	–	
Insertion Loss ($V_C = V_{DD}$, V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz, $I_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$)	13,14	–	-5.0	5.0															dB
R_L = 1.0 kΩ					–	–	–	2.3	–	–	–	–	–	–	2.3	–	–	–	
R_L = 10 kΩ					–	–	–	0.2	–	–	–	–	–	–	0.2	–	–	–	
R_L = 100 kΩ					–	–	–	0.1	–	–	–	–	–	–	0.1	–	–	–	
R_L = 1.0 MΩ					–	–	–	0.05	–	–	–	–	–	–	0.05	–	–	–	
Bandwidth (-3 dB) ($V_C = V_{DD}$, V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc)	13,14	BW	-5.0	5.0															MHz
R_L = 1.0 kΩ					–	–	–	54	–	–	–	–	–	–	54	–	–	–	
R_L = 10 kΩ					–	–	–	40	–	–	–	–	–	–	40	–	–	–	
R_L = 100 kΩ					–	–	–	38	–	–	–	–	–	–	38	–	–	–	
R_L = 1.0 MΩ					–	–	–	37	–	–	–	–	–	–	37	–	–	–	
Feedthrough ($V_C = V_{SS}$, $20 \log_{10} \frac{V_{out}}{V_{in}}$ = -50 dB)	14	–	-5.0	5.0															kHz
R_L = 1.0 kΩ					–	–	–	1250	–	–	–	–	–	–	1250	–	–	–	
R_L = 10 kΩ					–	–	–	140	–	–	–	–	–	–	140	–	–	–	
R_L = 100 kΩ					–	–	–	18	–	–	–	–	–	–	18	–	–	–	
R_L = 1.0 MΩ					–	–	–	2.0	–	–	–	–	–	–	2.0	–	–	–	

FIGURE 1 – OUTPUT VOLTAGE TEST CIRCUIT

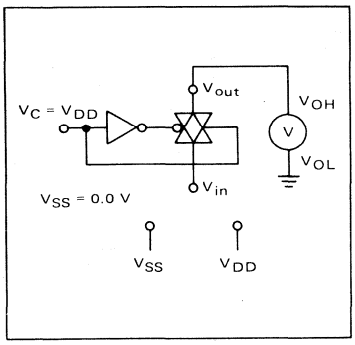
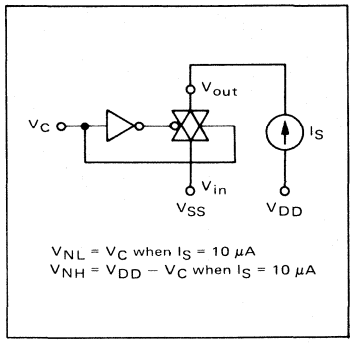
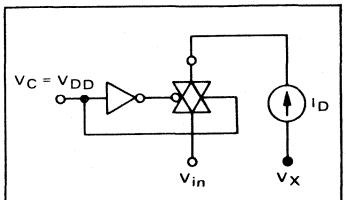


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT



$V_{NL} = V_C$ when I_S = 10 μA
$V_{NH} = V_{DD} - V_C$ when I_S = 10 μA

FIGURE 3 – OUTPUT DRIVER CURRENT TEST CIRCUIT



Measurement	V_{in}	V_X
P-Channel	V_{DD}	V_{out}
N-Channel	V_{SS}	V_{out}

7

FIGURE 4 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

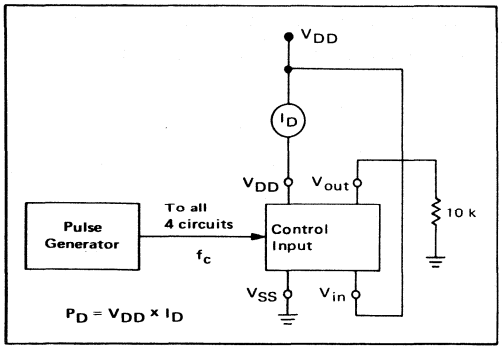
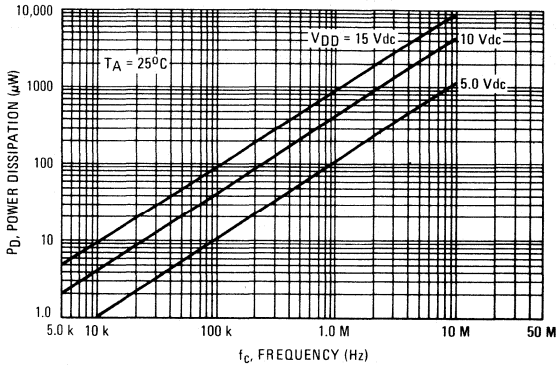


FIGURE 5 – TYPICAL POWER DISSIPATION PER CIRCUIT (1/4 OF DEVICE SHOWN)



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 6 – V_{SS} = -5.0 V and -7.5 V

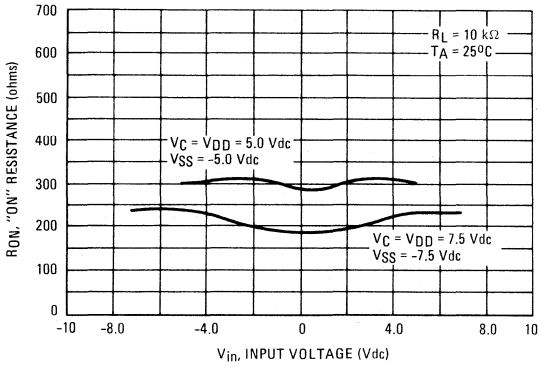


FIGURE 7 – V_{SS} = 0 V

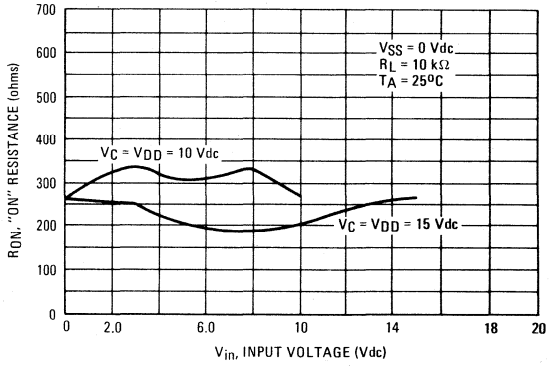


FIGURE 8 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

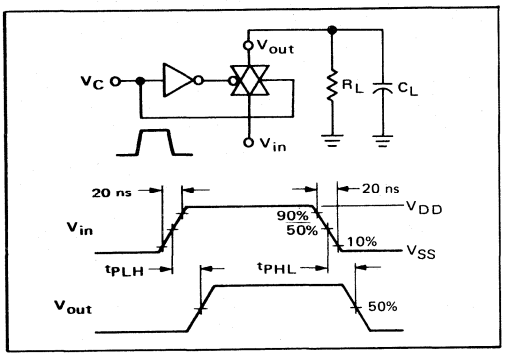


FIGURE 9 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

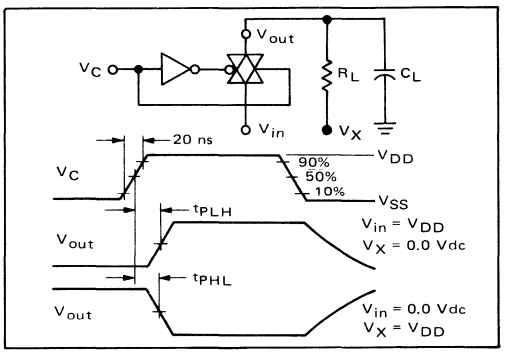


FIGURE 10 – CROSSTALK TEST CIRCUIT

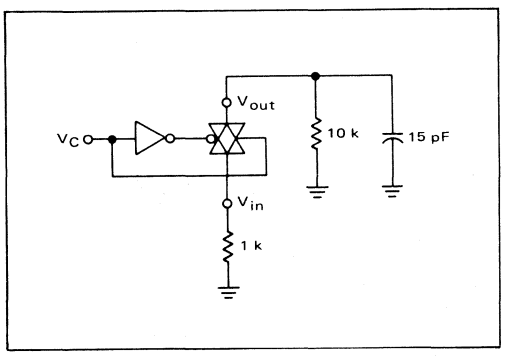
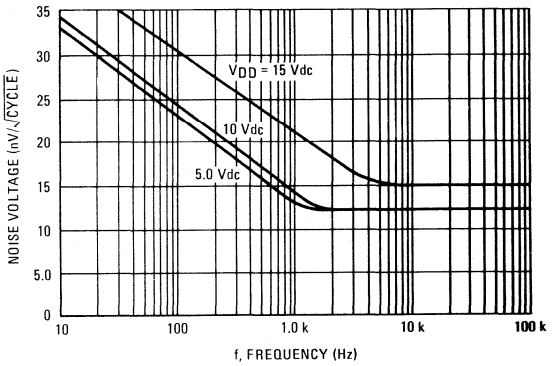


FIGURE 11 – TYPICAL NOISE CHARACTERISTICS



7

FIGURE 12 – R_{ON} CHARACTERISTICS TEST CIRCUIT

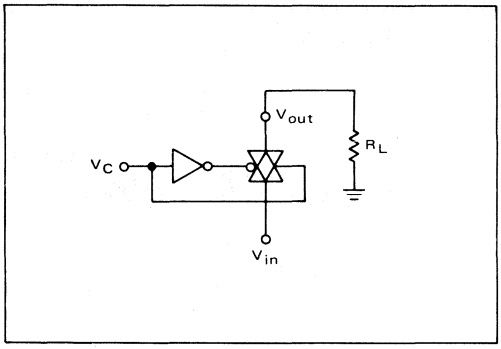


FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS

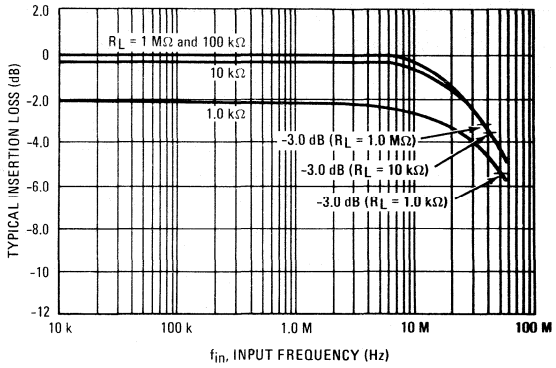


FIGURE 14 – FREQUENCY RESPONSE TEST CIRCUIT

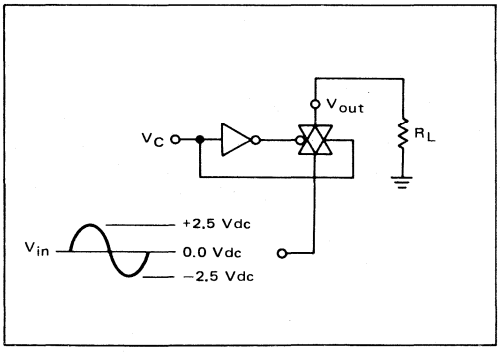
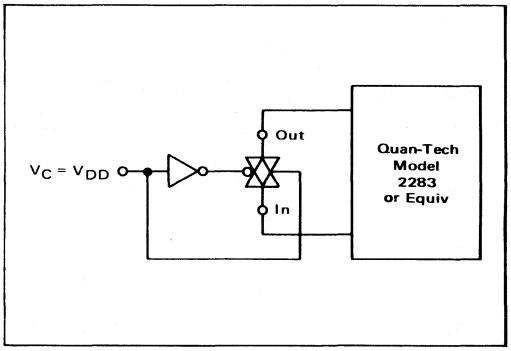


FIGURE 15 – NOISE VOLTAGE TEST CIRCUIT



MC14017AL
MC14017CL
MC14017CP

DECADE COUNTER/DIVIDER

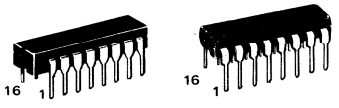
The MC14017 is a five-stage Johnson decade counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Replacement for CD4017A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DECADE COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14017AL — MC14017CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14017AL — MC14017CL/CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

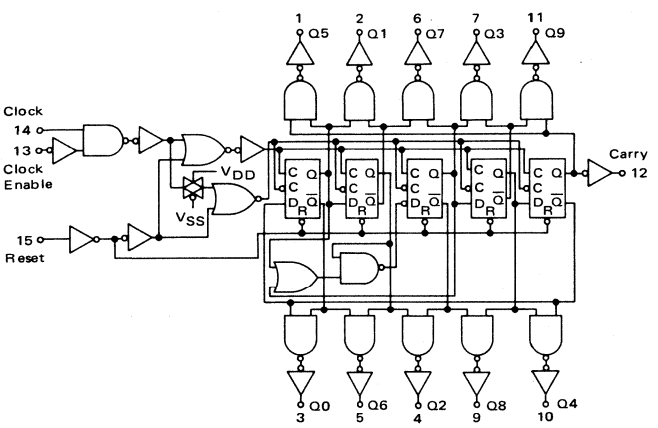
FUNCTIONAL TRUTH TABLE

(Positive Logic)

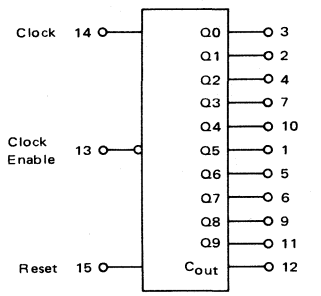
CLOCK	CLOCK ENABLE	RESET	DECODE OUTPUT = n
0	X	0	n
X	1	0	n
X	X	1	Q0
⌐	0	0	n+1
⌐	X	0	n
X	⌐	0	n
1	⌐	0	n+1

X = Don't Care If n <5 Carry = "1", Otherwise = "0"

LOGIC DIAGRAM



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

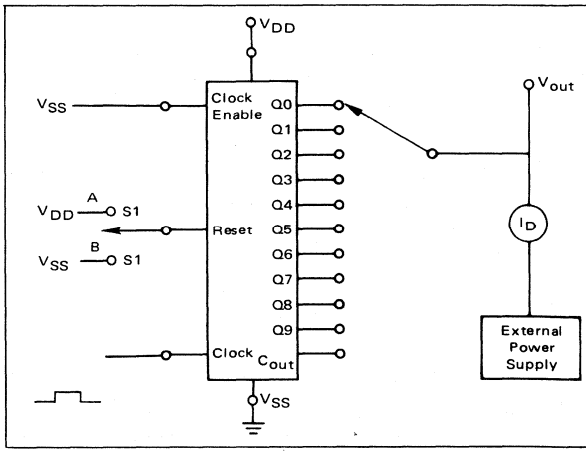
See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14017AL -55°C Min	MC14017AL -55°C Max	MC14017AL +25°C Min	MC14017AL +25°C Typ	MC14017AL +25°C Max	MC14017AL +125°C Min	MC14017AL +125°C Max	MC14017CL/CP -40°C Min	MC14017CL/CP -40°C Max	MC14017CL/CP +25°C Min	MC14017CL/CP +25°C Typ	MC14017CL/CP +25°C Max	MC14017CL/CP +85°C Min	MC14017CL/CP +85°C Max	Unit
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.95	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.95	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF)	2	P_D																mW
P_D = (0.7 mW/MHz) f + 0.0015 mW			5.0	–	0.025	–	0.0015	0.025	–	1.5	–	0.25	–	0.0025	0.25	–	3.5	
P_D = (2.2 mW/MHz) f + 0.005 mW			10	–	0.10	–	0.005	0.10	–	6.0	–	1.0	–	0.01	1.0	–	14	
P_D = (4.36 mW/MHz) f + 0.01 mW			15	–	–	–	0.01	–	–	–	–	–	–	0.02	–	–	–	
Output Rise and Fall Time	3	t_r, t_f																ns
(C_L = 15 pF)																		
t_r, t_f = (4.8 ns/pF) C_L + 28 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (2.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (2.2 ns/pF) C_L + 2.0 ns			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
*Turn-On, Turn-Off Delay Time	3	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Reset to Decode Output																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 420 ns			5.0	–	–	–	450	800	–	–	–	–	–	450	1200	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 186.5 ns			10	–	–	–	200	400	–	–	–	–	–	200	500	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 109.5 ns			15	–	–	–	120	–	–	–	–	–	–	120	–	–	–	
Turn-On, Turn-Off Delay Time	3	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Clock to C_{out}																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 320 ns			5.0	–	–	–	350	550	–	–	–	–	–	350	700	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 111 ns			10	–	–	–	125	250	–	–	–	–	–	125	300	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 74.5 ns			15	–	–	–	85	–	–	–	–	–	–	85	–	–	–	
Turn-On, Turn-Off Delay Time	3	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Clock to Decode Output																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 455 ns			5.0	–	–	–	485	730	–	–	–	–	–	485	940	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 166.5 ns			10	–	–	–	180	360	–	–	–	–	–	180	400	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 114.5 ns			15	–	–	–	125	–	–	–	–	–	–	125	–	–	–	

*The clock input has an improved noise immunity of typically 60% of V_{DD} from either input level.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



	OUTPUT SINK DRIVE	OUTPUT SOURCE DRIVE
DECODE OUTPUTS	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14017AL -55°C Min	MC14017AL -55°C Max	MC14017AL +25°C Min	MC14017AL +25°C Typ	MC14017AL +25°C Max	MC14017AL +125°C Min	MC14017AL +125°C Max	MC14017CL/CP -40°C Min	MC14017CL/CP -40°C Max	MC14017CL/CP +25°C Min	MC14017CL/CP +25°C Typ	MC14017CL/CP +25°C Max	MC14017CL/CP +85°C Min	MC14017CL/CP +85°C Max	Unit
Turn-Off Delay Time (C_L = 15 pF) Reset to C_{out}	3	t_{PLH}	5.0	–	–	–	350	750	–	–	–	–	–	350	1000	–	–	ns
t_{PLH} = (2.0 ns/pF)C_L + 320 ns			10	–	–	–	125	250	–	–	–	–	–	125	300	–	–	
t_{PLH} = (0.9 ns/pF)C_L + 111.5 ns			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
t_{PLH} = (0.7 ns/pF)C_L + 69.5 ns																		
Minimum Clock Pulse Width Ncp = Pcp	3	PW_C	5.0	–	–	–	100	200	–	–	–	–	–	100	250	–	–	ns
			10	–	–	–	42	70	–	–	–	–	–	42	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Maximum Clock Frequency	3	PRF	5.0	–	–	2.5	5.0	–	–	–	–	–	2.0	5.0	–	–	–	MHz
			10	–	–	7.0	12	–	–	–	–	–	5.0	12	–	–	–	
			15	–	–	–	16	–	–	–	–	–	–	16	–	–	–	
Minimum Reset Pulse Width	3	PW_R	5.0	–	–	–	200	330	–	–	–	–	–	200	500	–	–	ns
			10	–	–	–	100	165	–	–	–	–	–	100	250	–	–	
			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Reset Removal Time	3	t_{rem}	5.0	–	–	–	300	500	–	–	–	–	–	300	750	–	–	ns
			10	–	–	–	100	200	–	–	–	–	–	100	275	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Maximum Clock Input Rise and Fall Time (C_L = 15 pF)	3	t_r,t_f	5.0	No Maximum Limit							–	–	–	∞	100	–	–	µs
			10								–	–	–	∞	100	–	–	
			15								–	–	–	∞	–	–	–	
Clock Enable Setup Time (C_L = 15 pF)	3	t_{setup}	5.0	–	–	–	175	300	–	–	–	–	–	175	700	–	–	ns
			10	–	–	–	75	150	–	–	–	–	–	75	300	–	–	
			15	–	–	–	52	–	–	–	–	–	–	52	–	–	–	
Clock Enable Release Time (C_L = 15 pF)	3	t_{rel}	5.0	–	–	–	260	405	–	–	–	–	–	260	700	–	–	ns
			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	

NOTE: All unused inputs should be returned to either V_{DD} or V_{SS} as appropriate for circuit application.

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT

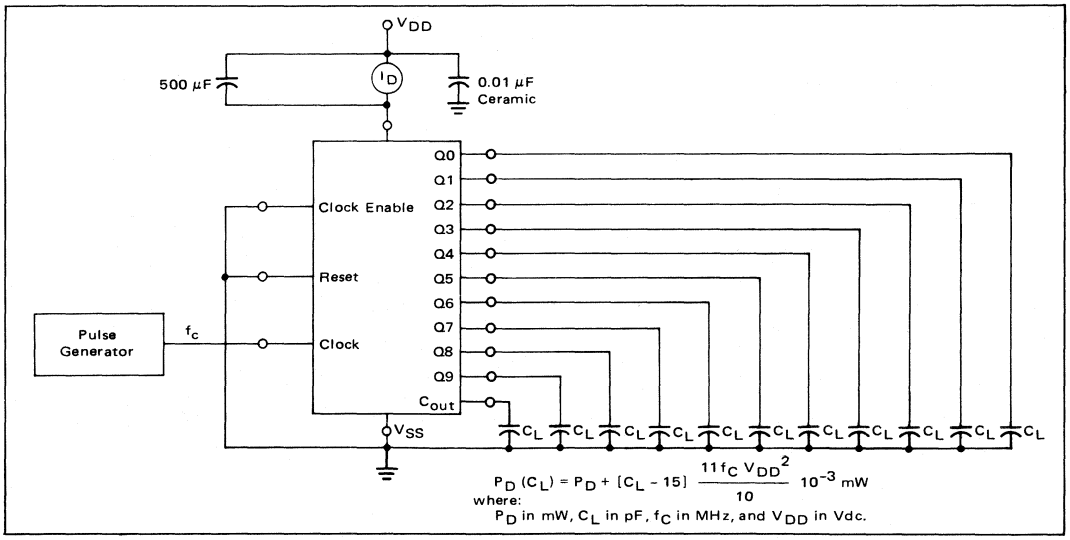
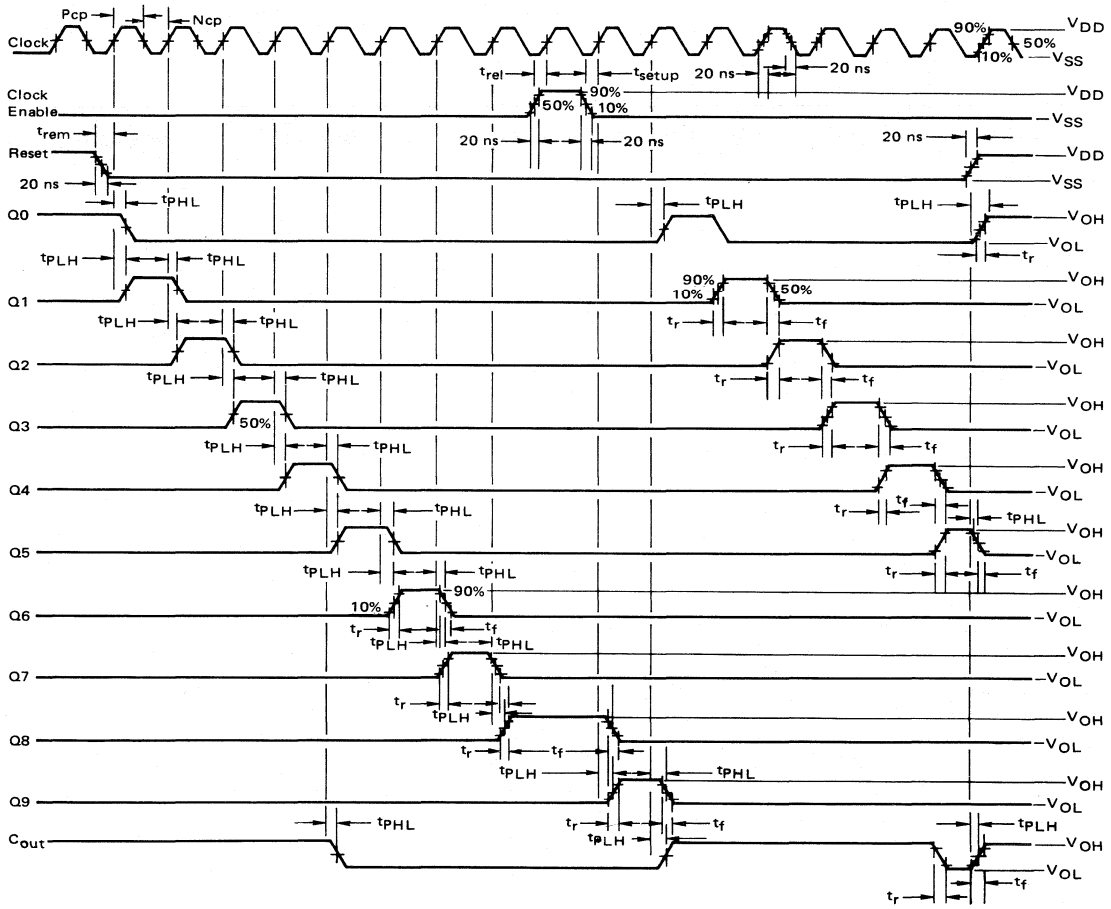


FIGURE 3 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14020AL
MC14020CL
MC14020CP

Advance Information

14-BIT BINARY COUNTER

The MC14020 14-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 14 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-dividing circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50nW/package typical @ V_{DD} = 5.0V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14020AL)
  = 3.0 Vdc to 16 Vdc (MC14020CL/CP)
- Low Input Capacitance = 5.0pF typical
- Buffered Outputs Available from stages 1 and 4 thru 14
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15V
- Pin-for-Pin Replacement for CD4020A

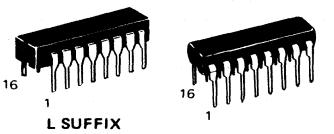
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14020AL MC14020CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14020AL – MC14020CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

McMOS

(LOW-POWER COMPLEMENTARY MOS)

14-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

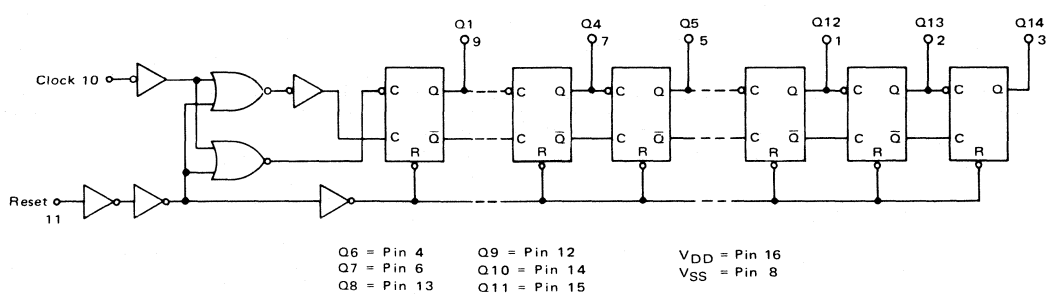
CLOCK	RESET	OUTPUT STATE
⌐	0	No Change
¬	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

LOGIC DIAGRAM



Q6 = Pin 4
Q7 = Pin 6
Q8 = Pin 13

Q9 = Pin 12
Q10 = Pin 14
Q11 = Pin 15

V_{DD} = Pin 16
V_{SS} = Pin 8

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14020AL -55°C Min	MC14020AL -55°C Max	MC14020AL +25°C Min	MC14020AL +25°C Typ	MC14020AL +25°C Max	MC14020AL +125°C Min	MC14020AL +125°C Max	MC14020CL/CP -40°C Min	MC14020CL/CP -40°C Max	MC14020CL/CP +25°C Min	MC14020CL/CP +25°C Typ	MC14020CL/CP +25°C Max	MC14020CL/CP +85°C Min	MC14020CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																
$V_{out} \geq 3.5$ Vdc			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
$V_{out} \geq 7.0$ Vdc			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
$V_{out} \geq 10.5$ Vdc			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
$V_{out} \leq 1.5$ Vdc		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
$V_{out} \leq 3.0$ Vdc			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
$V_{out} \leq 4.5$ Vdc			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source	–		5.0	-0.62	–	-0.5	-1.7	–	-0.35	–	-0.23	–	-0.2	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.0	–	0.65	–	0.6	–	0.5	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**†	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (1.2 mW/MHz) f + 0.00005 mW			5.0	–	0.025	–	0.00005	0.025	–	1.5	–	0.25	–	0.00005	0.25	–	3.5	
P_D = (5.0 mW/MHz) f + 0.0002 mW			10	–	0.10	–	0.0002	0.10	–	6.0	–	1.0	–	0.0002	1.0	–	14	
P_D = (13.5 mW/MHz) f + 0.005 mW			15	–	–	–	0.0005	–	–	–	–	–	–	0.0005	–	–	–	
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 35 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 57 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock Turn-On, Turn-Off Delay Time**	2	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF)																		
Clock to Q1																		
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 324 ns			5.0	–	–	–	350	600	–	–	–	–	–	350	650	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 130 ns			10	–	–	–	140	225	–	–	–	–	–	140	250	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 92 ns			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Clock to Q14																		
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 2774 ns			5.0	–	–	–	2.8	5.6	–	–	–	–	–	2.8	8.4	–	–	µs
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 990 ns			10	–	–	–	1.0	2.0	–	–	–	–	–	1.0	3.0	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 592 ns			15	–	–	–	0.6	–	–	–	–	–	–	0.6	–	–	–	
Reset Turn-On Delay Time**	–	t_{PHL}																ns
(C_L = 15 pF)																		
Reset on Q_n																		
t_{PHL} = (1.75 ns/pF) C_L + 514 ns			5.0	–	–	–	540	3000	–	–	–	–	–	540	3500	–	–	
t_{PHL} = (0.70 ns/pF) C_L + 190 ns			10	–	–	–	200	775	–	–	–	–	–	200	900	–	–	
t_{PHL} = (0.53 ns/pF) C_L + 152 ns			15	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
Minimum Clock Pulse Width	–	PW_C	5.0	–	–	–	140	335	–	–	–	–	–	140	500	–	–	ns
(C_L = 15 pF)			10	–	–	–	55	125	–	–	–	–	–	55	165	–	–	
			15	–	–	–	38	–	–	–	–	–	–	38	–	–	–	
Maximum Clock Pulse Frequency	–	PRF	5.0	–	–	1.5	3.5	–	–	–	–	–	1.0	3.5	–	–	–	MHz
(C_L = 15 pF)			10	–	–	4.0	9.0	–	–	–	–	–	3.0	9.0	–	–	–	
			15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	
Maximum Clock Rise and Fall Time	–	t_r, t_f	5.0	NO MAXIMUM LIMIT							–	–	–	∞	100	–	–	µs
(C_L = 15 pF)			10								–	–	–	∞	100	–	–	
			15								–	–	–	∞	–	–	–	
Minimum Reset Pulse Width	–	PW_R	5.0	–	–	–	320	2500	–	–	–	–	–	320	3000	–	–	ns
(C_L = 15 pF)			10	–	–	–	120	475	–	–	–	–	–	120	550	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_D(C_L) = P_D + 1 \times 10^{-3} (C_L - 15) V_{DD}^2 f$ where:

P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

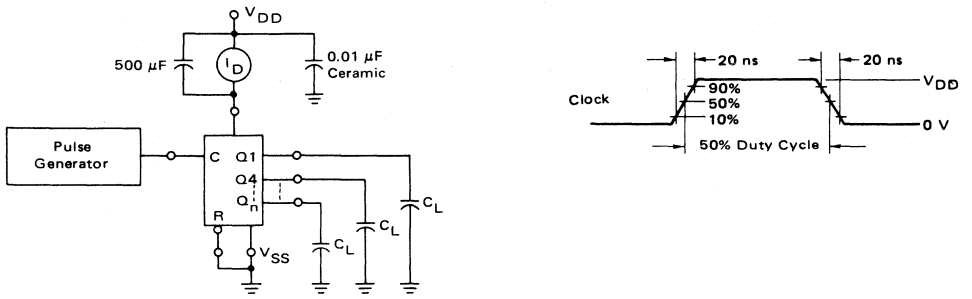


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

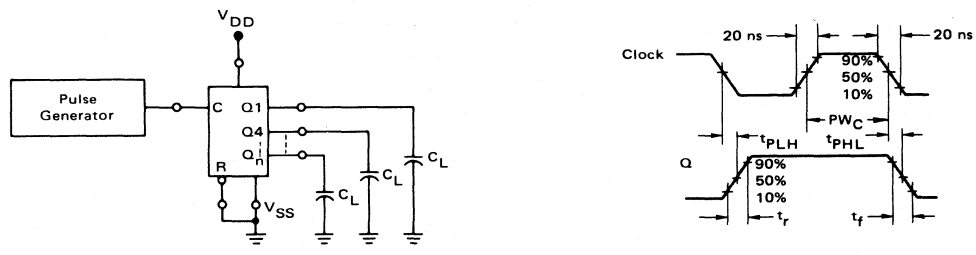
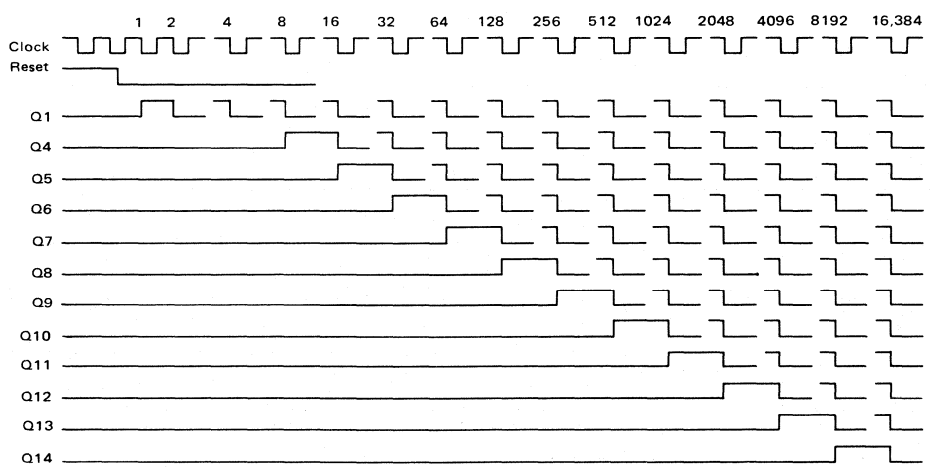


FIGURE 3 – TIMING DIAGRAM



7

MC14021AL
MC14021CL
MC14021CP

8-BIT STATIC SHIFT REGISTER

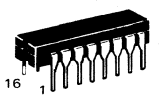
The MC14021 8-bit static shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This shift register finds primary use in parallel to serial data conversion, asynchronous parallel input, serial output data queueing; and other general purpose register applications requiring low power and/or high noise immunity

- Asynchronous Parallel Input/Serial Output
- Synchronous Serial Input/Serial Output
- Full Static Operation from DC to 7.0 MHz
- "Q" Outputs from Sixth, Seventh, and Eighth Stages
- Pin-for-Pin Replacement for CD4021A

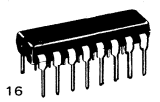
McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14021AL MC14021CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	—MC14021AL —MC14021CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.i., either V_{SS} or V_{DD}.

TRUTH TABLE

SERIAL OPERATION:

t	CLOCK	D_S	P/S	Q6 t = n+6	Q7 t = n+7	Q8 t = n+8
n	⌐⌐	0	0	0	?	?
n+1	⌐⌐	1	0	1	0	?
n+2	⌐⌐	0	0	0	1	0
n+3	⌐⌐	1	0	1	0	1
	⌐_	X	0	Q6	Q7	Q8

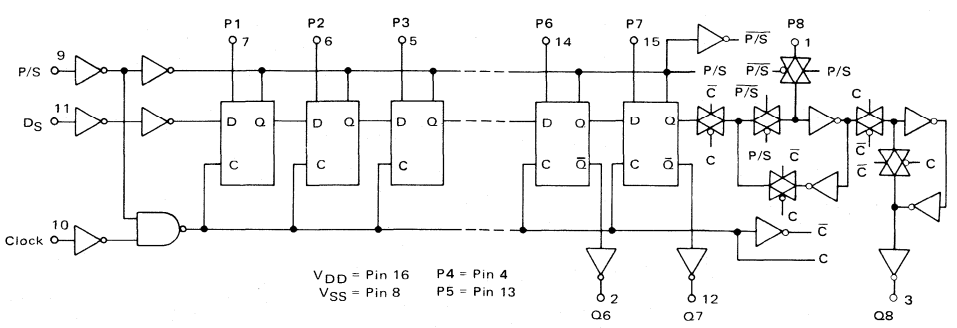
PARALLEL OPERATION:

CLOCK	D_S	P/S	D_m	$*Q_m$
X	X	1	0	0
X	X	1	1	1

*Q6, Q7, & Q8 are available externally

X = Don't Care

LOGIC DIAGRAM



See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14021AL −55°C Min	MC14021AL −55°C Max	MC14021AL +25°C Min	MC14021AL +25°C Typ	MC14021AL +25°C Max	MC14021AL +125°C Min	MC14021AL +125°C Max	MC14021CL/CP −40°C Min	MC14021CL/CP −40°C Max	MC14021CL/CP +25°C Min	MC14021CL/CP +25°C Typ	MC14021CL/CP +25°C Max	MC14021CL/CP +85°C Min	MC14021CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geqslant 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geqslant 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geqslant 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leqslant 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leqslant 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leqslant 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	-1.3	–	-0.35	–	-0.23	–	-0.20	-1.3	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.75	–	-0.35	–	-0.23	–	-0.20	-0.75	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.6	–	0.28	–	0.23	–	0.20	0.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	1.1	–	0.65	–	0.60	–	0.50	1.1	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.5	–	–	–	–	–	–	7.5	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF, f = 0 Hz)	1	P_Q																mW
			5.0	–	0.025	–	0.0015	0.025	–	1.5	–	0.25	–	0.0025	0.25	–	3.5	
			10	–	0.1	–	0.005	0.1	–	6.0	–	1.0	–	0.01	1.0	–	14	
			15	–	–	–	0.01	–	–	–	–	–	–	0.02	–	–	–	
Total Power Dissipation† (C_L = 15 pF)	–	P_D	5.0	P_D = (1.2 mW/MHz) f + 0.0015 mW														mW
			10	P_D = (10.1 mW/MHz) f + 0.005 mW														
			15	P_D = (12.1 mW/MHz) f + 0.01 mW														
Output Rise Time (C_L = 15 pF)	2	t_r																ns
			5.0	–	–	–	100	300	–	–	–	–	–	100	400	–	–	
			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time (C_L = 15 pF)	2	t_r																ns
			5.0	–	–	–	100	300	–	–	–	–	–	100	200	–	–	
			10	–	–	–	50	125	–	–	–	–	–	50	110	–	–	
			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On, Turn-Off Delay Time (C_L = 15 pF)	2	t_{PHL}, t_{PLH}																ns
			5.0	–	–	–	200	750	–	–	–	–	–	200	1000	–	–	
			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Clock Pulse Width (C_L = 15 pF)	2	PW_C																ns
			5.0	–	–	–	150	400	–	–	–	–	–	150	500	–	–	
			10	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Clock Pulse Frequency (C_L = 15 pF)	2	PRF																MHz
			5.0	–	–	1.5	3.0	–	–	–	–	–	1.0	3.0	–	–	–	
			10	–	–	3.0	7.0	–	–	–	–	–	2.5	7.0	–	–	–	
			15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
Clock Pulse Rise and Fall Time (C_L = 15 pF) V_{DD} = 5.0 to 15 Vdc)	2	t_r, t_f	–	–	–	15	–	–	–	–	–	–	15	–	–	–	–	μs
Parallel/Serial Control Pulse Width (C_L = 15 pF)	2	PW_H																ns
			5.0	–	–	–	150	400	–	–	–	–	–	150	500	–	–	
			10	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Setup Time (C_L = 15 pF)	2	t_{setup}																ns
			5.0	–	–	–	150	300	–	–	–	–	–	150	300	–	–	
			10	–	–	–	50	80	–	–	–	–	–	50	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

†For dissipation at different external load capacitances refer to corresponding formula:

$P_T(C_L) = P_D + 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

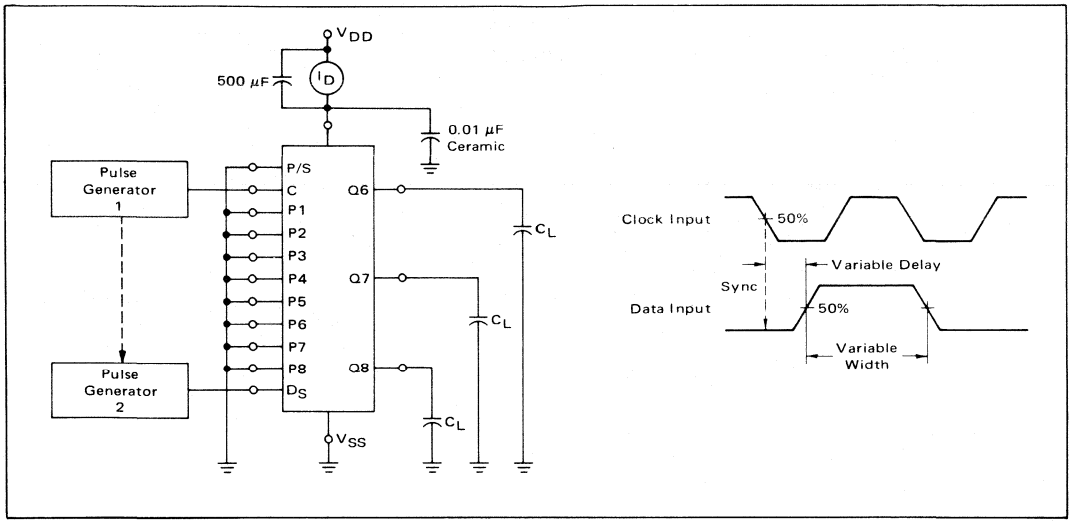
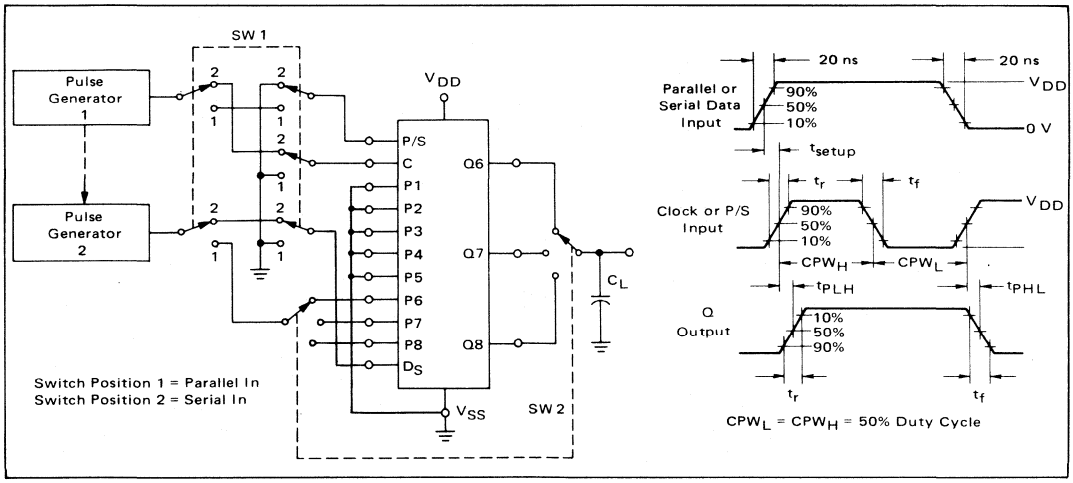


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14022AL
MC14022CL
MC14022CP

Advance Information

OCTAL COUNTER/DRIVER

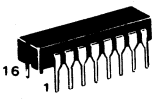
The MC14022 is a four-stage Johnson octal counter with built-in code converter. High-speed operation and spike-free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- 12 MHz (typical) Operation @ V_{DD} = 10 Vdc
- Divide-by-N Counting when used with MC14001 NOR Gate
- Pin-for-Pin Replacement for CD4022A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

OCTAL COUNTER/DIVIDER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14022AL — MC14022CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14022AL — MC14022CL/CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

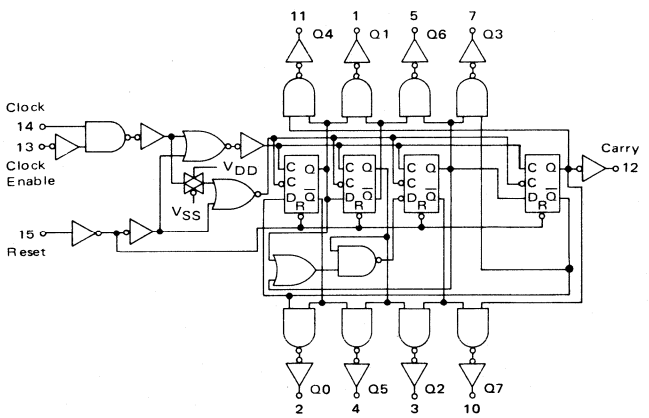
FUNCTIONAL TRUTH TABLE

(Positive Logic)

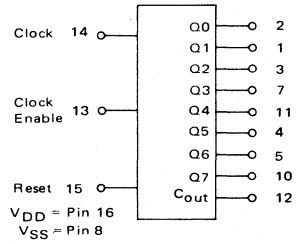
CLOCK	CLOCK ENABLE	RESET	OUTPUT = n
0	X	0	n
X	1	0	n
↗	0	0	n+1
↘	X	0	n
1	↘	0	n+1
X	↗	0	n
X	X	1	Q0

X = Don't Care If n≤4 Carry = 1, Otherwise = 0

LOGIC DIAGRAM



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

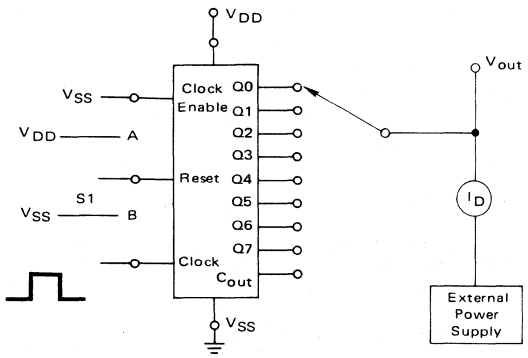
7

ELECTRICAL CHARACTERISTICS

Characteristic	Fig.	Symbol	V_{DD} Vdc	MC14022AL -55°C Min	MC14022AL -55°C Max	MC14022AL +25°C Min	MC14022AL +25°C Typ	MC14022AL +25°C Max	MC14022AL +125°C Min	MC14022AL +125°C Max	MC14022CL/CP -40°C Min	MC14022CL/CP -40°C Max	MC14022CL/CP +25°C Min	MC14022CL/CP +25°C Typ	MC14022CL/CP +25°C Max	MC14022CL/CP +80°C Min	MC14022CL/CP +80°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.95	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.95	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)	–	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-1.0	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	1	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF)**	2	P_D																mW
P_D = (0.58 mW/MHz) f + 0.0015 mW			5.0	–	0.025	–	0.0015	0.025	–	1.5	–	0.25	–	0.0025	0.25	–	3.5	
P_D = (1.8 mW/MHz) f + 0.005 mW			10	–	0.10	–	0.005	0.10	–	6.0	–	1.0	–	0.01	1.0	–	14	
P_D = (3.6 mW/MHz) f + 0.01 mW			15	–	–	–	0.01	–	–	–	–	–	–	0.02	–	–	–	
Output Rise and Fall Time**		t_r, t_f																ns
(C_L = 15 pF)																		
t_r, t_f = (4.8 ns/pF) C_L + 28 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (0.8 ns/pF) C_L + 8.0 ns			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Turn-On, Turn-Off Delay Time**		t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Reset to Decode Output																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 420 ns			5.0	–	–	–	450	800	–	–	–	–	–	450	1200	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 186.5 ns			10	–	–	–	200	400	–	–	–	–	–	200	500	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 109.5 ns			15	–	–	–	120	–	–	–	–	–	–	120	–	–	–	
Turn-On, Turn-Off Delay Time**		t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Clock to C_{out}																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 320 ns			5.0	–	–	–	350	550	–	–	–	–	–	350	700	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 111.5 ns			10	–	–	–	125	250	–	–	–	–	–	125	300	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 74.5 ns			15	–	–	–	85	–	–	–	–	–	–	85	–	–	–	
Turn-On, Turn-Off Delay Time**		t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) Clock to Decode Output																		
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L +455 ns			5.0	–	–	–	485	730	–	–	–	–	–	485	940	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 166.5 ns			10	–	–	–	180	360	–	–	–	–	–	180	400	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 114.4 ns			15	–	–	–	125	–	–	–	–	–	–	125	–	–	–	

*The clock input has an improved noise immunity of typically 60% of V_{DD} from either input level.
**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE AND OUTPUT SINK CHARACTERISTICS TEST CIRCUIT



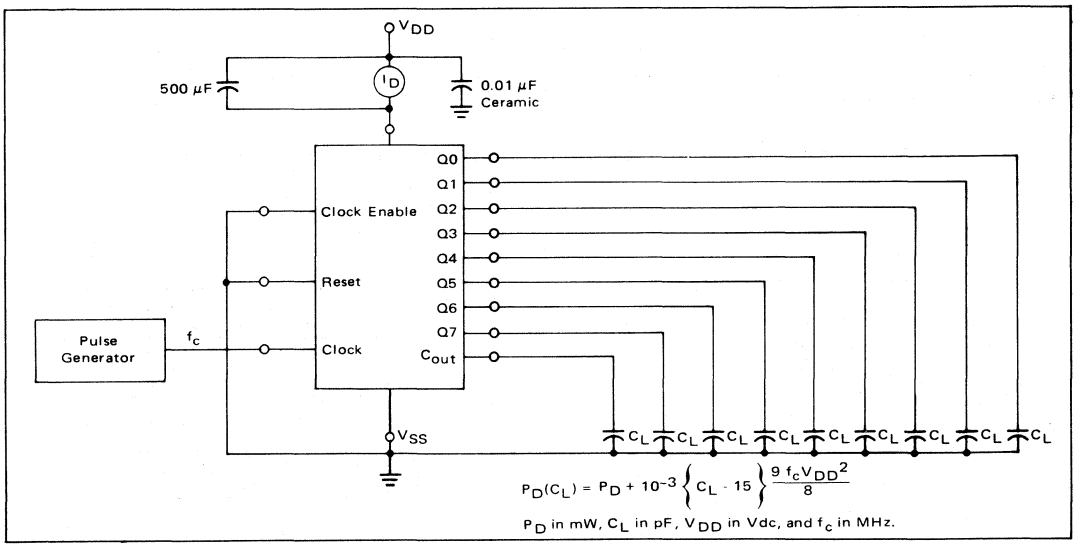
Outputs	Output Sink Drive (S1 to A)	Output Source Drive (S1 to B)
Carry	Clock to 5 thru 7 (S1 to B)	S1 to A
V_{GS} =	V_{DD}	$-V_{DD}$
V_{DS} =	V_{out}	$V_{out} - V_{DD}$

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Fig.	Symbol	V_{DD} Vdc	MC14022AL							MC14022CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Turn-Off Delay Time (C_L = 15 pF) Reset to C_{out}	3	t_{PLH}																ns
t_{PLH} = (2.0 ns/pF) C_L + 320 ns			5.0	–	–	–	350	750	–	–	–	–	–	350	1000	–	–	
t_{PLH} = (0.9 ns/pF) C_L + 111.5 ns			10	–	–	–	125	250	–	–	–	–	–	125	300	–	–	
t_{PLH} = (0.7 ns/pF) C_L + 69.5 ns			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Minimum Clock Pulse Width	3	PW_C																ns
			5.0	–	–	–	100	200	–	–	–	–	–	100	250	–	–	
			10	–	–	–	42	70	–	–	–	–	–	42	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Maximum Clock Frequency	3	PRF																MHz
			5.0	–	–	2.5	5.0	–	–	–	–	–	2.0	5.0	–	–	–	
			10	–	–	7.0	12	–	–	–	–	–	5.0	12	–	–	–	
			15	–	–	–	16	–	–	–	–	–	–	16	–	–	–	
Minimum Reset Pulse Width	3	PW_R																ns
			5.0	–	–	–	200	330	–	–	–	–	–	200	500	–	–	
			10	–	–	–	100	165	–	–	–	–	–	100	250	–	–	
			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Reset Removal Time	3	t_{rem}																ns
			5.0	–	–	–	300	500	–	–	–	–	–	300	750	–	–	
			10	–	–	–	100	200	–	–	–	–	–	100	275	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Maximum Clock Input Rise and Fall Time (C_L = 15 pF)	3	t_r, t_f	5.0	No Maximum Limit							–	–	–	∞	100			μs
			10								–	–	–	∞	100			
			15								–	–	–	∞	–			
Clock Enable Setup Time (C_L = 15 pF)	3	t_{setup}																ns
			5.0	–	–	–	175	300	–	–	–	–	–	175	700	–	–	
			10	–	–	–	75	150	–	–	–	–	–	75	300	–	–	
			15	–	–	–	52	–	–	–	–	–	–	52	–	–	–	
Clock Enable Release Time (C_L = 15 pF)	3	t_{rel}																ns
			5.0	–	–	–	260	405	–	–	–	–	–	260	700	–	–	
			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	

NOTE: All unused inputs should be returned to either V_{DD} or V_{SS} as appropriate for circuit application.

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



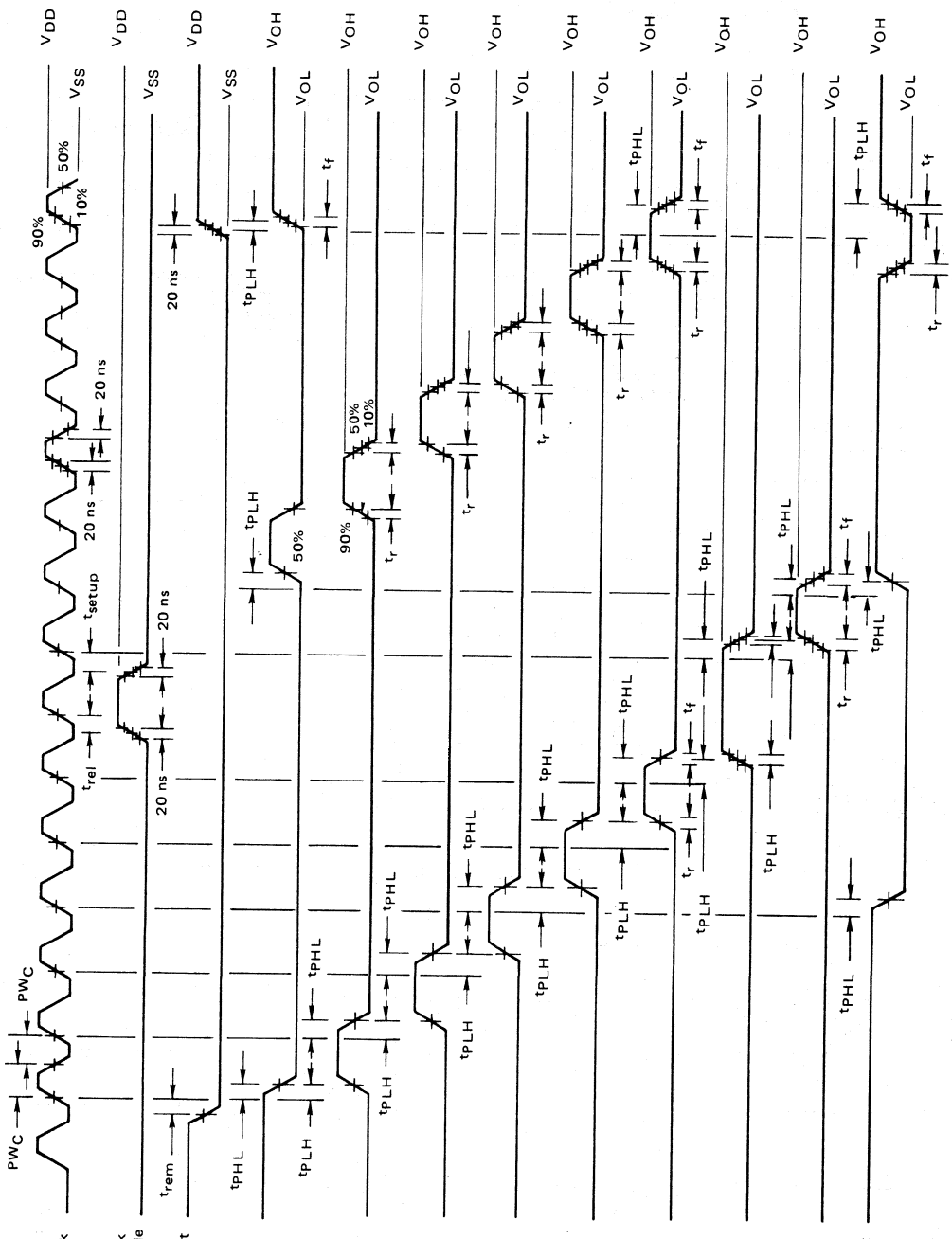


FIGURE 3 – AC MEASUREMENT DEFINITION AND FUNCTIONAL WAVEFORMS

MC14023AL
MC14023CL
MC14023CP

TRIPLE 3-INPUT "NAND" GATE

The MC14023 triple 3-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14023AL)
  = 3.0 Vdc to 16 Vdc (MC14023CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 750 ohms typical
- Pin-For-Pin Replacement for CD4023

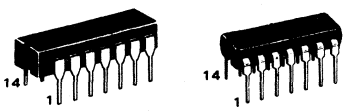
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14023AL MC14023CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14023AL –MC14023CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

McMOS

(LOW-POWER COMPLEMENTARY MOS)

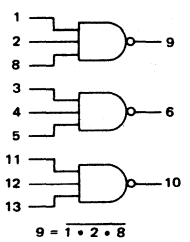
TRIPLE 3-INPUT "NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

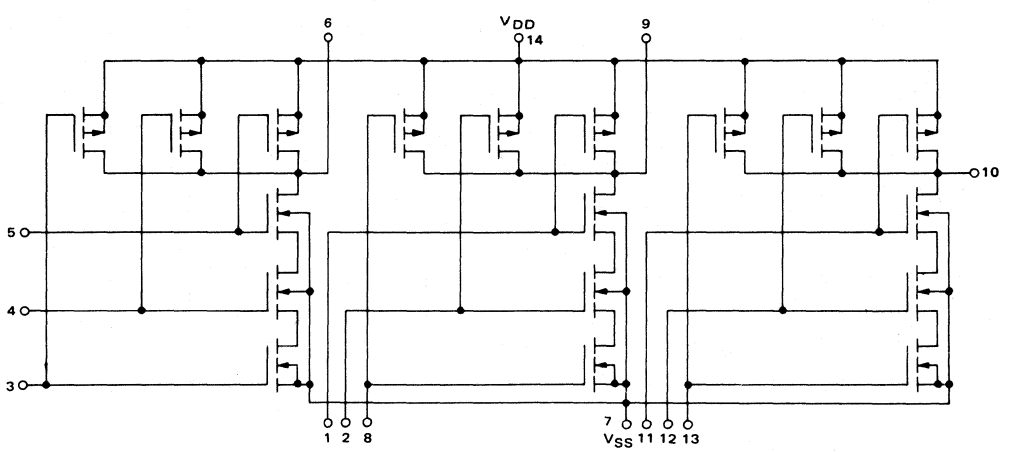
LOGIC DIAGRAM
(Positive Logic)



$9 = \overline{1 \cdot 2 \cdot 8}$

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC



See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14023AL							MC14023CL/CP							Unit
					-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
					Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	"0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*																			
($V_{out} \geq 3.5$ Vdc)			V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \leq 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current																			
(V_{OH} = 2.5 Vdc)	Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)				10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.26	–	mAdc
(V_{OL} = 0.5 Vdc)				10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current			I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)			C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		3	P_D																μW
				5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	
				10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
Output Rise Time (C_L = 15 pF)		4	t_r																ns
				5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Output Fall Time (C_L = 15 pF)		4	t_f																ns
				5.0	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
				10	–	–	–	25	75	–	–	–	–	–	25	110	–	–	
				15	–	–	–	14	–	–	–	–	–	–	14	–	–	–	
Turn-On Delay Time (C_L = 15 pF)		4	t_{PHL}																ns
				5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
				15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Turn-Off Delay Time (C_L = 15 pF)		4	t_{PLH}																ns
				5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	
				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

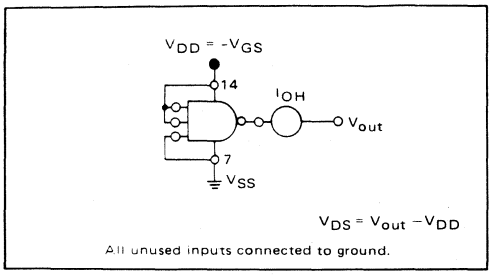
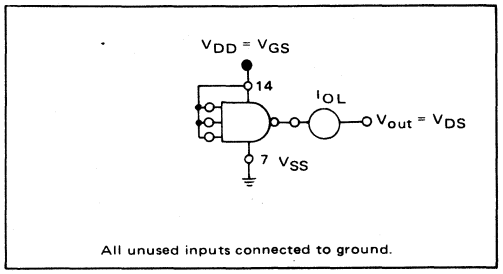
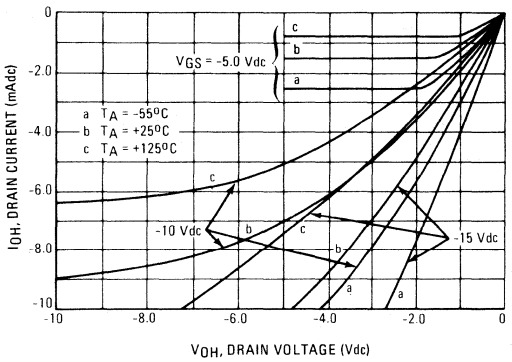


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS





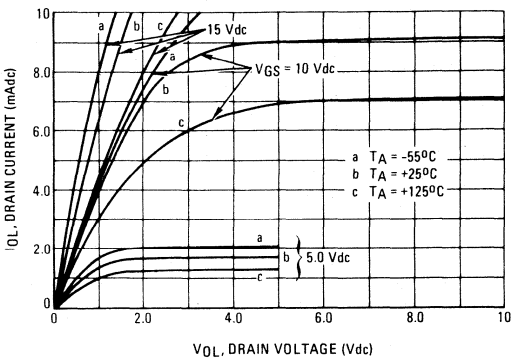


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

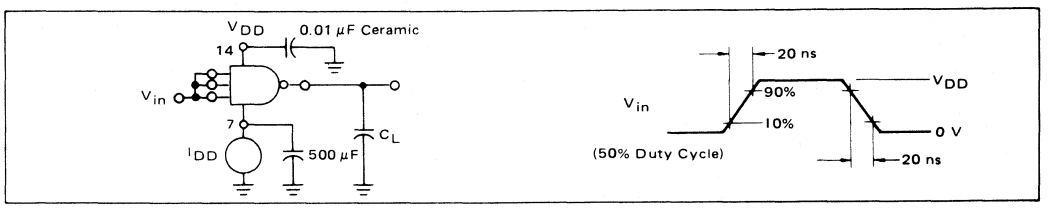
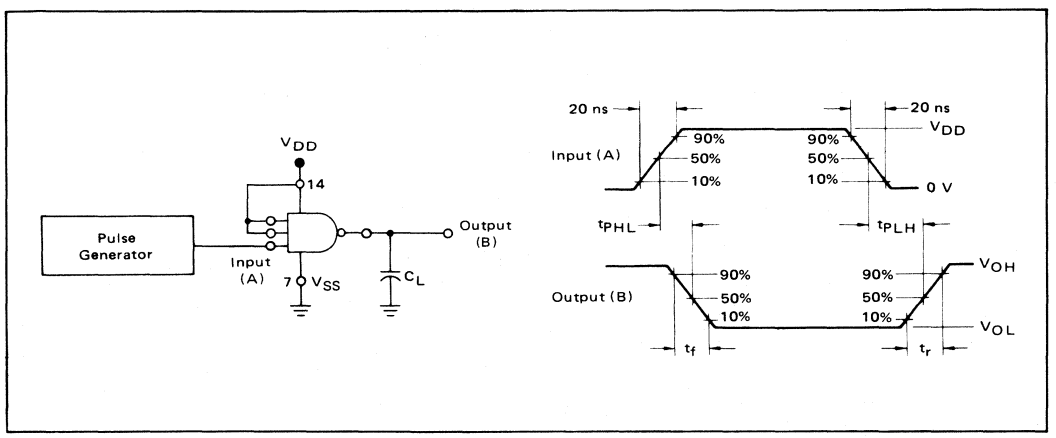


FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MC14024AL
MC14024CL
MC14024CP

SEVEN STAGE RIPPLE COUNTER

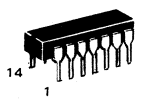
The MC14024 is a seven stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity (typically 45% of V_{DD}), however the Clock input has a typical noise immunity of 70% of V_{DD} with no maximum Clock input rise or fall time. The output of each counter stage is buffered.

- Quiescent Power Dissipation = 0.01 μW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- 8-MHz Operation @ V_{DD} = 10 Vdc typical
- Exceedingly Slow Input Transition Rates may be Applied to the Clock Input
- Pin-For-Pin Replacement for CD4024A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

SEVEN STAGE RIPPLE COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

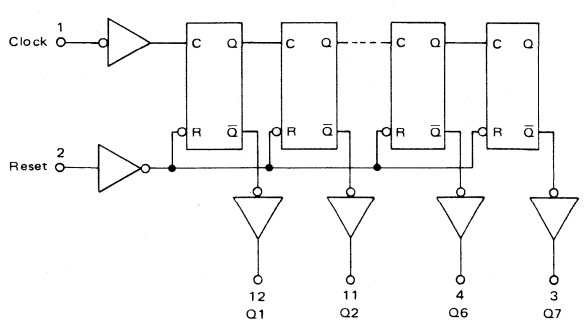
P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14024AL – MC14024CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14024AL – MC14024CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

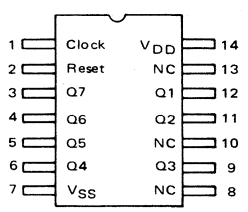
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

LOGIC DIAGRAM



Q3 = Pin 9
Q4 = Pin 6
Q5 = Pin 5

PIN ASSIGNMENT



V_{DD} = Pin 14
V_{SS} = Pin 7

NC = No Connection

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14024AL -55°C Min	MC14024AL -55°C Max	MC14024AL +25°C Min	MC14024AL +25°C Typ	MC14024AL +25°C Max	MC14024AL +125°C Min	MC14024AL +125°C Max	MC14024CL/CP -40°C Min	MC14024CL/CP -40°C Max	MC14024CL/CP +25°C Min	MC14024CL/CP +25°C Typ	MC14024CL/CP +25°C Max	MC14024CL/CP +85°C Min	MC14024CL/CP +85°C Max	Unit
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.20	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.50	–	0.40	0.80	–	0.28	–	0.23	–	0.20	0.80	–	0.60	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.10	–	0.90	1.20	–	0.65	–	0.60	–	0.50	1.20	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.80	–	–	–	–	–	–	7.80	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation** (C_L = 15 pF, f = 0 Hz)	3	P_D																μW
P_D = (0.645 mW/MHz) f + 0.0025 μW			5.0	–	0.25	–	0.0025	0.25	–	15	–	–	–	0.0025	2.5	–	75	
P_D = (2.5 mW/MHz) f + 0.01 μW			10	–	1.0	–	0.01	1.0	–	60	–	–	–	0.01	10	–	300	
P_D = (5.6 mW/MHz) f + 1.0 μW			15	–	–	–	1.0	–	–	–	–	–	–	1.0	–	–	–	
Output Rise and Fall Time** (C_L = 15 pF)	4	t_r, t_f																ns
t_r, t_f = (4.3 ns/pF) C_L + 35 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (0.47 ns/pF) C_L + 8.0 ns			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Turn-On, Turn-Off Delay** (C_L = 15 pF) (Clock to Q1)	4	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (2.7 ns/pF) C_L + 284.5 ns			5.0	–	–	–	325	400	–	–	–	–	–	325	500	–	–	
t_{PHL}, t_{PLH} = (1.6 ns/pF) C_L + 96 ns			10	–	–	–	120	150	–	–	–	–	–	120	180	–	–	
t_{PHL}, t_{PLH} = 1.2 ns/pF) C_L + 72 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Turn-On, Turn-Off Delay** (C_L = 15 pF) (Clock to Q7)	4	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = 2.7 ns/pF) C_L + 959.5 ns			5.0	–	–	–	1000	2000	–	–	–	–	–	1000	3000	–	–	
t_{PHL}, t_{PLH} = 1.6 ns/pF) C_L + 376 ns			10	–	–	–	400	545	–	–	–	–	–	400	750	–	–	
t_{PHL}, t_{PLH} = 1.2 ns/pF) C_L + 282 ns			15	–	–	–	300	–	–	–	–	–	–	300	–	–	–	
Reset Delay Time** (C_L = 15 pF) (Reset to Qn)	4	t_R																ns
t_{PHL}, t_{PLH} = (2.7 ns/pF) C_L + 459.5 ns			5.0	–	–	–	500	700	–	–	–	–	–	500	800	–	–	
t_{PHL}, t_{PLH} = (1.6 ns/pF) C_L + 226 ns			10	–	–	–	250	350	–	–	–	–	–	250	400	–	–	
t_{PHL}, t_{PLH} = (1.2 ns/pF) C_L + 162 ns			15	–	–	–	180	–	–	–	–	–	–	180	–	–	–	
Minimum Clock Pulse Width NCP = PCP = PW_C	4	PW_C																ns
			5.0	–	–	–	200	330	–	–	–	–	–	200	500	–	–	
			10	–	–	–	60	125	–	–	–	–	–	60	165	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Minimum Reset Pulse Width	4	PW_R																ns
			5.0	–	–	–	375	500	–	–	–	–	–	375	600	–	–	
			10	–	–	–	200	300	–	–	–	–	–	200	350	–	–	
			15	–	–	–	150	–	–	–	–	–	–	150	–	–	–	
Reset Removal Time	4	t_{rem}																ns
			5.0	–	–	–	250	375	–	–	–	–	–	250	625	–	–	
			10	–	–	–	75	110	–	–	–	–	–	75	190	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Maximum Clock Input Rise and Fall Times		t_r, t_f																μs
			5.0	No Maximum Limit							–	–	–	∞	100	–	–	
			10								–	–	–	∞	100	–	–	
			15								–	–	–	∞	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

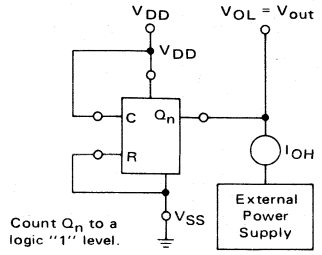


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

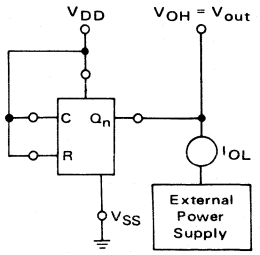
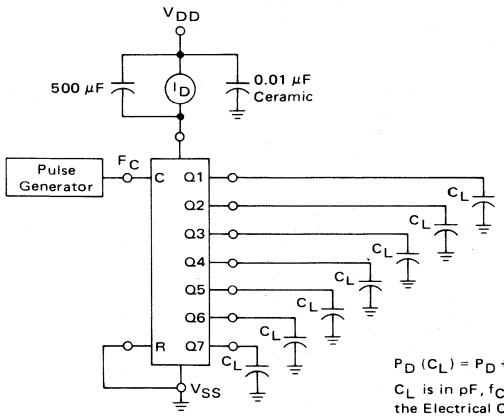


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT



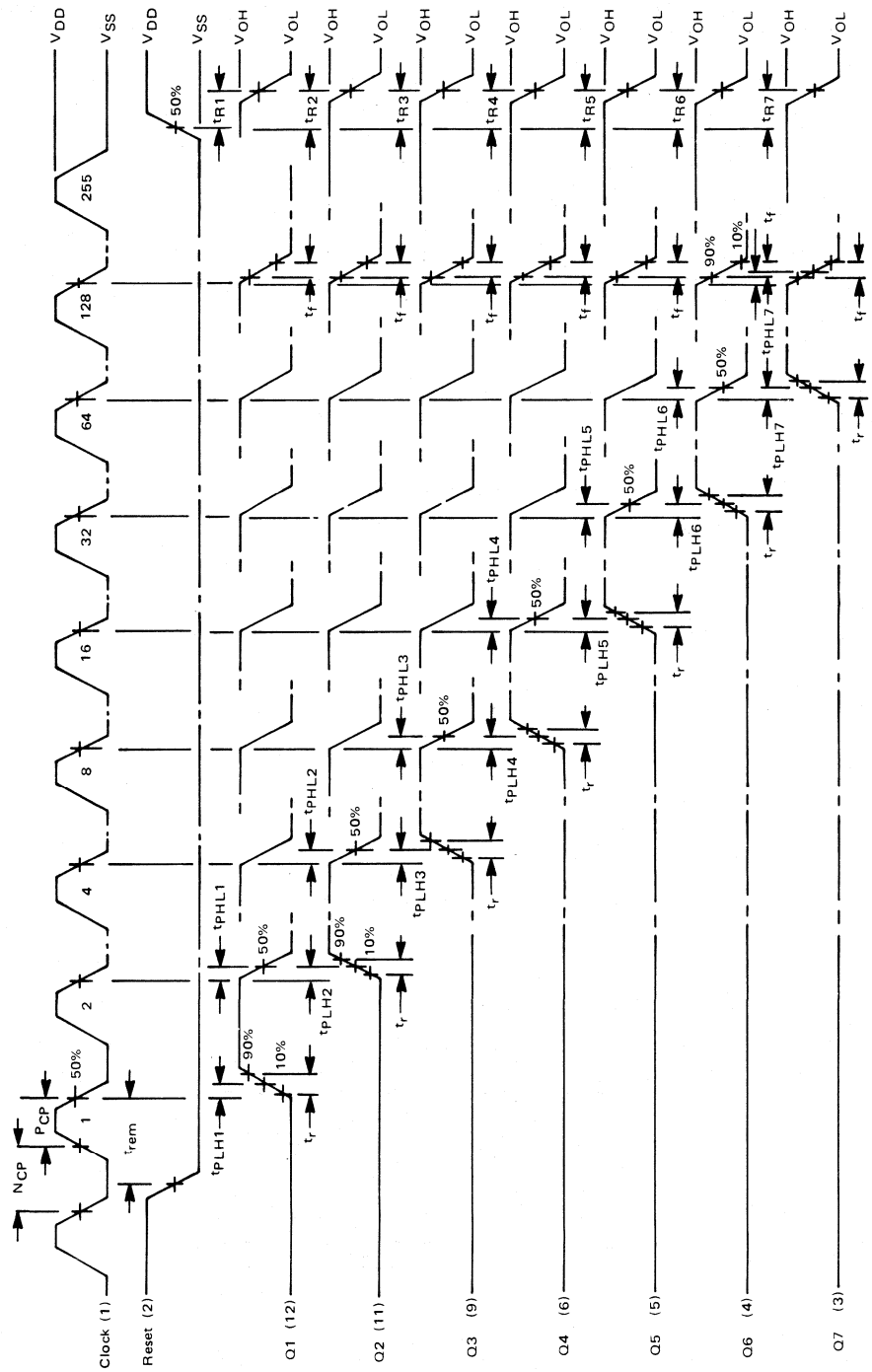
$P_D (C_L) = P_D + (C_L - 15) f_C V_{DD}^2 \times 10^{-3}$ mW

C_L is in pF, f_C is in MHz, V_{DD} is in Vdc, and P_D is obtained from the Electrical Characteristics table.

TRUTH TABLE

CLOCK	RESET	STATE
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
¬	0	Advance One Count
¬	1	All Outputs Low

FIGURE 4 – FUNCTIONAL WAVEFORMS



Input t_r and t_f = 20 ns

MC14025AL
MC14025CL
MC14025CP

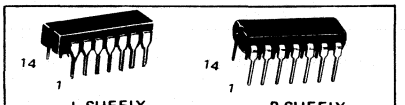
TRIPLE 3-INPUT "NOR" GATE

The MC14025 triple 3-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14025AL)
  = 3.0 Vdc to 16 Vdc (MC14025CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 750 ohms typical
- Pin-for-Pin Replacement for CD4025A

MCMOS
(LOW-POWER COMPLEMENTARY MOS)

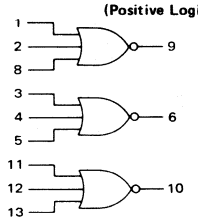
TRIPLE 3-INPUT "NOR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

LOGIC DIAGRAM
(Positive Logic)



V_{DD} = Pin 14
V_{SS} = Pin 7

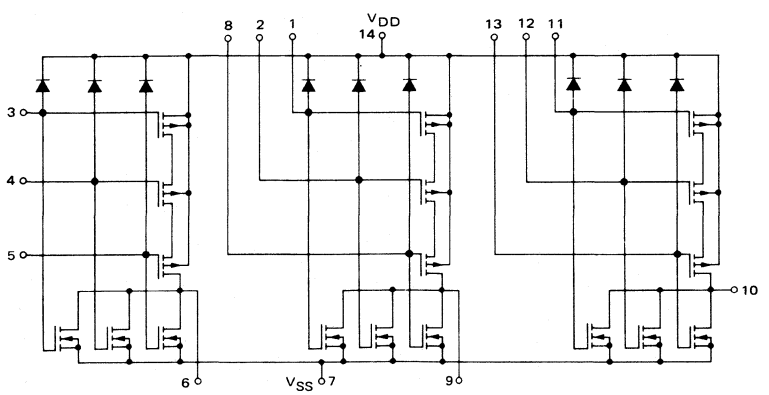
$9 = \overline{1 + 2 + 8}$

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14025AL —MC14025CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14025AL —MC14025CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC



See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14025AL -55°C Min	MC14025AL -55°C Max	MC14025AL +25°C Min	MC14025AL +25°C Typ	MC14025AL +25°C Max	MC14025AL +125°C Min	MC14025AL +125°C Max	MC14025CL/CP -40°C Min	MC14025CL/CP -40°C Max	MC14025CL/CP +25°C Min	MC14025CL/CP +25°C Typ	MC14025CL/CP +25°C Max	MC14025CL/CP +85°C Min	MC14025CL/CP +85°C Max	Unit
Output Voltage	"0" Level	1,2,3	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*		–																	Vdc
($V_{out} \geq 3.5$ Vdc)			V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \leq 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current			I_{OH}																mAdc
(V_{out} = 2.5 Vdc)	Source	4		5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	
(V_{out} = 9.5 Vdc)				10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{out} = 13.5 Vdc)				15	–	–	–	-3.6	–	–	–	–	–	–	3.6	–	–	–	
(V_{out} = 0.4 Vdc)	Sink	5	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{out} = 0.5 Vdc)				10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{out} = 1.5 Vdc)				15	–	–	–	7.8	–	–	–	–	–	–	7.8	–		–	
Input Current		–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation			P_D	5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	μW
				10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
Output Rise Time		9	t_r	5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	ns
(C_L = 15 pF)				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Output Fall Time		9	t_f	5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	ns
(C_L = 15 pF)				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Turn-On Delay Time		9	t_{PHL}	5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	ns
(C_L = 15 pF)				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
				15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Turn-Off Delay Time		9	t_{PLH}	5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	ns
(C_L = 15 pF)				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

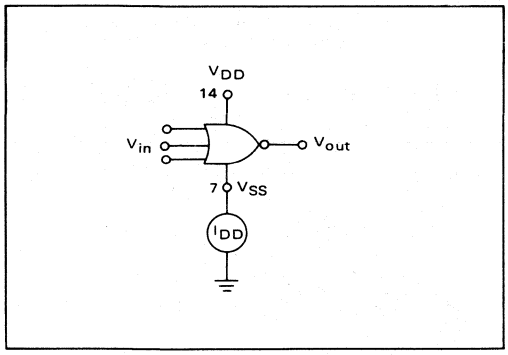


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

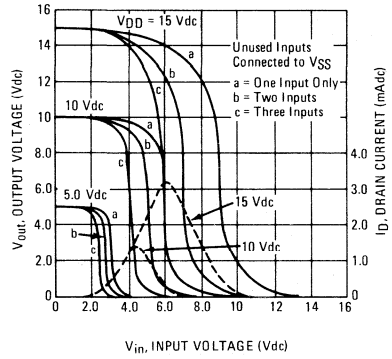


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

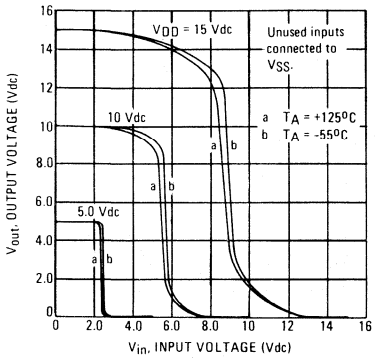
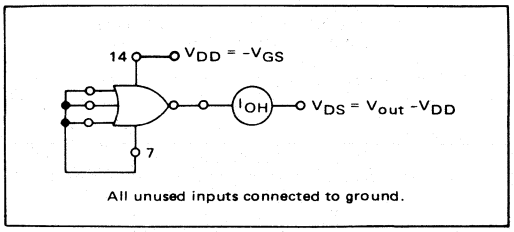


FIGURE 4 – TYPICAL SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



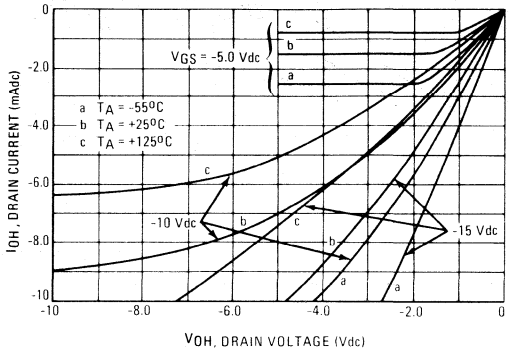
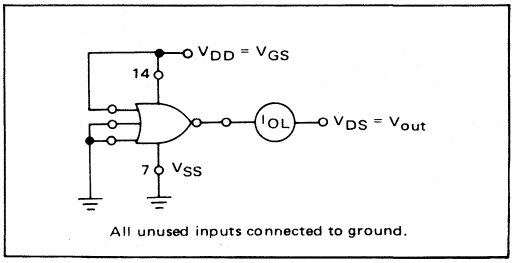
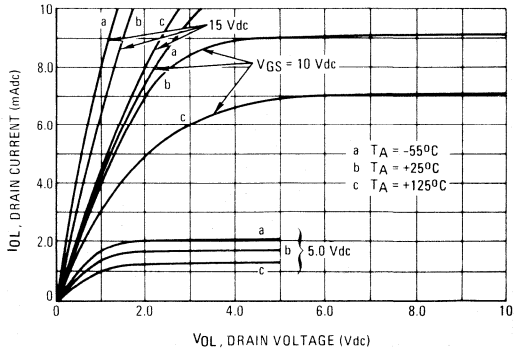


FIGURE 5 – TYPICAL SINK CURRENT CHARACTERISTICS TEST CIRCUIT





7

FIGURE 6 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

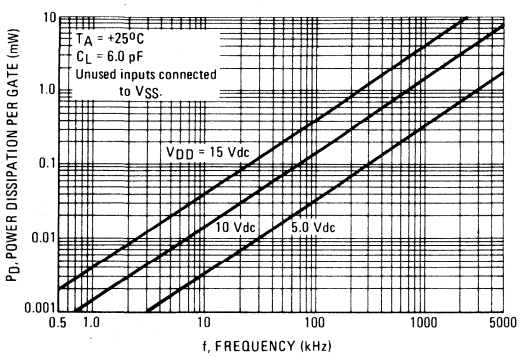


FIGURE 7 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

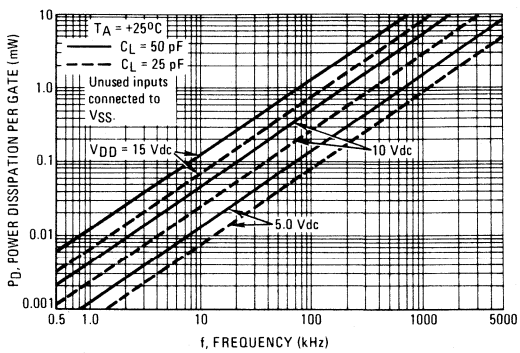


FIGURE 8 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

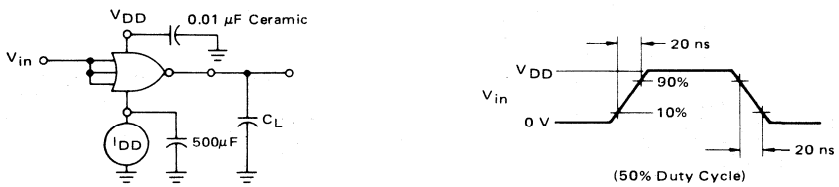
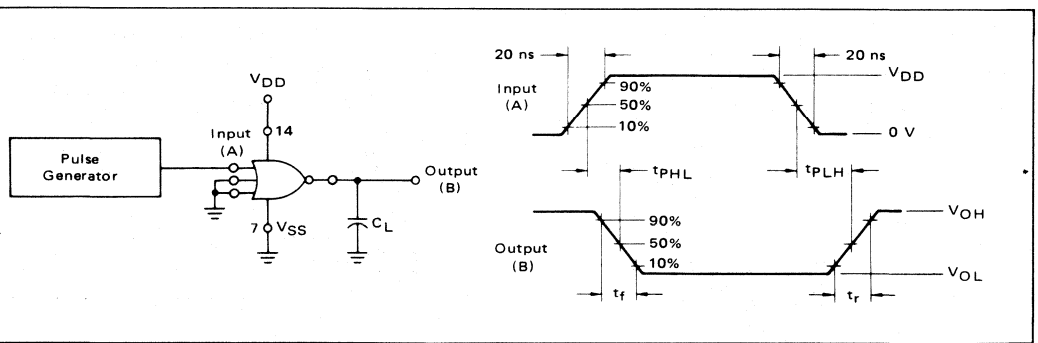


FIGURE 9 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14027AL
MC14027CL
MC14027CP

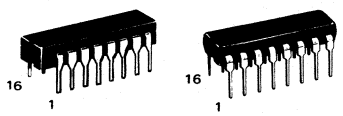
DUAL J-K FLIP-FLOP

The MC14027 dual J-K flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent J, K, Clock, Set and Reset inputs. These devices may be used in control, register, or toggle functions. They find primary use where very low power dissipation and/or high noise immunity inherent in CMOS offers a system advantage.

- Quiescent Power Dissipation = 50 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14027AL)
  = 3.0 Vdc to 16 Vdc (MC14027CL/CP)
- Single Supply Operation – Positive or Negative
- Toggle Rate = 8.0 MHz typical
- Logic Swing Independent of Fanout
- Logic Edge-Clocked Flip-Flop Design –
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4027

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL J-K FLIP-FLOP



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14027AL MC14027CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14027AL MC14027CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

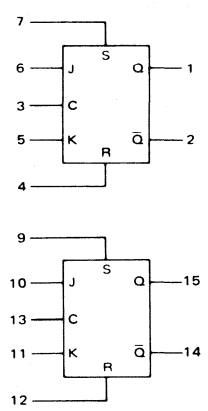
Synchronous

J	K	Q_n	Q_{n+1}
0	0	Q_n	Q_n
1	0	0	1
1	0	1	1
0	1	0	0
0	1	1	0
1	1	0	1
1	1	1	0

Asynchronous

R	S	Q	$\bar{Q}$
1	0	0	1
0	1	1	0
1	1	1	1

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

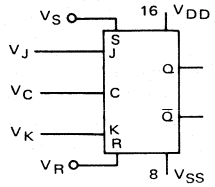
See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	MC14027AL							MC14027CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage		–																Vdc
(V_{DD} = 5.0 Vdc)	"0" Level		V_{OL}	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{DD} = 10 Vdc)				–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{DD} = 5.0 Vdc)	"1" Level		V_{OH}	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
(V_{DD} = 10 Vdc)				9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity		–																Vdc
(V_{DD} = 5.0 Vdc)			V_{NL}	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{DD} = 10 Vdc)				3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{DD} = 5.0 Vdc)			V_{NH}	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{DD} = 10 Vdc)				2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc, V_{DS} = 5.0 Vdc)	Source	4	I_{OH}	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	
(V_{OH} = 9.5 Vdc, V_{DS} = 10 Vdc)				-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OL} = 0.4 Vdc, V_{DS} = 5.0 Vdc)	Sink	5	I_{OL}	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc, V_{DS} = 10 Vdc)				1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
Input Current		–	I_{in}	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance		–	C_{in}															pF
(V_{in} = 0)				–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation		2,3	P_D															µW
(V_{DD} = 5.0 Vdc)				–	5.0	–	0.025	5.0	–	300	–	50	–	0.05	50	–	700	
(V_{DD} = 10 Vdc)				–	20	–	0.05	20	–	1200	–	200	–	0.2	200	–	2800	
Output Rise Time		6,7	t_r															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	100	175	–	–	–	–	–	100	200	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Output Fall Time		6,7	t_f															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	100	175	–	–	–	–	–	100	200	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Turn-On Delay Time		6,8	t_{PHL}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	150	300	–	–	–	–	–	150	400	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	75	110	–	–	–	–	–	75	150	–	–	
Turn-Off Delay Time		6,8	t_{PLH}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	150	300	–	–	–	–	–	150	400	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	75	110	–	–	–	–	–	75	150	–	–	
Min Clock Pulse Width		6	PW															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	125	300	–	–	–	–	–	125	400	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	50	100	–	–	–	–	–	50	150	–	–	
Max Clock Pulse Frequency		6	PRF															MHz
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	1.5	3.0	–	–	–	–	–	1.0	3.0	–	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	4.5	8.0	–	–	–	–	–	3.0	8.0	–	–	–	
Clock Pulse Rise and Fall Times		6	t_r, t_f															µs
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	15	–	–	–	–	–	–	15	–	–	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	–	
Set and Reset Propagation Delay Times		–	t_{PHL}, t_{PLH}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	175	225	–	–	–	–	–	175	350	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	75	110	–	–	–	–	–	75	150	–	–	
Set and Reset Pulse Width		–	PW_H															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	125	200	–	–	–	–	–	125	300	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	50	80	–	–	–	–	–	50	120	–	–	
Setup Time		–	t_{setup}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	70	150	–	–	–	–	–	70	200	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	25	50	–	–	–	–	–	25	75	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level, that the circuit will withstand before producing an output state change.

FIGURE 1 – INPUT THRESHOLD VOLTAGE TEST CIRCUIT AND PROCEDURES

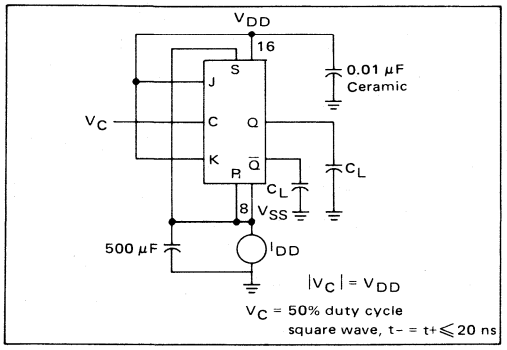


V_C = 500 kHz, 50% duty cycle
square wave, $t_- = t_+ \leqslant 20$ ns

Note: Unused inputs connected to V_{SS}.

1. Clock Input: $V_R = V_S = V_{NL}$ min (worst "0").
   $V_J = V = V_{DD} - V_{NH}$ min (worst "1").
   a. V_{th} L: Increase V_C "0" state level until toggling action stops.
   b. V_{th} H: Decrease V_C "1" state level until toggling action stops.
2. J, K Inputs: $V_R = V_S = V_{NL}$ min
   a. V_{th} L: (J) V_K = "1" Increase V_J "0" state level until toggling action begins.
   (K) V_J = "1" Increase V_K "0" state level until toggling action begins.
   b. V_{th} H: (J) V_K = "1" Decrease V_J "1" state level until toggling action stops.
   (K) V_J = "1" Decrease V_K "1" state level until toggling action stops.
3. Set, Reset Inputs: $V_J = V_K = V_{DD} - V_{NH}$ min
   a. V_{th} L: Increase V_R or V_S "0" state level until toggling action stops.
   b. V_{th} H: Decrease V_R or V_S "1" state level until toggling action begins.

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT



V_C = 50% duty cycle
square wave, $t_- = t_+ \leqslant 20$ ns

FIGURE 3 – TYPICAL POWER DISSIPATION CHARACTERISTICS

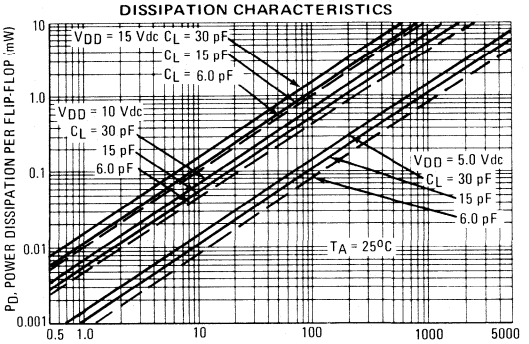
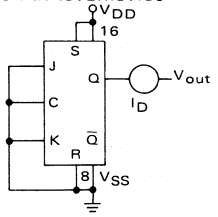


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS



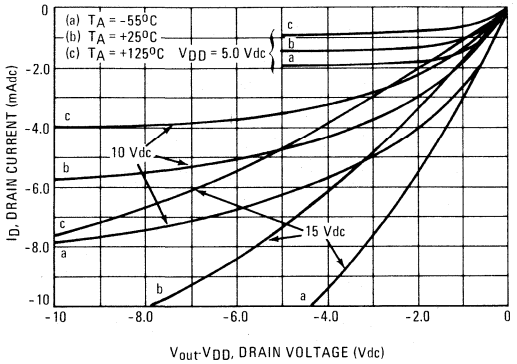
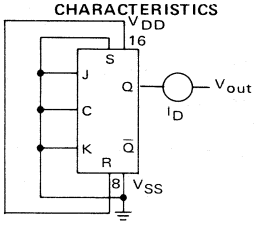


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS



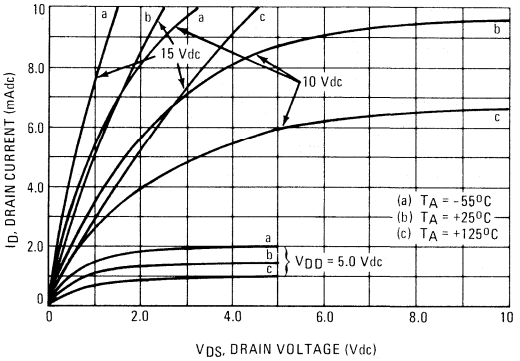


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FIGURE 6 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

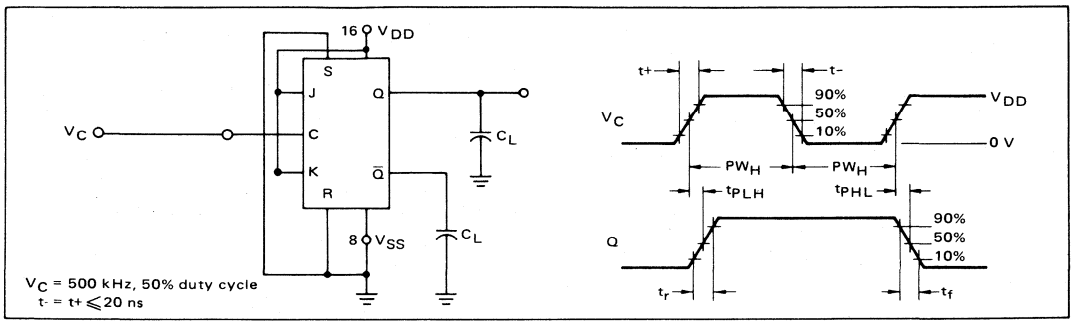


FIGURE 7 – TYPICAL RISE AND FALL TIMES versus LOAD CAPACITANCE

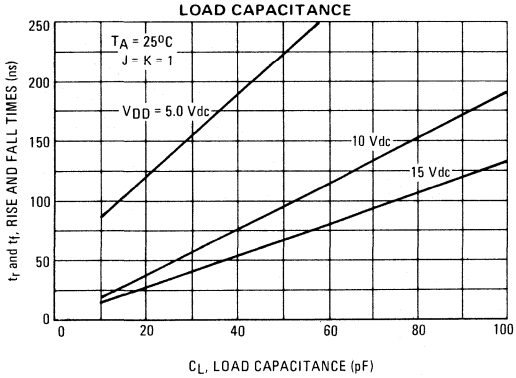


FIGURE 8 – TYPICAL TURN-ON AND TURN-OFF DELAY CHARACTERISTICS

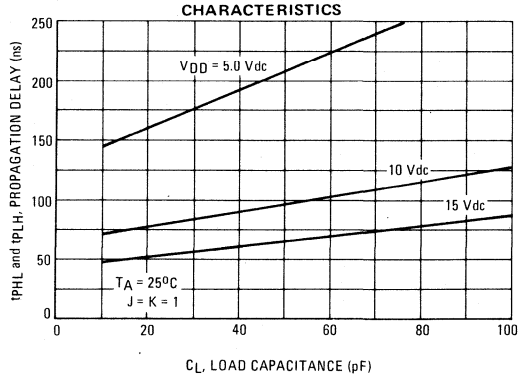
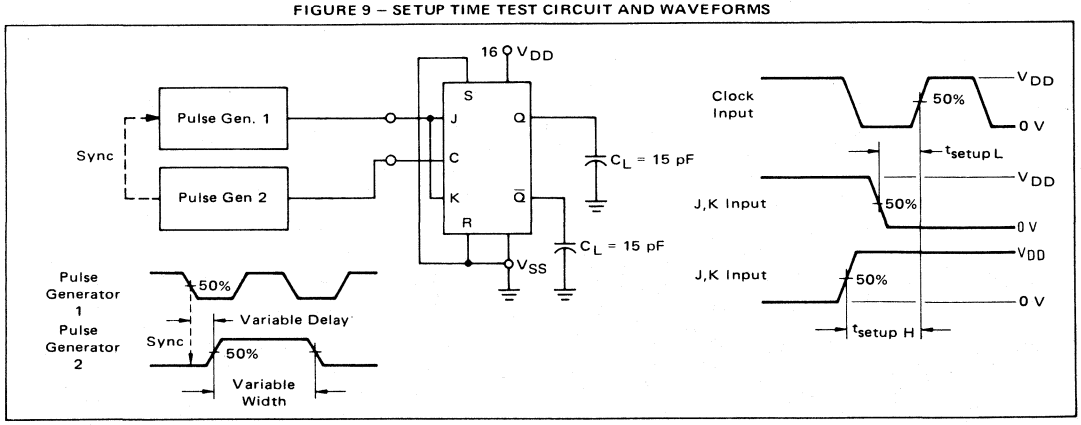
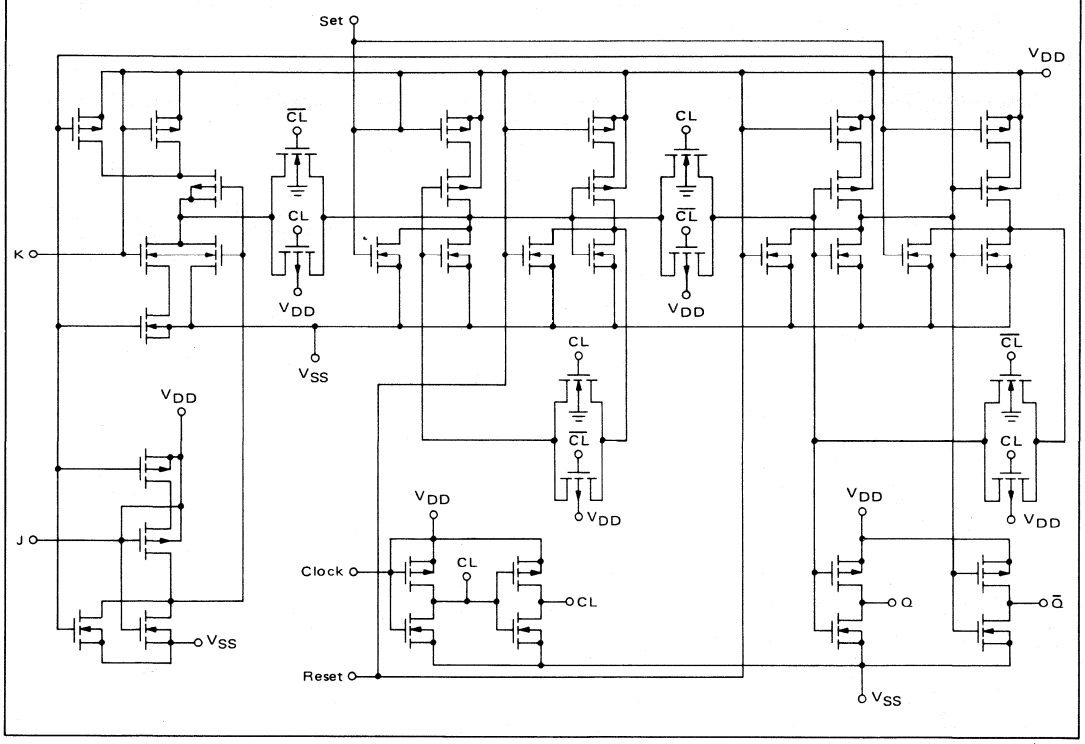


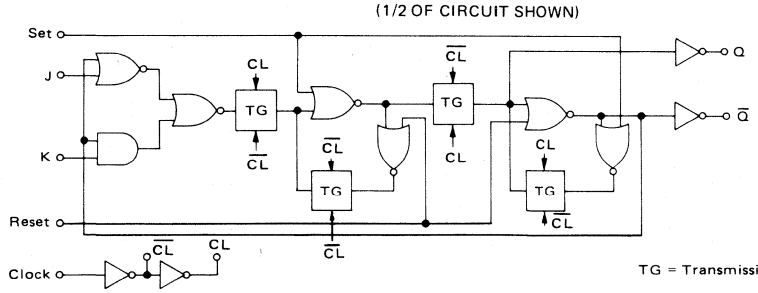
FIGURE 9 – SETUP TIME TEST CIRCUIT AND WAVEFORMS



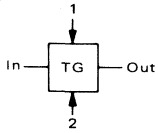
CIRCUIT SCHEMATIC
(1/2 OF DEVICE SHOWN)



LOGIC DIAGRAM
(1/2 OF CIRCUIT SHOWN)



TG = Transmission Gate



Input to Output is:

(a) A bidirectional short circuit when control input 1 is "Low" and control input 2 is "High".

(b) An open circuit when control input 1 is "High" and control input 2 is "Low".

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MC14028AL
MC14028CL
MC14028CP

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER

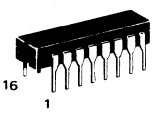
The MC14028 decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one-of-ten) decoded output, while a 3-bit binary input provides a decoded octal (one-of-eight) code output with D forced to a logic "0". Expanded decoding such as binary-to-hexadecimal (one-of-16), etc., can be achieved by using other MC14028 devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout — > 50
- Buffered Outputs Compatible with HTL and Low-Power TTL
- Positive Logic Design
- Low Power Dissipation of 25 nW/package typical
- Low Outputs on All Illegal Input Combinations
- Pin-for-Pin Replacement for CD4028A

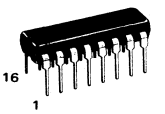
McMOS

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-DECIMAL DECODER
BINARY-TO-OCTAL DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



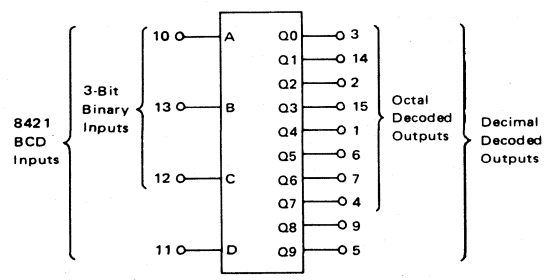
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14028AL — MC14028CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14028AL — MC14028CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLE

INPUT				OUTPUT									
D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14028AL -55°C Min	MC14028AL -55°C Max	MC14028AL +25°C Min	MC14028AL +25°C Typ	MC14028AL +25°C Max	MC14028AL +125°C Min	MC14028AL +125°C Max	MC14028CL/CP -40°C Min	MC14028CL/CP -40°C Max	MC14028CL/CP +25°C Min	MC14028CL/CP +25°C Typ	MC14028CL/CP +25°C Max	MC14028CL/CP +85°C Min	MC14028CL/CP +85°C Max	Unit
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*		V_{NL}																Vdc
(V_{out} ≥ 3.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≥ 7.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≥ 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
(V_{out} ≤ 1.5 Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
(V_{out} ≤ 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≤ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	-1.8	–	-0.35	–	-0.23	–	-0.20	-1.8	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.0	–	-0.35	–	-0.23	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.9	–	–	–	–	–	–	-3.9	–	–	–	
		I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation** †	1a	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (1.3 mW/MHz) f + 0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (5.0 mW/MHz) f + 0.000010 mW			10	–	0.10	–	0.000010	0.10	–	6.0	–	1.0	–	0.000010	1.0	–	14	
P_D = (11.5 mW/MHz) f + 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	1b	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	1b	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.77 ns/pF) C_L + 23 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.59 ns/pF) C_L + 16 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time**	1b	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (1.7 ns/pF) C_L + 120 ns			5.0	–	–	–	145	480	–	–	–	–	–	145	700	–	–	
t_{PLH} = (0.8 ns/pF) C_L + 45 ns			10	–	–	–	57	180	–	–	–	–	–	57	290	–	–	
t_{PLH} = (0.47 ns/pF) C_L + 40 ns			15	–	–	–	47	–	–	–	–	–	–	47	–	–	–	
Turn-On Delay Time**	1b	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (1.0 ns/pF) C_L + 225 ns			5.0	–	–	–	240	480	–	–	–	–	–	240	700	–	–	
t_{PHL} = (0.67 ns/pF) C_L + 90 ns			10	–	–	–	100	180	–	–	–	–	–	100	290	–	–	
t_{PHL} = (0.33 ns/pF) C_L + 60 ns			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

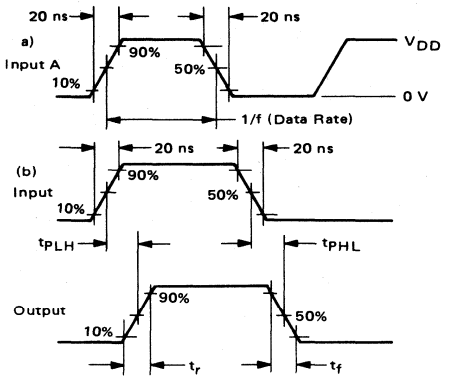
**The formula given is for the typical characteristics only.

†For dissipation at different external Load Capacitance (C_L) refer to corresponding formula:

$P_D(C_L) = P_D + 10^{-3}(C_L - 15\text{ pF})\ V_{DD}{}^2 f$

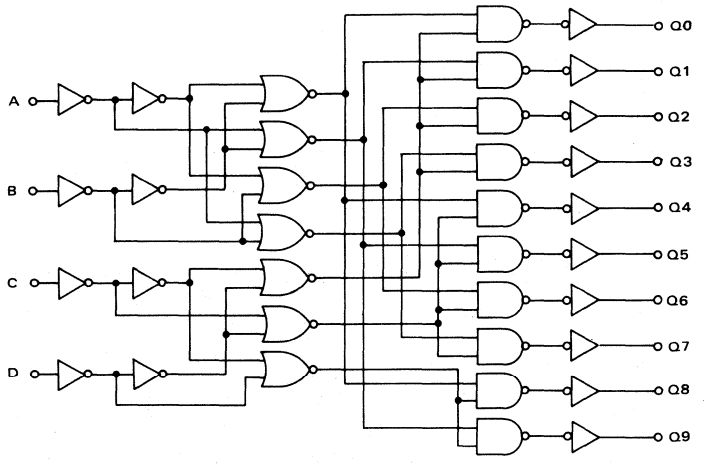
where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – DYNAMIC SIGNAL WAVEFORMS



All outputs connected to respective C_L loads.

LOGIC DIAGRAM



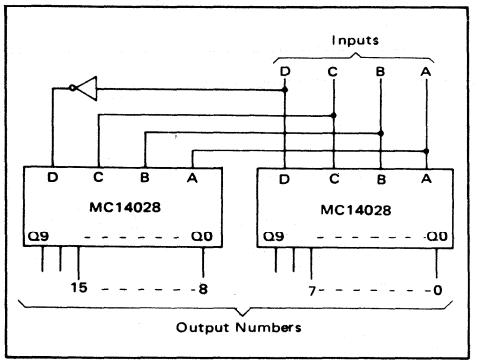
7

APPLICATION INFORMATION

Expanded decoding can be performed by using the MC14028 and other McMOS Integrated Circuits. The circuits in Figure 2 converts any 4-bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4-bit binary, 4-bit gray, excess-3, or excess-3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6-bit binary 1-of-64 decoder using nine MC14028 circuits and two MC14009 inverting hex buffers.

The MC14028 can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

FIGURE 2 – CODE CONVERSION CIRCUIT AND TRUTH TABLE



INPUTS				OUTPUT NUMBERS																CODE AND REDEFINED OUTPUT NUMBERS					
																				Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4-Bit Binary	4-Bit Gray	Excess-3	Excess-3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

FIGURE 3 – SIX-BIT BINARY 1-OF-64 DECODER

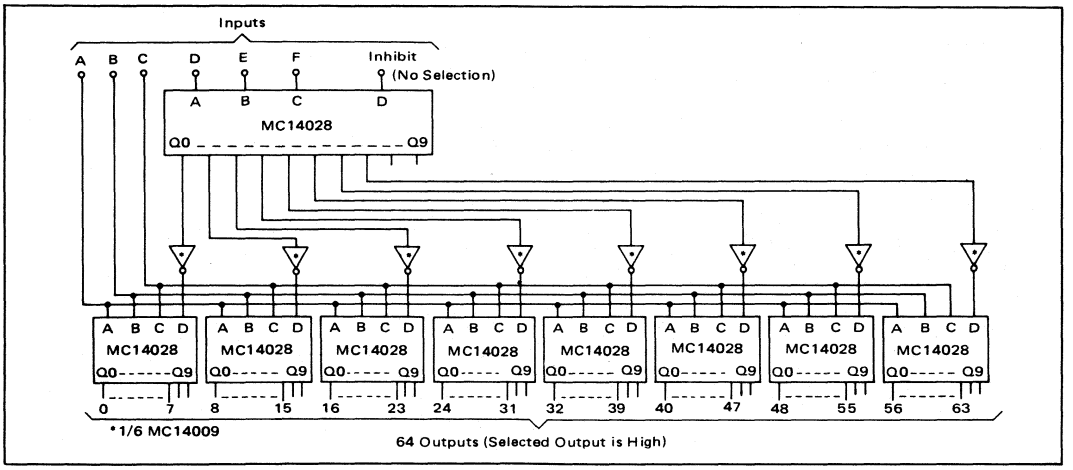
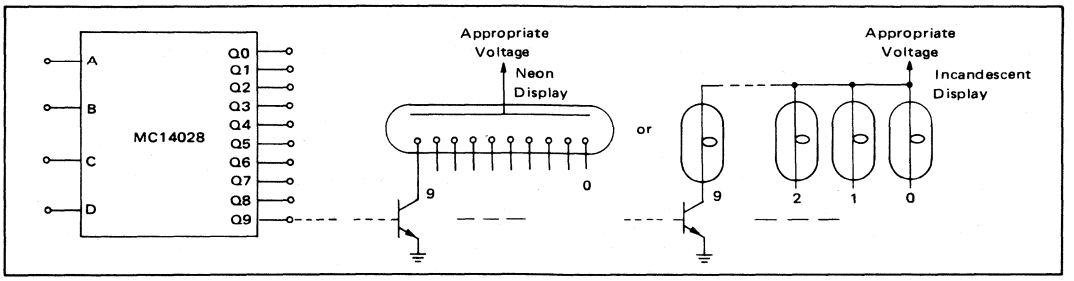


FIGURE 4 – DECIMAL DIGIT DISPLAY APPLICATION



MC14032AL
MC14032CL
MC14032CP
MC14038AL
MC14038CL
MC14038CP

Advance Information

TRIPLE SERIAL ADDERS

The MC14032 and MC14038 triple serial adders have the clock and carry reset inputs common to all three adders. The carry is added on the positive-going clock transition for the MC14032, and on the negative-going clock transition for the MC14038. Typical applications include serial arithmetic units, digital correlators, digital servo control systems, datalink computers, and flight control computers.

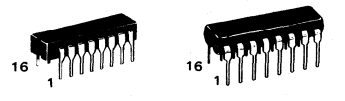
- Static Operation from dc to 5.0 MHz
- Buffered Outputs
- Single-Phase Clocking
- Quiescent Power Dissipation = 0.25 μW/package typical @ V_{DD} = 5.0 Vdc
- Pin-for-Pin Replacement for CD4032A and CD4038A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

TRIPLE SERIAL ADDERS

Positive Logic — MC14032
Negative Logic — MC14038



L SUFFIX
CERAMIC PACKAGE
CASE 620

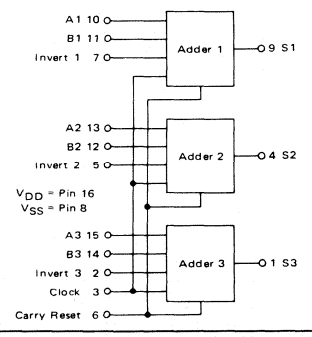
P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14032AL/038AL —MC14032CL,CP/038CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range— MC14032AL/038AL MC14032CL,CP/038CL,CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

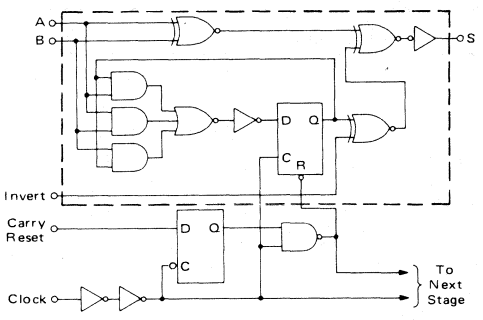
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

BLOCK DIAGRAM

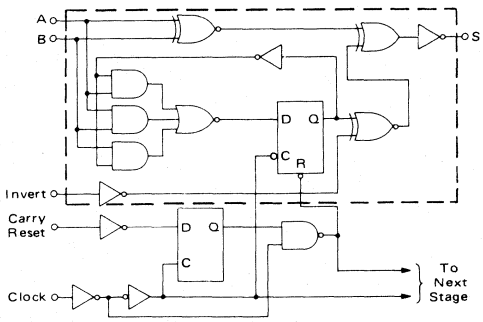


LOGIC DIAGRAMS
(ONE SECTION AND COMMON INPUTS SHOWN)

MC14032



MC14038



This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14032AL/MC14038AL -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC14032CL,CP/MC14038CL,CP -40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Level "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	Vdc
"1" Level			5.0	4.99	–	4.99	5.0	–	–	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	4.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	9.95	–	–	–	–	15	–	–	–	
Noise Immunity*		V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	1	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.5	-1.3	–	-0.35	–	-0.23	–	-0.2	-1.3	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.6	–	0.28	–	0.23	–	0.2	0.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.6	–	0.65	–	0.6	–	0.5	1.6	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF)	3	P_D																μW
P_D = (3.5 mW/MHz) C_L + 0.00025 mW			5.0	–	25	–	0.25	25	–	–	–	250	–	0.25	250	–	3500	
P_D = (14 mW/MHz) C_L + 0.001 mW)			10	–	100	–	1.0	100	–	–	–	1000	–	1.0	1000	–	14000	
P_D = (30 mW/MHz) C_L + 0.002 mW)			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Output Rise and Fall Time**		t_r, t_f																ns
(C_L = 15 pF)																		
t_r, t_f = (3.0 ns/pF) C_L + 30 ns			5.0	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
t_r, t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (1.0 ns/pF) C_L + 10 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On and Turn-Off Delay Time**	4	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF)																		
A,B or Invert to Sum																		
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 198 ns			5.0	–	–	–	225	1100	–	–	–	–	–	225	1400	–	–	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 78 ns			10	–	–	–	90	250	–	–	–	–	–	90	300	–	–	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 61 ns			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	
Clock to Sum																		
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 423 ns			5.0	–	–	–	450	2200	–	–	–	–	–	450	2400	–	–	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 138 ns			10	–	–	–	150	500	–	–	–	–	–	150	600	–	–	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 106 ns			15	–	–	–	115	–	–	–	–	–	–	115	–	–	–	
Input Setup Time #	4	t_{setup}	5.0	–	–	–	-10	10	–	–	–	–	–	-10	10	–	–	ns
			10	–	–	–	0	10	–	–	–	–	–	0	10	–	–	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
Maximum Clock Pulse Frequency		PRF	5.0	–	–	1.5	4.0	–	–	–	–	–	1.0	4.0	–	–	–	MHZ
(C_L = 15 pF)			10	–	–	3.0	10	–	–	–	–	–	2.5	10	–	–	–	
			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Maximum Clock Rise and Fall Times		t_r, t_f	5.0	–	–	15	–	–	–	–	–	–	15	–	–	–	–	μs
			10	–	–	15	–	–	–	–	–	–	15	–	–	–	–	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	

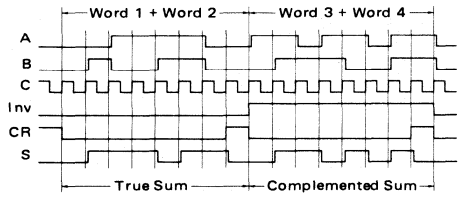
*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

#Input Setup Time is defined as the minimum time required between the positive transition of the clock (MC14032) and a change of state of A, B, or Reset. (Negative transition for MC14038).

TIMING DIAGRAMS

MC14032

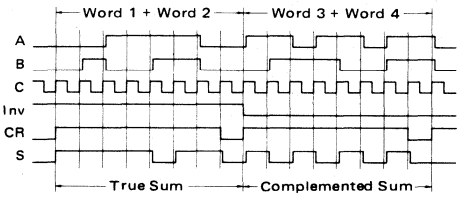


Word 1: 0.0111100 = +60 Word 3: 1.1011011 = -37

Word 2: 0.0110010 = +50 Word 4: 1.1001110 = -50

0.1101110 = +110 1.0101001 = -87

MC14038



Word 1: 1.1000011 = -61 Word 3: 0.0100100 = +36

Word 2: 1.1001101 = -51 Word 4: 0.0110001 = +49

1.0010000 = -112 0.1010101 = +85

Note: Unused input pins must be connected to either V_{DD} or V_{SS}.

FIGURE 1 – TYPICAL OUTPUT SOURCE TEST CIRCUIT

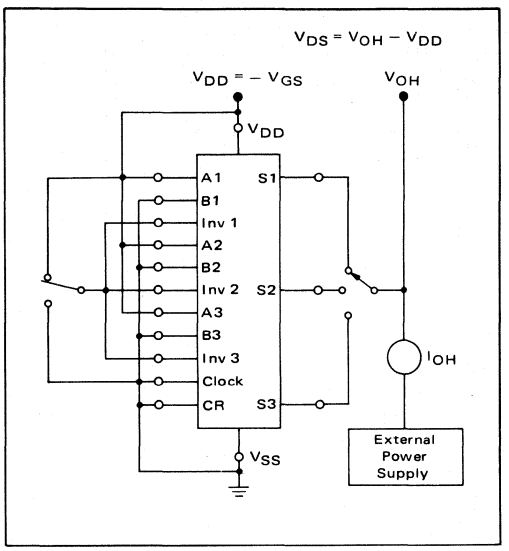


FIGURE 2 – TYPICAL OUTPUT SINK TEST CIRCUIT

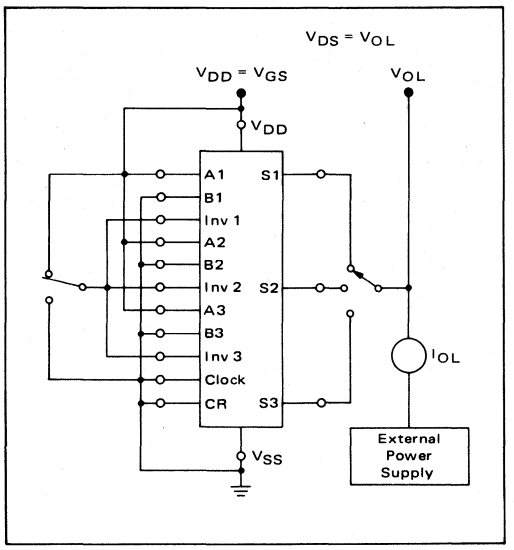


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

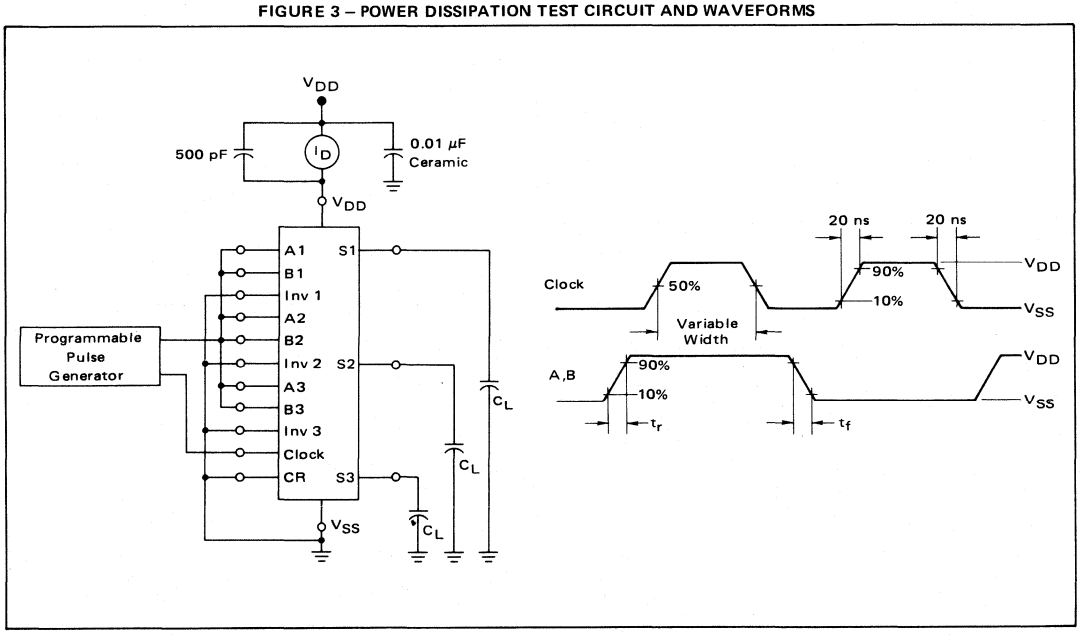


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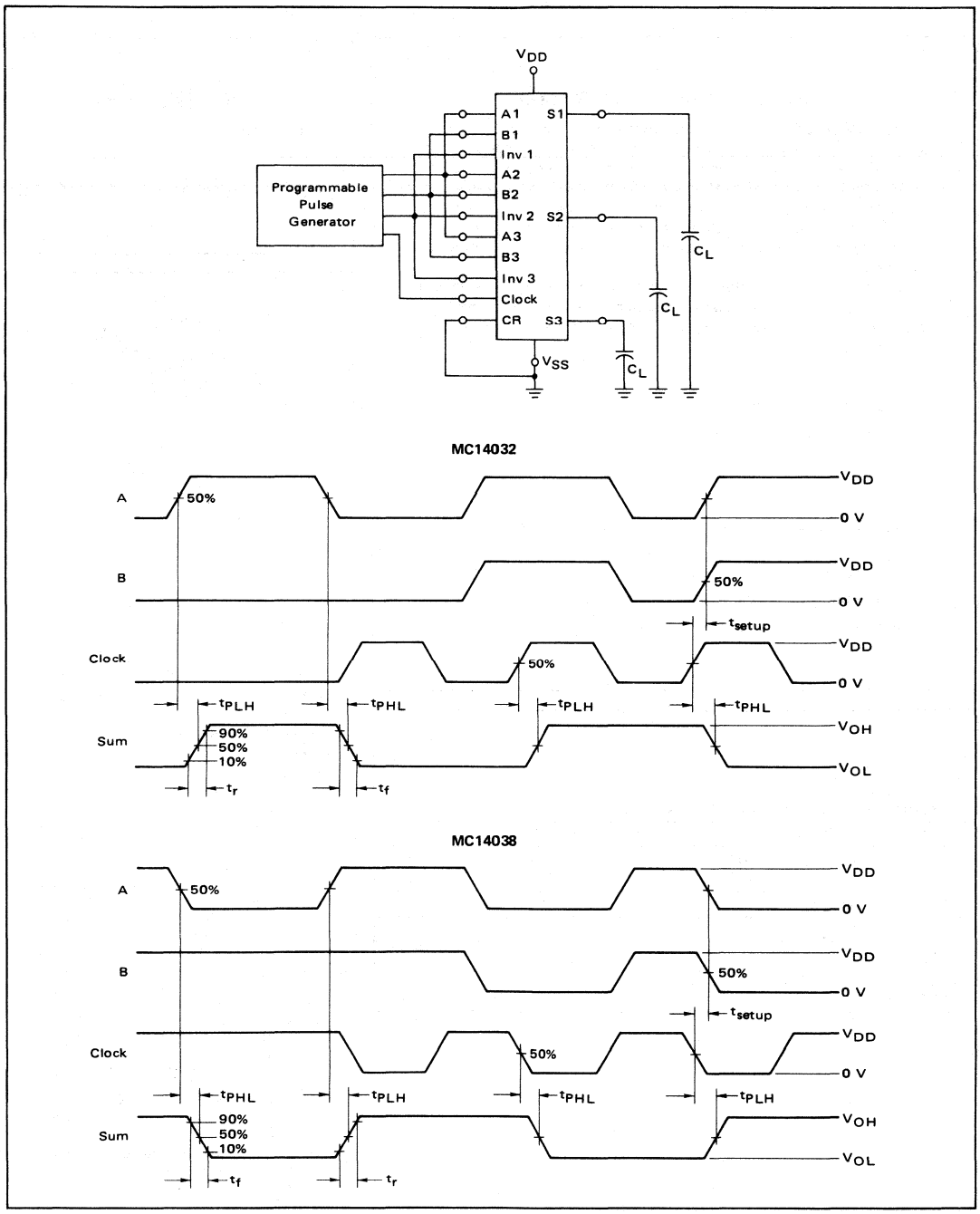
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14034AL
MC14034CL

8-BIT UNIVERSAL BUS REGISTER

The MC14034AL/CL is a bidirectional 8-bit static parallel/serial, input/output bus register. The device contains two sets of input/output lines which allows the bidirectional transfer of data between two buses; the conversion of serial data to parallel form, or the conversion of parallel data to serial form. Additionally the serial data input allows data to be entered shift/right, while shift/left can be accomplished by hard-wiring each parallel output to the previous parallel bit input.

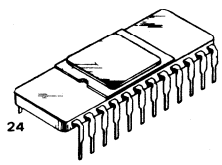
Other useful applications for this device include pseudo-random code generation, sample and hold register, frequency and phase-comparator, address or buffer register, and serial/parallel input/output conversions.

- Bidirectional Parallel Data Input
- Quiescent Power Dissipation = 5.0 μW/package typical @ V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14034AL)
  = 3.0 Vdc to 16 Vdc (MC14034CL)
- Static Operation 0 to 5.0 MHz @ V_{DD} = 10 Vdc
- Single Supply Operation = Positive or Negative
- Pin-for-Pin Replacement for CD4034A

McMOS

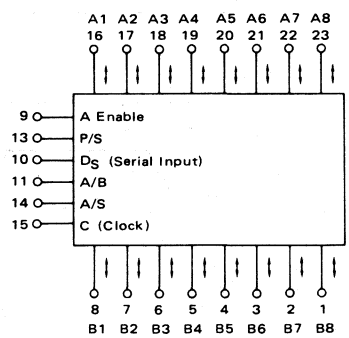
(LOW-POWER COMPLEMENTARY MOS)

8-BIT UNIVERSAL BUS REGISTER



CERAMIC PACKAGE
CASE 684

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14034AL MC14034CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14034AL —MC14034CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

MC14034 (continued)

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14034AL -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC14034CL -40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
	–	I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	0.5	–	0.4	0.9	–	0.28	–	0.23	–	0.2	0.9	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.3	–	0.65	–	0.6	–	0.5	2.3	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	1,2	P_D	5.0	–	0.025	–	0.0015	0.025	–	–	–	–	–	0.0015	0.25	–	3.5	mW
			10	–	0.1	–	0.005	0.1	–	–	–	–	–	0.005	1.0	–	14	
			15	–	–	–	0.015	–	–	–	–	–	–	0.015	–	–	–	
Output Transition Times* (C_L = 15 pF) A Data Output, B Data Output	3,4,5	t_r, t_f																ns
t_r, t_f = (1.9 ns/pF) C_L + 47 ns			5.0	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
t_r, t_f = (1.0 ns/pF) C_L + 20 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (0.7 ns/pF) C_L + 15 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On Turn-Off Delay Time** (C_L = 15 pF) A (B) Synchronous Parallel Data Input, B (A) Parallel Data Output	3,4,5	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (0.9 ns/pF) C_L + 459 ns			5.0	–	–	–	470	940	–	–	–	–	–	470	1200	–	–	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 169 ns			10	–	–	–	175	350	–	–	–	–	–	175	480	–	–	
t_{PLH}, t_{PHL} = (0.3 ns/pF) C_L + 121			15	–	–	–	125	–	–	–	–	–	–	125	–	–	–	
Turn-On, Turn-Off Delay Time** (C_L = 15 pF) A (B) Asynchronous Parallel Data Input, B (A) Parallel Data Output		t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.2 ns/pF) C_L + 432 ns			5.0	–	–	–	450	900	–	–	–	–	–	450	1350	–	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 143 ns			10	–	–	–	150	300	–	–	–	–	–	150	450	–	–	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 104 ns			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)		PW_C	5.0	–	–	–	170	340	–	–	–	–	–	170	500	–	–	ns
			10	–	–	–	70	70	–	–	–	–	–	70	200	–	–	
			15	–	–	–	55	–	–	–	–	–	–	55	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)		PRF	5.0	–	–	1.5	2.5	–	–	–	–	–	1.0	2.5	–	–	–	MHz
			10	–	–	3.0	6.0	–	–	–	–	–	2.5	6.0	–	–	–	
			15	–	–	–	8.0	–	–	–	–	–	–	8.0	–	–	–	
Maximum Clock Pulse Rise and Fall Time (C_L = 15 pF)		t_r, t_f	5.0	–	–	15	–	–	–	–	–	–	15	–	–	–	–	μs
			10	–	–	15	–	–	–	–	–	–	15	–	–	–	–	
A, B Input Setup Time (C_L = 15 pF)		t_{setup}	5.0	–	–	–	35	70	–	–	–	–	–	35	100	–	–	ns
			10	–	–	–	15	30	–	–	–	–	–	15	45	–	–	
			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Minimum High Level AE, P/S, A/S Pulse Width (C_L = 15 pF)		PW	5.0	–	–	–	200	400	–	–	–	–	–	200	600	–	–	ns
			10	–	–	–	90	180	–	–	–	–	–	90	270	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

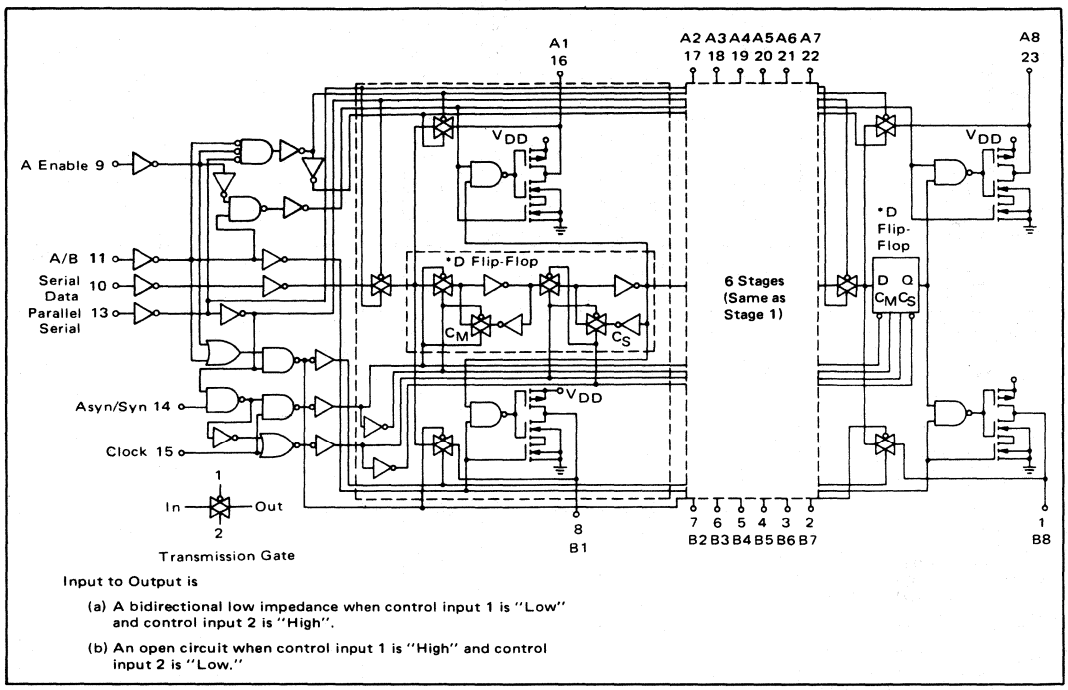
TRUTH TABLE

"A" Enable	P/S	A/B	A/S	MODE	OPERATION†
0	0	0	X	Serial	Synchronous Serial data input, A and B parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous serial data input, B-Parallel data output.
1	1	0	0	Parallel	B-Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B-Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A-Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A-Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

†Outputs change at positive transition of clock in the serial mode and when the A/S input is low in the parallel mode.
During transfer from parallel to serial operation, A/S should remain low in order to prevent D_S transfer into flip-flops.

LOGIC DIAGRAM



Input to Output is

(a) A bidirectional low impedance when control input 1 is "Low" and control input 2 is "High".

(b) An open circuit when control input 1 is "High" and control input 2 is "Low."

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

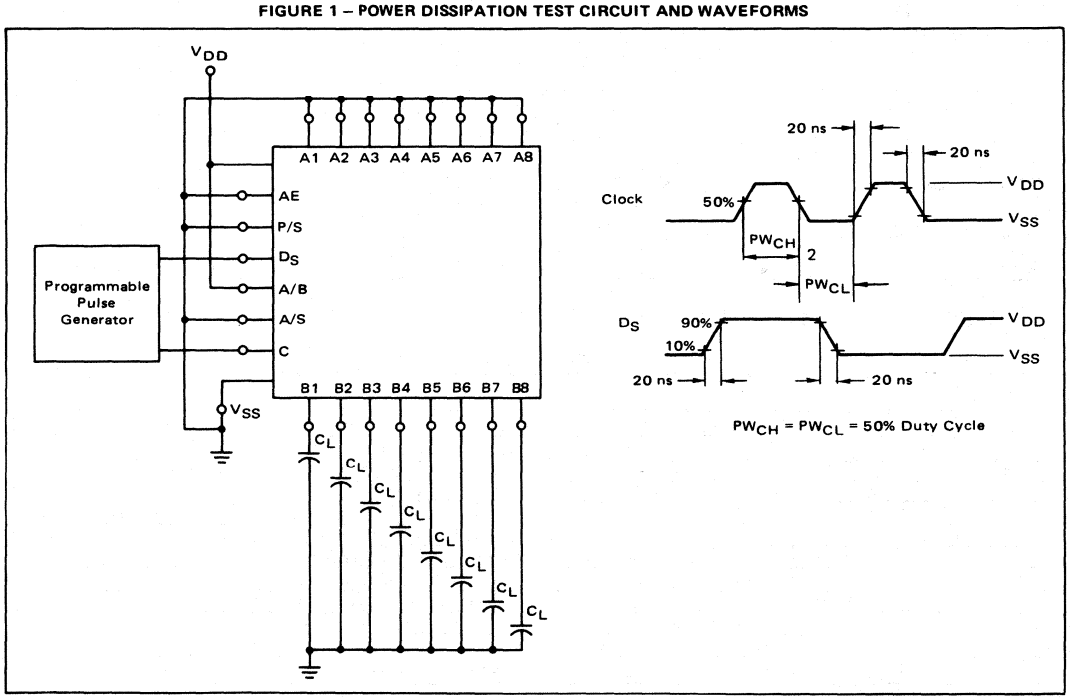


FIGURE 2 – TYPICAL POWER DISSIPATION CHARACTERISTICS

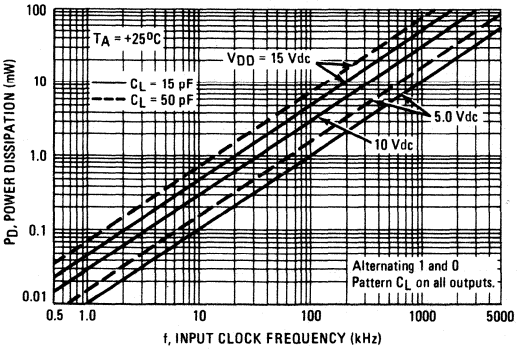
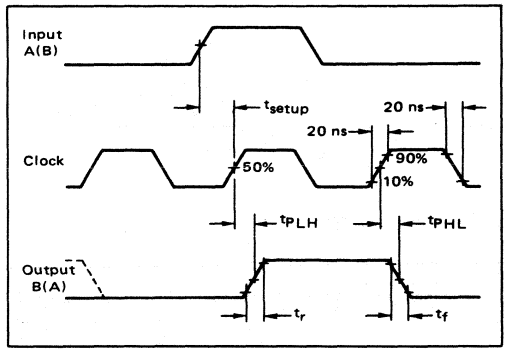


FIGURE 3 – PROPAGATION DELAY AND TRANSITION TIMES WAVEFORMS



PROPAGATION AND TRANSITION TIME TEST CIRCUITS

FIGURE 4 – A SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME

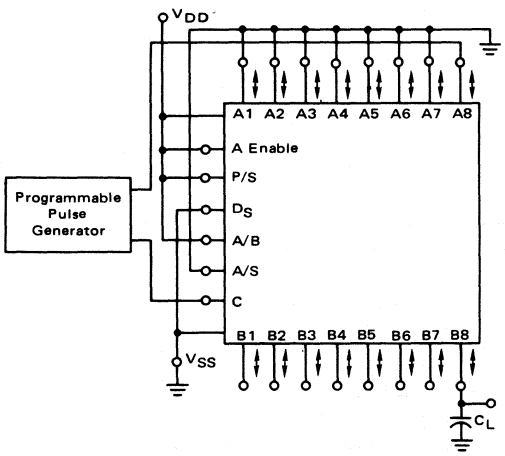
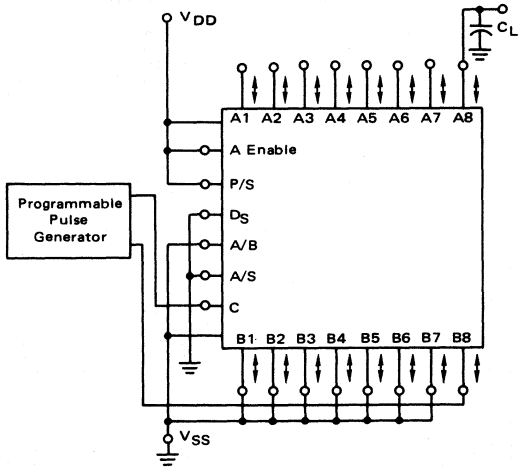


FIGURE 5 – B SYNCHRONOUS DATA INPUT, B PARALLEL DATA OUTPUT AND SETUP TIME



APPLICATIONS

FIGURE 6 – 16-BIT PARALLEL IN/PARALLEL OUT, PARALLEL IN/SERIAL OUT, SERIAL IN/PARALLEL OUT, SERIAL IN/SERIAL OUT REGISTER

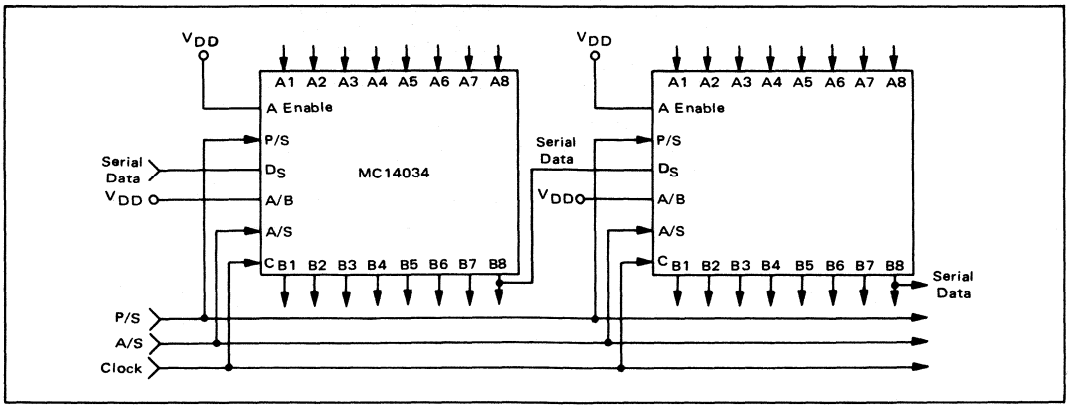
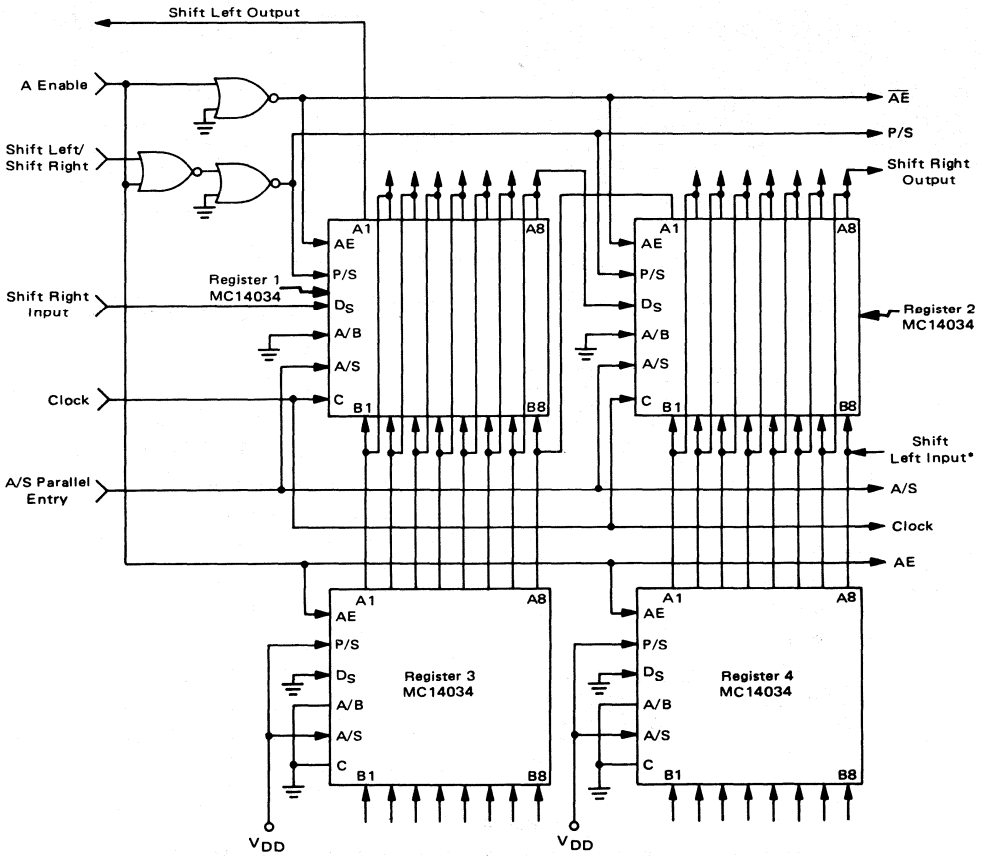


FIGURE 7 – SHIFT RIGHT/SHIFT LEFT WITH PARALLEL INPUTS



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Reg. 1 and 2 and enables the "A" data lines on registers 3 and 4 and allows parallel data into registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Reg. 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

MC14035AL
MC14035CL
MC14035CP

4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

The MC14035 4-bit shift register is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. It consists of a 4-stage clocked serial-shift register with synchronous parallel inputs and buffered parallel outputs. The Parallel/Serial (P/S) input allows serial-right shifting of data or synchronous parallel loading via inputs D_{P0} thru D_{P3}. The True/Complement (T/C) input determines whether the outputs display the Q or $\overline{Q}$ outputs of the flip-flop stages. J-$\overline{K}$ logic forms the serial input to the first stage. With the J and $\overline{K}$ inputs connected together they operate as a serial "D" input. Additional characteristics can be found on the Family Data Sheet.

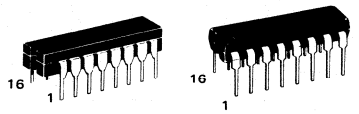
This device may be effectively used for shift-right/shift-left registers, parallel-to-serial/serial-to-parallel conversion, sequence generation, up/down Johnson or ring counters, pseudo-random code generation, frequency and phase comparators, sample and hold registers, etc. . .

- 4-Stage Clocked Serial-Shift Operation
- Synchronous Parallel Loading of all Four Stages
- J-$\overline{K}$ Serial Inputs on First Stage
- Asynchronous True/Complement Control of all Outputs
- Fully Static Operation
- Asynchronous Master Reset
- Data Transfer Occurs on the Positive-Going Clock Transition
- No Limit on Clock Rise and Fall Times
- All Inputs are Buffered
- 6.0 MHz Operation @ V_{DD} = 10 Vdc

McMOS

(LOW-POWER COMPLEMENTARY MOS)

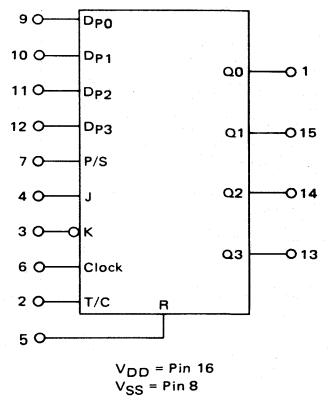
4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14035AL —MC14035CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14035AL —MC14035CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS				t_n OUTPUT
C	J	$\overline{K}$	R	Q0
⎍	0	0	0	0
⎍	0	1	0	Q0 (n - 1)
⎍	1	0	0	$\overline{Q0}$ (n - 1)
⎍	1	1	0	1
⎎	x	x	0	Q0 (n - 1)
x	x	x	1	0

x = Don't Care
P/S = 0 = Serial Mode
T/C = 1 = True Outputs

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD}	MC14035AL							MC14035CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
			Vdc	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation **†	–	P_Q																mW
(C_L = 15 pF, f = 0Hz)			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
			10	–	0.10	–	0.0001	0.10	–	6.0	–	1.0	–	0.0001	1.0	–	14	
			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Power Dissipation (Dynamic plus Quiescent) (C_L = 15 pF)	–	P_D	5.0	P_D = (3.25 mW/MHz) f + 0.000025 mW														mW
			10	P_D = (13 mW/MHz) f + 0.0001 mW														
			15	P_D = (30 mW/MHz) f + 0.00023 mW														
Output Rise Time** (C_L = 15 pF)	–	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time ** (C_L = 15 pF)	–	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock to Q or $\overline{Q}$ Propagation Delay Time** (C_L = 15 pF)	1	t_{PLH} t_{PHL}																ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 223 ns			5.0	–	–	–	250	500	–	–	–	–	–	250	700	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 89 ns			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 67 ns			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Reset to Q or $\overline{Q}$ Propagation Delay Time** (C_L = 15 pF)	–	t_{PHL} t_{PLH}																ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 223 ns			5.0	–	–	–	250	500	–	–	–	–	–	250	700	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 89 ns			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 67 ns			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	1	PW_C																ns
			5.0	–	–	–	135	335	–	–	–	–	–	135	500	–	–	
			10	–	–	–	45	165	–	–	–	–	–	45	250	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Minimum Reset Pulse Width (C_L = 15 pF)	–	PW_R																ns
			5.0	–	–	–	80	400	–	–	–	–	–	80	500	–	–	
			10	–	–	–	40	175	–	–	–	–	–	40	200	–	–	
			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Maximum Clock Pulse Rise and Fall Time	–	t_r,t_f	5.0	No Maximum Limit									100	∞	–	–	–	µs
			10										100	∞	–	–	–	
			15										100	∞	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)	1	PRF																MHz
			5.0	–	–	1.5	2.5	–	–	–	–	–	1.0	2.5	–	–	–	
			10	–	–	3.0	6.0	–	–	–	–	–	2.0	6.0	–	–	–	
			15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
J-$\overline{K}$ Setup Time (C_L = 15 pF)	1	t_{setup}																ns
			5.0	–	–	–	120	500	–	–	–	–	–	120	750	–	–	
			10	–	–	–	50	200	–	–	–	–	–	50	250	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
P/S Control Setup Time (C_L = 15 pF)	1	t_{setup}																ns
			5.0	–	–	–	25	500	–	–	–	–	–	25	750	–	–	
			10	–	–	–	10	200	–	–	–	–	–	10	250	–	–	
			15	–	–	–	7.5	–	–	–	–	–	–	7.5	–	–	–	
Parallel Input Setup Time (C_L = 15 pF)	1	t_{setup}																ns
			5.0	–	–	–	90	500	–	–	–	–	–	90	750	–	–	
			10	–	–	–	20	200	–	–	–	–	–	20	250	–	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

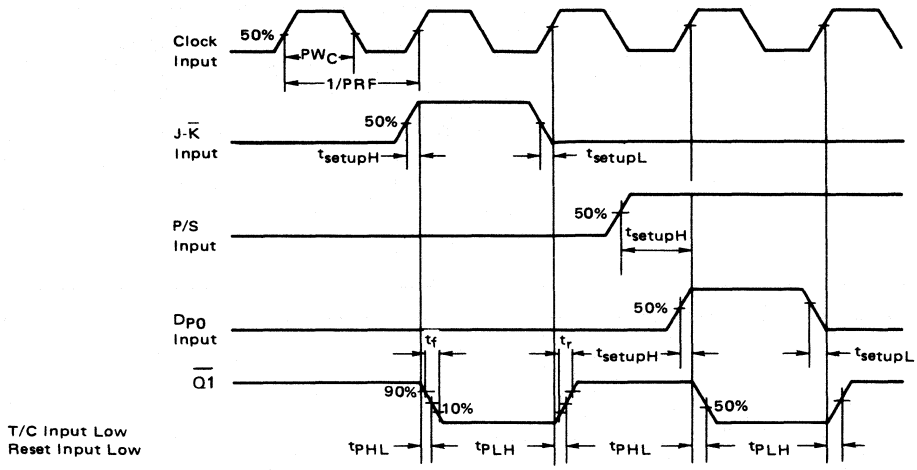
**The formula given is for the typical characteristics only.

†For dissipation at different external Load Capacitance (C_L) refer to corresponding formula:

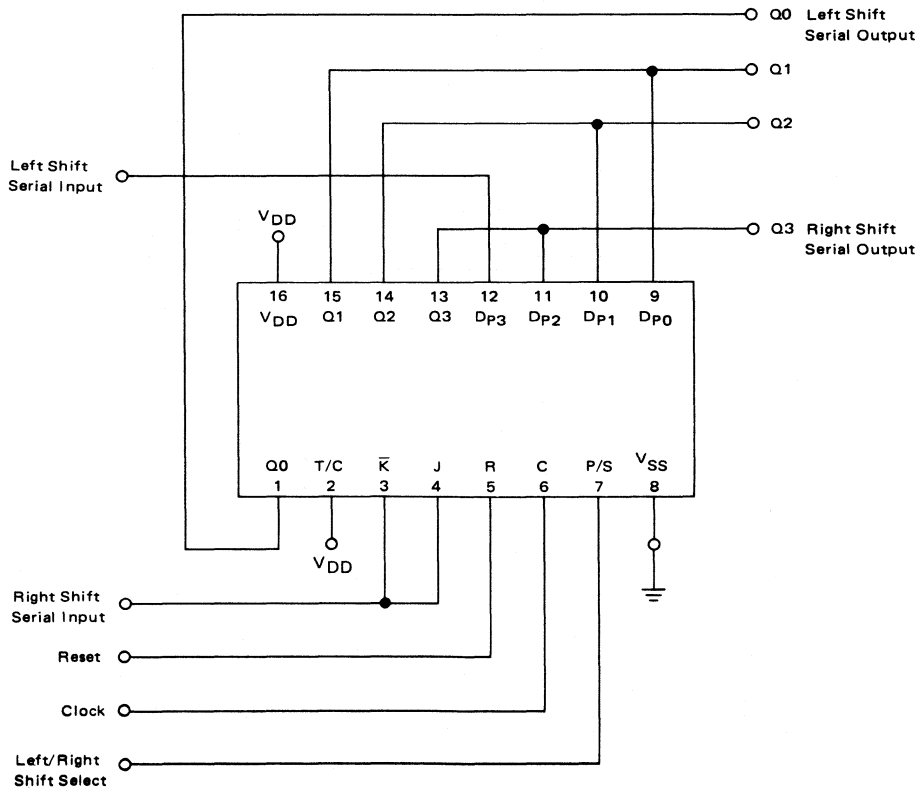
$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$

where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

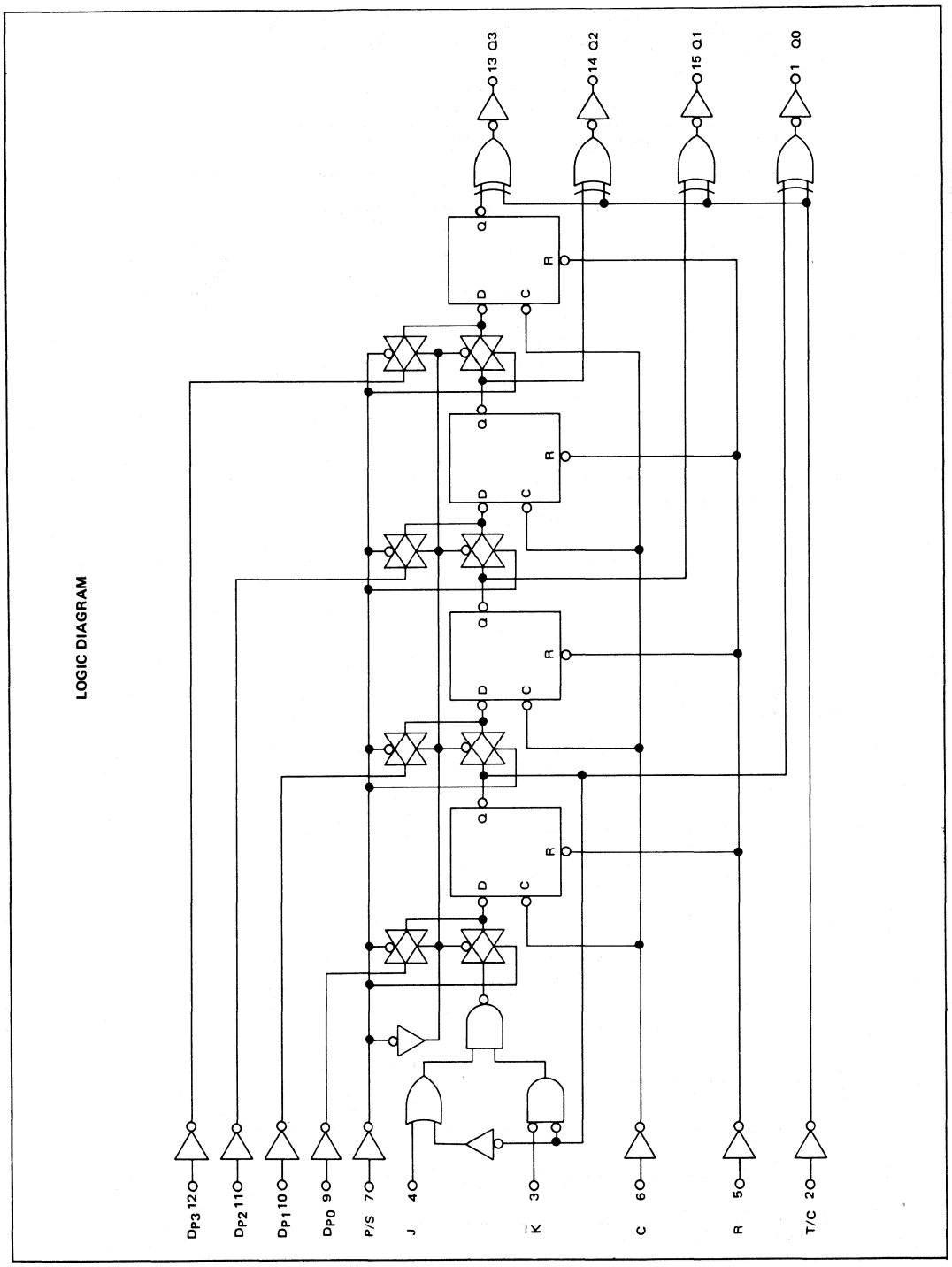
FIGURE 1 – TIMING DIAGRAM



APPLICATION DIAGRAM
Shift Left/Shift Right Register



LOGIC DIAGRAM



MC14040AL
MC14040CL
MC14040CP

12-BIT BINARY COUNTER

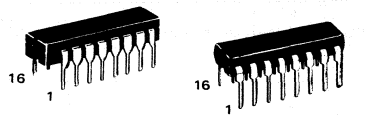
The MC14040 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50 nW/package typical @ V_{DD} = 5.0 V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14040AL)
  = 3.0 Vdc to 16 Vdc (MC14040CL/CP)
- Low Input Capacitance = 5.0 pF typical
- All 12 Buffered Outputs Available
- Common Reset Line
- 13 MHz Typical Counting Rate @ V_{DD} = 15 V
- Pin-for-Pin Replacement for CD4040A

McMOS

(LOW-POWER COMPLEMENTARY MOS)

12-BIT BINARY COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

CLOCK	RESET	OUTPUT STATE
⌐‾	0	No Change
‾⌐	0	Advance to next state
X	1	All Outputs are low

X = Don't Care

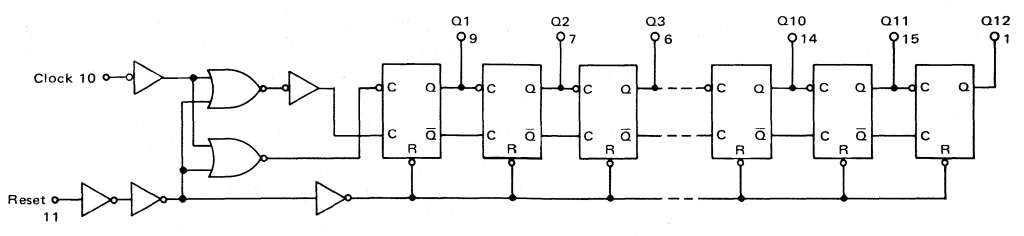
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14040AL MC14040CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14040AL —MC14040CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



Q4 = Pin 5 Q7 = Pin 4
Q5 = Pin 3 Q8 = Pin 13
Q6 = Pin 2 Q9 = Pin 12

V_{DD} = Pin 16
V_{SS} = Pin 8

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14040AL -55°C Min	MC14040AL -55°C Max	MC14040AL +25°C Min	MC14040AL +25°C Typ	MC14040AL +25°C Max	MC14040AL +125°C Min	MC14040AL +125°C Max	MC14040CL/CP -40°C Min	MC14040CL/CP -40°C Max	MC14040CL/CP +25°C Min	MC14040CL/CP +25°C Typ	MC14040CL/CP +25°C Max	MC14040CL/CP +85°C Min	MC14040CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source	–		5.0	-0.62	–	-0.5	-1.7	–	-0.35	–	-0.23	–	-0.2	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	0.23	–	0.2	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.0	–	0.65	–	0.6	–	0.5	2.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**†	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (1.2 mW/MHz) f + 0.00005 mW			5.0	–	0.025	–	0.00005	0.025	–	1.5	–	0.25	–	0.00005	0.25	–	3.5	
P_D = (5.0 mW/MHz) f + 0.0002 mW			10	–	0.10	–	0.0002	0.10	–	6.0	–	1.0	–	0.0002	1.0	–	14	
P_D = (13.5 mW/MHz) f + 0.0005 mW			15	–	–	–	0.0005	–	–	–	–	–	–	0.0005	–	–	–	
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 35 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 57 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock Turn-On, Turn-Off Delay Time**	2	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF)																		
Clock to Q1																		
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 324 ns			5.0	–	–	–	350	700	–	–	–	–	–	350	1050	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 130 ns			10	–	–	–	140	280	–	–	–	–	–	140	420	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 92 ns			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Clock to Q12																		
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 2474 ns			5.0	–	–	–	2.5	5.0	–	–	–	–	–	2.5	7.5	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 890 ns			10	–	–	–	0.9	1.8	–	–	–	–	–	0.9	2.7	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 492 ns			15	–	–	–	0.5	–	–	–	–	–	–	0.5	–	–	–	
Reset Turn-On Delay Time**	–	t_{PHL}																ns
(C_L = 15 pF)																		
Reset on Q_n																		
t_{PHL} = (1.75 ns/pF) C_L + 514 ns			5.0	–	–	–	540	1080	–	–	–	–	–	540	1620	–	–	
t_{PHL} = (0.70 ns/pF) C_L + 190 ns			10	–	–	–	200	400	–	–	–	–	–	200	600	–	–	
t_{PHL} = (0.53 ns/pF) C_L + 152 ns			15	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
Minimum Clock Pulse Width	–	PW_C	5.0	–	–	–	140	250	–	–	–	–	–	140	385	–	–	ns
(C_L = 15 pF)			10	–	–	–	55	100	–	–	–	–	–	55	150	–	–	
			15	–	–	–	38	–	–	–	–	–	–	38	–	–	–	
Maximum Clock Pulse Frequency	–	PRF	5.0	–	–	2.0	3.5	–	–	–	–	–	1.5	3.5	–	–	–	MHz
(C_L = 15 pF)			10	–	–	5.0	9.0	–	–	–	–	–	3.5	9.0	–	–	–	
			15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	
Maximum Clock Rise and Fall Time	–	t_r, t_f	5.0								–	–	–	∞	100	–	–	μs
(C_L = 15 pF)			10				NO MAXIMUM LIMIT				–	–	–	∞	100	–	–	
			15								–	–	–	∞	–	–	–	
Minimum Reset Pulse Width	–	PW_R	5.0	–	–	–	320	640	–	–	–	–	–	320	960	–	–	ns
(C_L = 15 pF)			10	–	–	–	120	240	–	–	–	–	–	120	360	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

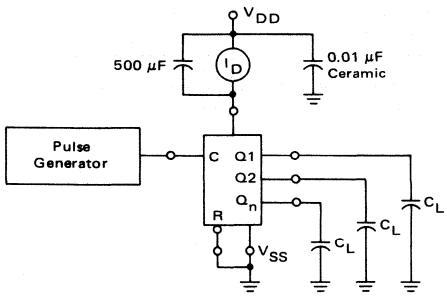
**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_D(C_L) = P_D + 1 \times 10^{-3} (C_L - 15) V_{DD}^2 f$ where:

P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



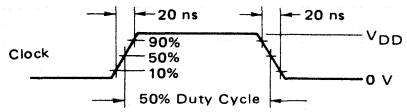
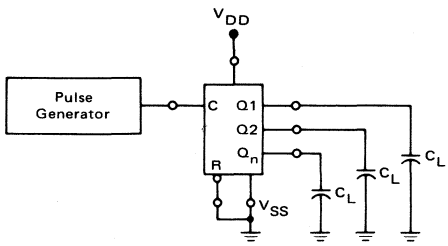


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



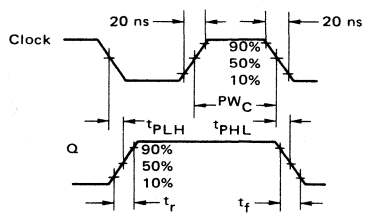


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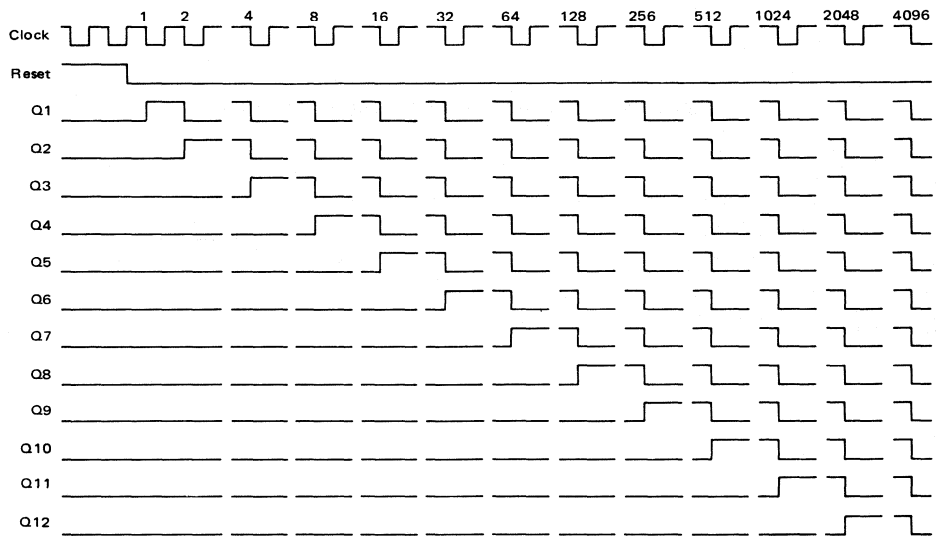
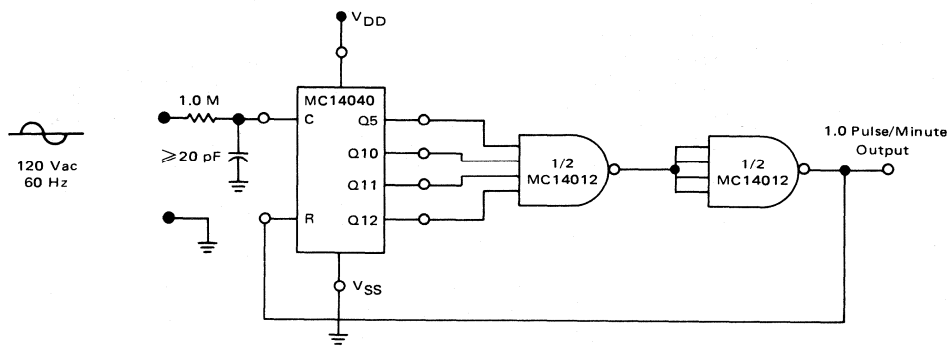
FIGURE 3 – TIMING DIAGRAM



APPLICATIONS INFORMATION

TIME-BASE GENERATOR

A 60 Hz sinewave obtained through a 1.0 Megohm resistor connected directly to a standard 120 Vac power line is applied to the clock input of the MC14040. By selecting outputs Q5, Q10, Q11, and Q12 division by 3600 is accomplished. The MC14040 decodes the counter outputs, produces a single output pulse, and resets the binary counter. The resulting output frequency is 1.0 pulse/minute.



MC14042AL
MC14042CL
MC14042CP

LATCH

Advance Information

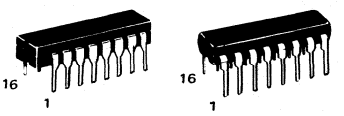
QUAD LATCH

The MC14042 quad latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

- Buffered Data Inputs
- Common Clock
- Positive or Negative Edge Clocked
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- No Limit on Clock Rise or Fall Times

McMOS
(LOW-POWER COMPLEMENTARY MOS)

QUAD LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 620

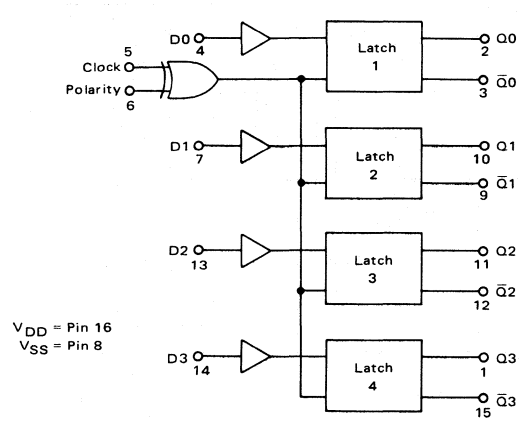
P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

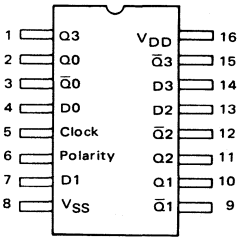
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14042AL MC14042CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14042AL MC14042CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

CLOCK	POLARITY	Q
0	0	Data
⌐	0	Latch
1	1	Data
¬	1	Latch

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

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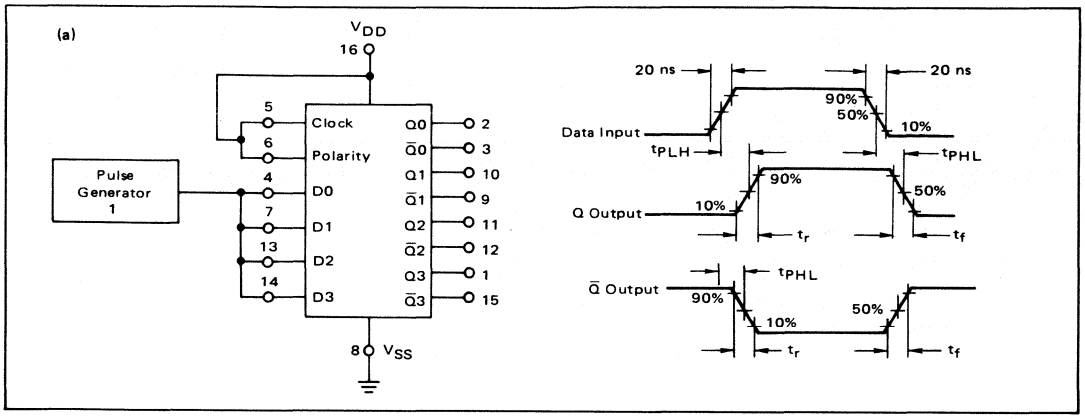
ELECTRICAL CHARACTERISTICS

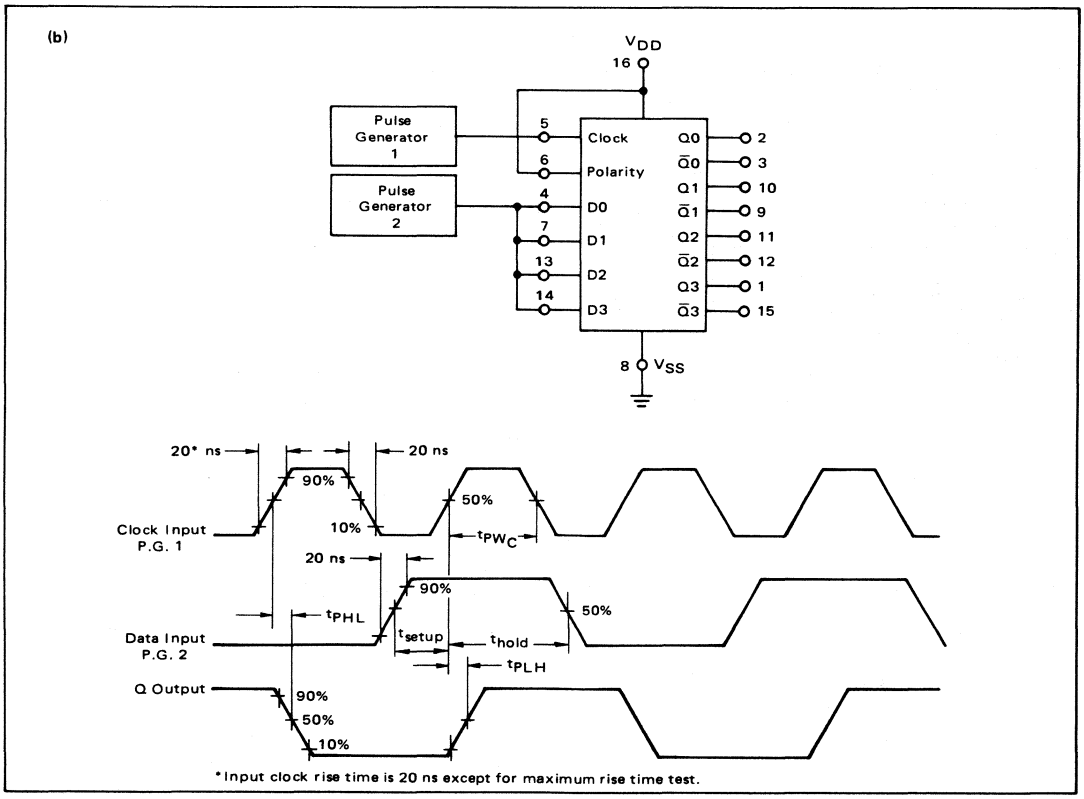
Characteristic	Figure	Symbol	V_{DD} Vdc	MC14042AL -55°C Min	MC14042AL -55°C Max	MC14042AL +25°C Min	MC14042AL +25°C Typ	MC14042AL +25°C Max	MC14042AL +125°C Min	MC14042AL +125°C Max	MC14042CL/CP -40°C Min	MC14042CL/CP -40°C Max	MC14042CL/CP +25°C Min	MC14042CL/CP +25°C Typ	MC14042CL/CP +25°C Max	MC14042CL/CP +85°C Min	MC14042CL/CP +85°C Max	Unit
Output Voltage "0" Level (V_{in} = V_{SS}, V_{DD})	–	V_{out}																Vdc
			5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq$ 3.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq$ 7.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq$ 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
	–	V_{NH}																Vdc
($V_{out} \leq$ 1.5 Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq$ 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq$ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.5	–	-0.35	–	-0.23	–	-0.20	-1.5	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.50	–	0.40	1.0	–	0.28	–	0.23	–	0.20	1.0	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.2	–	0.65	–	0.60	–	0.50	2.2	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Capacitance	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5	–	–	–	–	–	–	5	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF, f = 0 Hz)	–	P_D																mW
			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.00025	0.25	–	3.5	
			10	–	0.05	–	0.00005	0.05	–	5.0	–	0.5	–	0.0005	0.5	–	14	
			15	–	–	–	0.0002	–	–	–	–	–	–	0.002	–	–	–	
Typical Dynamic Power Dissipation (C_L = 15 pF)	–	P_{dyn}																mW
			5.0	P_{dyn} = (1.5 mW/MHz) f + 0.000025 mW														
			10	P_{dyn} = (6.0 mW/MHz) f + 0.00005 mW														
			15	P_{dyn} = (20 mW/MHz) f + 0.0002 mW														
Output Fall Time** (C_L = 15 pF)	1a	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Output Rise Time** (C_L = 15 pF)	1a	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	1b	t_{PW_C}																ns
			5.0	–	–	–	150	250	–	–	–	–	–	150	350	–	–	
			10	–	–	–	50	75	–	–	–	–	–	50	175	–	–	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Maximum Clock Rise Time	1b	t_{r_C}	5.0															
			10	NO LIMIT														
			15															
Hold Time (C_L = 15 pF)	1b	t_{hold}																ns
			5.0	–	–	–	50	100	–	–	–	–	–	50	125	–	–	
			10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Setup Time (C_L = 15 pF)	1b	t_{setup}																ns
			5.0	–	–	–	0	50	–	–	–	–	–	0	50	–	–	
			10	–	–	–	0	30	–	–	–	–	–	0	30	–	–	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
Turn-On, Turn-Off Delay Time (C_L = 15 pF) D to Q	1a	t_{PHL}, t_{PLH}																ns
			5.0	–	–	–	120	300	–	–	–	–	–	120	400	–	–	
			10	–	–	–	40	125	–	–	–	–	–	40	200	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
(C_L = 15 pF) Clock to $\overline{Q}$	1a	t_{PHL}, t_{PLH}																ns
			5.0	–	–	–	160	300	–	–	–	–	–	160	400	–	–	
			10	–	–	–	75	125	–	–	–	–	–	75	200	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
(C_L = 15 pF) D to Q	1a	t_{PHL}, t_{PLH}																ns
			5.0	–	–	–	150	300	–	–	–	–	–	150	400	–	–	
			10	–	–	–	60	125	–	–	–	–	–	60	200	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage charge from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – AC TEST CIRCUIT AND TIMING DIAGRAM





7

MC14049AL
MC14049CL
MC14049CP
MC14050AL
MC14050CL
MC14050CP

HEX BUFFERS

The MC14049 hex inverter/buffer and MC14050 noninverting hex buffer are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC}. The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters (V_{CC} = 5.0 V, $V_{OL} \leq$ 0.4 V, $I_{OL} \geq$ 3.2 mA). Note that pin 16 is not connected internally on these devices; consequently con nections to this terminal will not affect circuit operation.

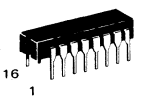
- Direct Drive of Two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5nw/package typical
- Single-Supply, Pin-for-Pin Replacements for Types MC14009 and MC14010 Respectively

McMOS

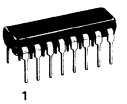
(LOW-POWER COMPLEMENTARY MOS)

HEX BUFFERS

Inverting – MC14049AL/CL/CP
Noninverting – MC14050AL/CL/CP



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

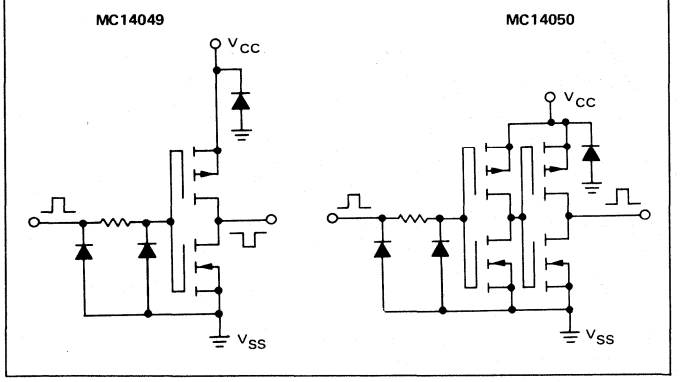
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

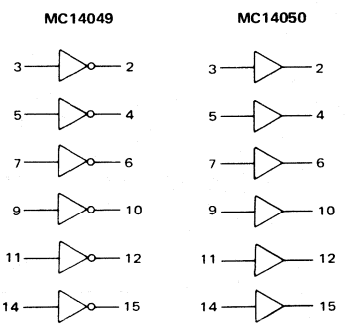
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	AL Version	V_{CC}	+18 to -0.5	Vdc
	CL,CP Version		+16 to -0.5	
Input Voltage, All Inputs		V_{in}	+18 to -0.5	Vdc
DC Current per Input Pin		I_{in}	10	mAdc
DC Current per Output Pin		I_{out}	45	mAdc
Operating Temperature Range	AL Version	T_A	-55 to +125	°C
	CL,CP Version		-40 to +85	
Storage Temperature Range		T_{stg}	-65 to +150	°C
Maximum Dissipation per Package		P_D	See Figure 1	

CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)



LOGIC DIAGRAMS



NC = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

NC = Pin 16
V_{SS} = Pin 8
V_{CC} = Pin 1

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{CC} Vdc	MC14049/050AL −55°C Min	MC14049/050AL −55°C Max	MC14049/050AL +25°C Min	MC14049/050AL +25°C Typ	MC14049/050AL +25°C Max	MC14049/050AL +125°C Min	MC14049/050AL +125°C Max	MC14049/050CL/CP −40°C Min	MC14049/050CL/CP −40°C Max	MC14049/050CL/CP +25°C Min	MC14049/050CL/CP +25°C Typ	MC14049/050CL/CP +25°C Max	MC14049/050CL/CP +85°C Min	MC14049/050CL/CP +85°C Max	Unit
Output Voltage "0" Level	2, 3	V_{out}																Vdc
MC14049																		
(V_{in} = 5.0 Vdc)			5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 10 Vdc)			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 15 Vdc)			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14050																		
(V_{in} = 0 Vdc)			5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{in} = 0 Vdc)			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
MC14049 "1" Level																		Vdc
(V_{in} = 0 Vdc)			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 0 Vdc)			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 0 Vdc)			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
MC14050																		
(V_{in} = 5.0 Vdc)			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
(V_{in} = 10 Vdc)			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
(V_{in} = 15 Vdc)			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	4	V_{NL}																Vdc
MC14049																		
(V_{out} ≥ 3.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.5	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≥ 7.0 Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{out} ≥ 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≤ 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤ 3.0 Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≤ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
MC14050		V_{NL}																Vdc
(V_{out} ≤ 1.5 Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
(V_{out} ≤ 3.0 Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
(V_{out} ≤ 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≥ 3.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≥ 7.0 Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
(V_{out} ≥ 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	6	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-1.85	–	-1.25	-2.5	–	-0.9	–	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	-1.85	–	-1.25	-2.5	–	-0.9	–	-1.5	–	-1.25	-2.5	–	-1.0	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-10	–	–	–	–	–	–	-1.0	–	–	–	
	7	I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	3.75	–	3.2	6.0	–	2.1	–	3.6	–	3.2	6.0	–	2.5	–	
(V_{OL} = 0.5 Vdc)			10	10	–	8.0	16	–	5.6	–	9.6	–	8.0	16	–	6.6	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance MC14049		C_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pF
MC14050			–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation (per package)		P_D	5.0	–	1.5	–	0.05	1.5	–	100	–	15	–	0.15	15	–	210	µW
			10	–	5.0	–	0.1	5.0	–	300	–	50	–	0.5	50	–	700	
			15	–	–	–	0.15	–	–	–	–	–	–	0.85	–	–	–	
Dynamic Power Dissipation (per Buffer)**		P_{dyn}																mW
(C_L = 15 pF) (Typical)			5.0	P_{dyn} = (0.6mW/MHz) f + 0.00001 mW														
			10	P_{dyn} = (3.0mW/MHz) f + 0.00002 mW														
			15	P_{dyn} = (6.0mW/MHz) f + 0.00003 mW														
Turn-On Delay Time † MC14049	8	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (0.38ns/pF) C_L + 25ns			5.0	–	–	–	30	55	–	–	–	–	–	30	70	–	–	
t_{PHL} = (0.12ns/pF) C_L + 17 ns			10	–	–	–	18	30	–	–	–	–	–	18	40	–	–	
t_{PHL} = (0.11ns/pF) C_L + 11 ns			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
MC14050																		
t_{PHL} = (0.2ns/pF) C_L + 45 ns			5.0	–	–	–	48	110	–	–	–	–	–	48	130	–	–	
t_{PHL} = (0.12ns/pF) C_L + 20ns			10	–	–	–	21	55	–	–	–	–	–	21	60	–	–	
t_{PHL} = (0.04ns/pF) C_L + 19ns			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	
Turn-Off Delay Time † MC14049	8	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (0.38ns/pF)C_L + 25ns			5.0	–	–	–	31	80	–	–	–	–	–	31	120	–	–	
t_{PLH} = (0.2ns/pF) C_L + 20ns			10	–	–	–	23	55	–	–	–	–	–	23	60	–	–	
t_{PLH} = (0.11ns/pF) C_L + 18 ns			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	
MC14050																		
t_{PLH} = (0.33ns/pF) C_L + 53ns			5.0	–	–	–	58	140	–	–	–	–	–	58	200	–	–	
t_{PLH} = (0.19ns/pF) C_L + 24ns			10	–	–	–	27	85	–	–	–	–	–	27	100	–	–	
t_{PLH} = (0.06ns/pF) C_L + 20ns			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Output Rise Time † MC14049	8	t_r																ns
(C_L = 15 pF)																		
t_r = (0.81ns/pF) C_L + 22ns			5.0	–	–	–	23	100	–	–	–	–	–	23	160	–	–	
t_r = (0.31ns/pF) C_L + 23ns			10	–	–	–	28	60	–	–	–	–	–	28	100	–	–	
t_r = (0.27ns/pF) C_L + 21ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
MC14050																		
t_r = (0.7ns/pF) C_L + 20ns			5.0	–	–	–	21	100	–	–	–	–	–	21	160	–	–	
t_r = (0.36ns/pF) C_L + 10ns			10	–	–	–	15	60	–	–	–	–	–	15	100	–	–	
t_r = (0.22ns/pF) C_L + 11ns			15	–	–	–	14	–	–	–	–	–	–	14	–	–	–	
Output Fall Time † MC14049	8	t_f																ns
(C_L = 15 pF)																		
t_f = (0.31ns/pF) C_L + 16ns			5.0	–	–	–	20	45	–	–	–	–	–	20	60	–	–	
t_f = (0.12ns/pF) C_L + 12ns			10	–	–	–	14	40	–	–	–	–	–	14	50	–	–	
t_f = (0.1ns/pF) C_L + 10ns			15	–	–	–	11	–	–	–	–	–	–	11	–	–	–	
MC14050																		
t_f = (0.2ns/pF) C_L + 20ns			5.0	–	–	–	23	45	–	–	–	–	–	23	60	–	–	
t_f = (0.06ns/pF) C_L + 14ns			10	–	–	–	15	40	–	–	–	–	–	15	50	–	–	
t_f = (0.035ns/pF) C_L + 13ns			15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	

*DC Noise Margin is defined as the maximum voltage change V_{NH} (down from a V_{CC} level input) and V_{NL} (up from a ground level input) before producing an output state change.

**For dynamic power dissipation per package, use the formula: P_{dyn} (C_L, V_{CC}, f) = P_D + 10^{-3} (C_L - 15 pF) $V_{CC}^2 f$ where P_D is in mW, C_L in pF, V_{CC} in volts, f in MHz, and all outputs driving C_L.

† Equations shown are for typical values only.

FIGURE 1 – AMBIENT TEMPERATURE POWER DERATING

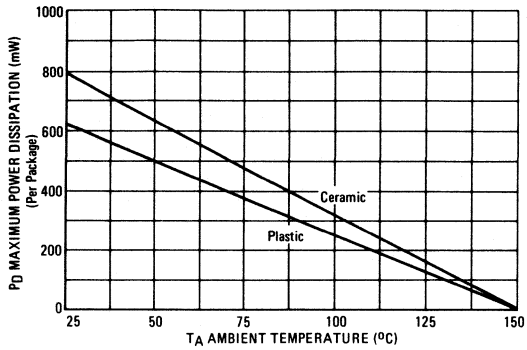
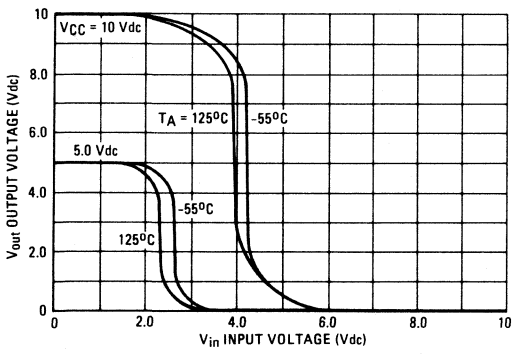
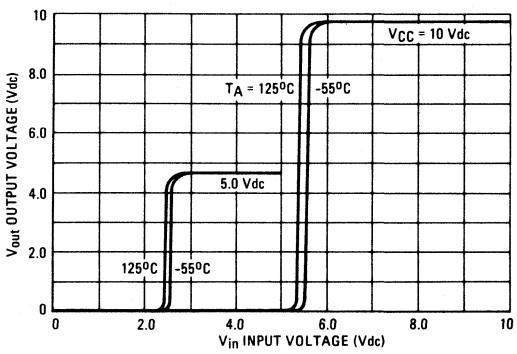


FIGURE 2 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

MC14049



MC14050



7

FIGURE 3 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

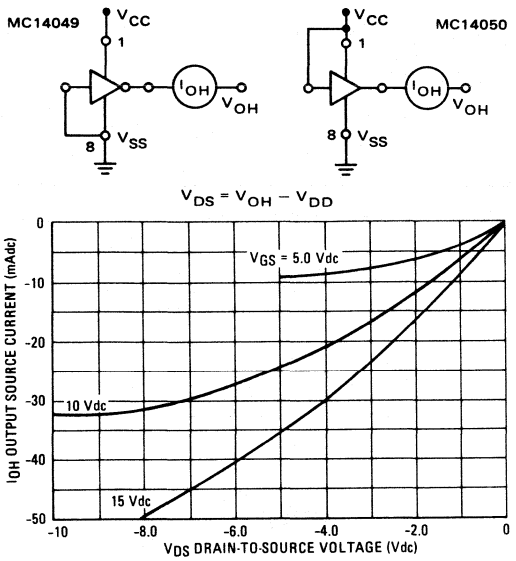


FIGURE 4 – TYPICAL OUTPUT SINK CHARACTERISTICS

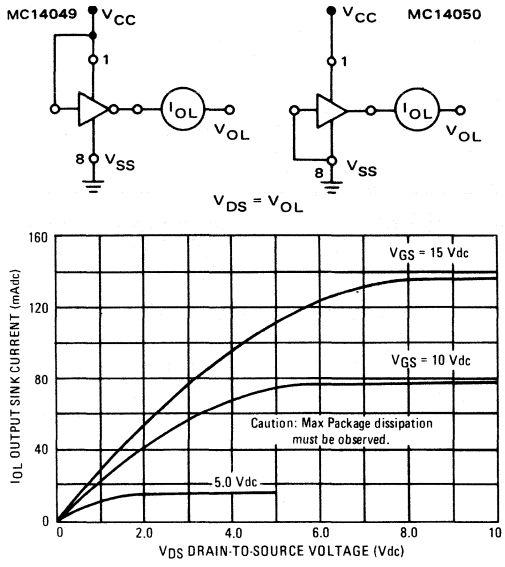
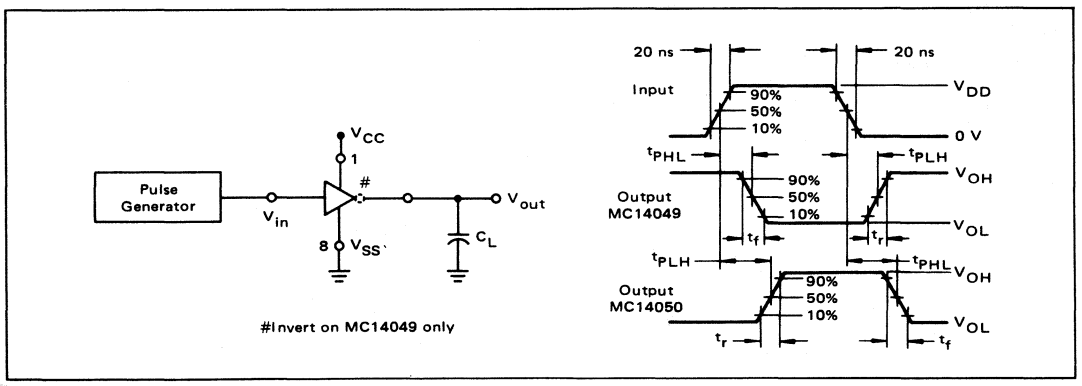


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



MC14501AL
MC14501CL
MC14501CP

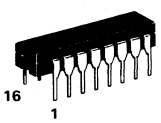
TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE

The MC14501 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

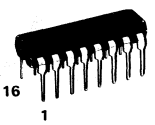
- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14501AL)
  = 3.0 Vdc to 16 Vdc (MC14501CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS
(LOW-POWER COMPLEMENTARY MOS)

TRIPLE GATE
DUAL 4-INPUT "NAND" GATE
2-INPUT "NOR/OR" GATE
8-INPUT "AND/NAND" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

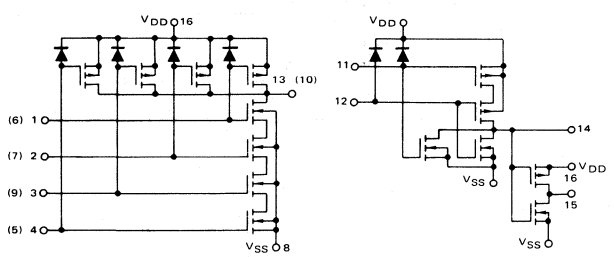


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14501AL MC14501CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14501AL – MC14501CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

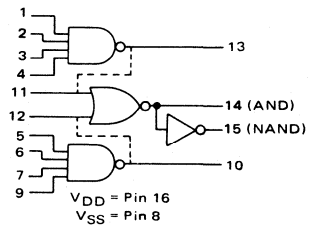
CIRCUIT SCHEMATIC



Numbers in parenthesis are for second 4-input gate.

LOGIC DIAGRAM
(POSITIVE LOGIC)

Use Dotted Connection Externally



Note: Pin 14 must not be used as an input to the inverter.

See Mechanical Data Section for package dimensions.

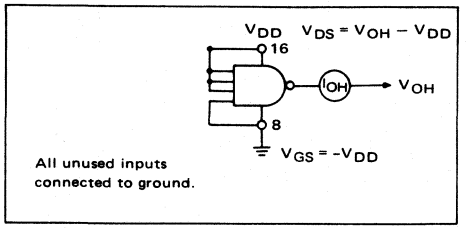
ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD}	MC14501AL -55°C Min	MC14501AL -55°C Max	MC14501AL +25°C Min	MC14501AL +25°C Typ	MC14501AL +25°C Max	MC14501AL +125°C Min	MC14501AL +125°C Max	MC14501CL/CP -40°C Min	MC14501CL/CP -40°C Max	MC14501CL/CP +25°C Min	MC14501CL/CP +25°C Typ	MC14501CL/CP +25°C Max	MC14501CL/CP +85°C Min	MC14501CL/CP +85°C Max	Unit
Output Voltage	"0" Level	3,4,5	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																			
($V_{out} \geq 3.5$ Vdc)			V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)				10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)				10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current			I_{OH}																
(V_{OH} = 2.5 Vdc)	Source	1		5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)	NAND			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OH} = 2.5 Vdc)	NOR	6		5.0	-0.84	–	-0.7	-3.0	–	-0.5	–	-0.36	–	-0.3	-3.0	–	-0.24	–	mAdc
(V_{OH} = 9.5 Vdc)				10	-0.84	–	-0.7	-1.5	–	-0.5	–	-0.36	–	-0.3	-1.5	–	-0.24	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-6.0	–	–	–	–	–	–	-6.0	–	–	–	
(V_{OH} = 2.5 Vdc)	NOR-	8		5.0	-1.8	–	-1.5	-5.0	–	-1.0	–	-0.72	–	-0.6	-5.0	–	-0.49	–	mAdc
(V_{OH} = 9.5 Vdc)	Inverter			10	-1.8	–	-1.5	-3.0	–	-1.0	–	-0.72	–	-0.6	-3.0	–	-0.49	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-12	–	–	–	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)	NAND			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
(V_{OL} = 0.4 Vdc)	NOR	7		5.0	0.62	–	0.5	1.0	–	0.35	–	0.3	–	0.25	1.0	–	0.17	–	mAdc
(V_{OL} = 0.5 Vdc)				10	1.36	–	1.1	2.3	–	0.8	–	0.72	–	0.6	2.3	–	0.49	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
(V_{OL} = 0.4 Vdc)	NOR-	9		5.0	0.74	–	0.6	1.3	–	0.4	–	0.36	–	0.3	1.3	–	0.24	–	mAdc
(V_{OL} = 0.5 Vdc)	Inverter			10	1.8	–	1.5	3.4	–	1.1	–	0.84	–	0.7	3.4	–	0.57	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	13	–	–	–	–	–	–	13	–	–	–	
Input Current			I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)			C_{in}	–	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	pF
Quiescent Dissipation		10,11	P_D	5.0	–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	μW
				10	–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
				15	–	–	–	2.0	–	–	–	–	–	–	2.0	–	–	–	
Output Rise Time (C_L = 15 pF)			t_r																ns
	NAND	12		5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
	NOR	13,14		5.0	–	–	–	70	125	–	–	–	–	–	70	150	–	–	ns
				10	–	–	–	30	65	–	–	–	–	–	30	95	–	–	
				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
	NOR-INVERTER	13,14		5.0	–	–	–	30	65	–	–	–	–	–	30	95	–	–	ns
				10	–	–	–	20	45	–	–	–	–	–	20	70	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Output Fall Time (C_L = 15 pF)			t_f																ns
	NAND	–		5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
	NOR	13,15		5.0	–	–	–	70	125	–	–	–	–	–	70	150	–	–	ns
				10	–	–	–	30	65	–	–	–	–	–	30	95	–	–	
				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
	NOR-INVERTER	13,15		5.0	–	–	–	30	65	–	–	–	–	–	30	95	–	–	ns
				10	–	–	–	20	45	–	–	–	–	–	20	70	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Turn-on Delay Time (C_L = 15 pF)			t_{PHL}																ns
	NAND	–		5.0	–	–	–	60	150	–	–	–	–	–	60	200	–	–	
				10	–	–	–	25	100	–	–	–	–	–	25	150	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
	NOR	16		5.0	–	–	–	45	60	–	–	–	–	–	40	75	–	–	ns
				10	–	–	–	20	40	–	–	–	–	–	20	60	–	–	
				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	
	NOR-INVERTER	16		5.0	–	–	–	60	75	–	–	–	–	–	60	100	–	–	ns
				10	–	–	–	25	50	–	–	–	–	–	25	60	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Turn-of Delay Time (C_L = 15 pF)			t_{PLH}																ns
	NAND	–		5.0	–	–	–	60	150	–	–	–	–	–	60	200	–	–	
				10	–	–	–	25	100	–	–	–	–	–	25	150	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
	NOR	17		5.0	–	–	–	45	60	–	–	–	–	–	45	–	–	–	ns
				10	–	–	–	20	40	–	–	–	–	–	20	–	–	–	
				15	–	–	–	18	–	–	–	–	–	–	18	–	–	–	
	NOR-INVERTER	17		5.0	–	–	–	60	75	–	–	–	–	–	60	–	–	–	ns
				10	–	–	–	25	50	–	–	–	–	–	25	–	–	–	
				15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

4-INPUT "NAND" GATE

FIGURE 1 – TYPICAL P-CHANNEL DRAIN CHARACTERISTICS



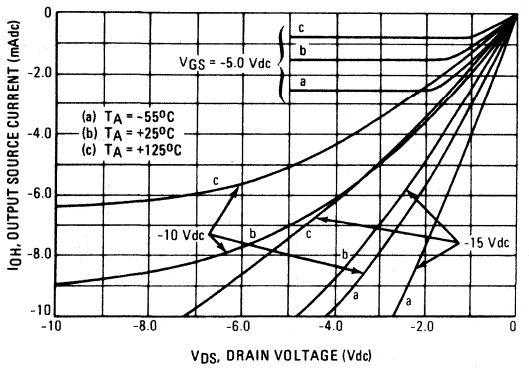
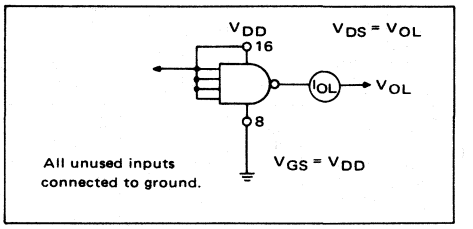
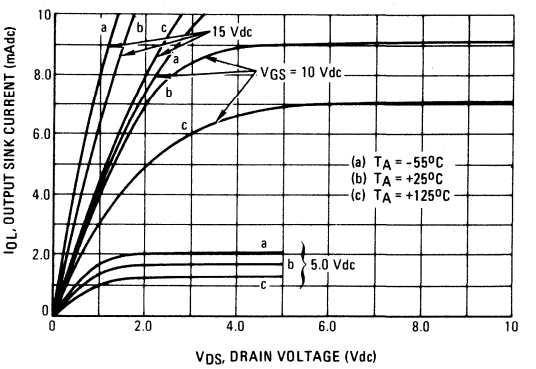


FIGURE 2 – TYPICAL N-CHANNEL DRAIN CHARACTERISTICS





2-INPUT "NOR-INVERTER"

FIGURE 3 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

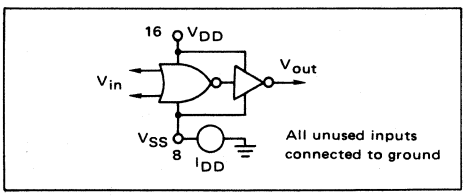


FIGURE 4 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

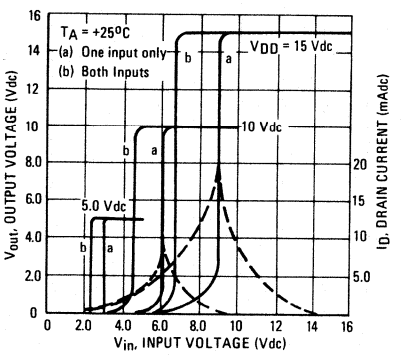
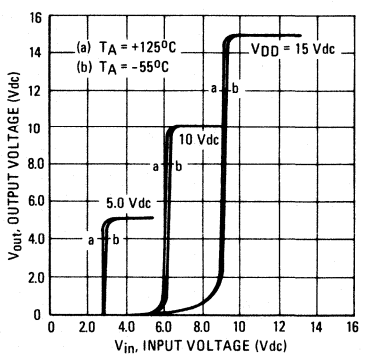


FIGURE 5 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE



7

2-INPUT "NOR-INVERTER" (continued)

FIGURE 6 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

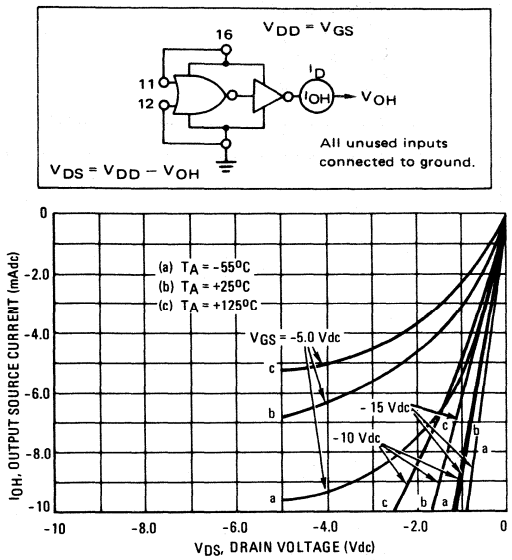
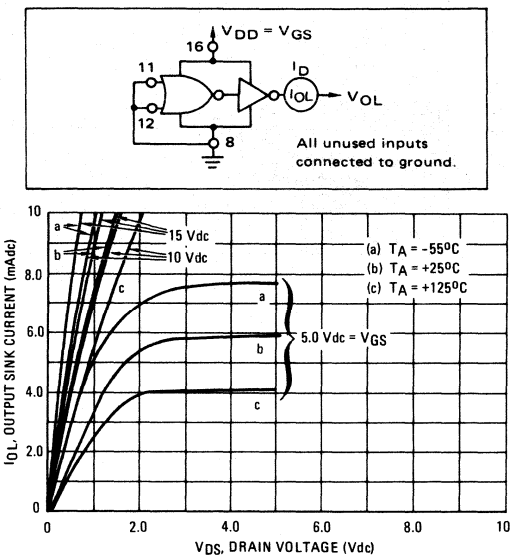


FIGURE 7 – TYPICAL OUTPUT SINK CHARACTERISTICS



2-INPUT "NOR" GATE

FIGURE 8 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

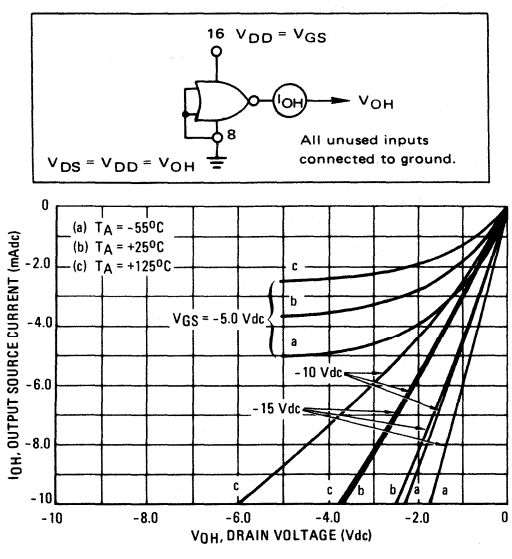
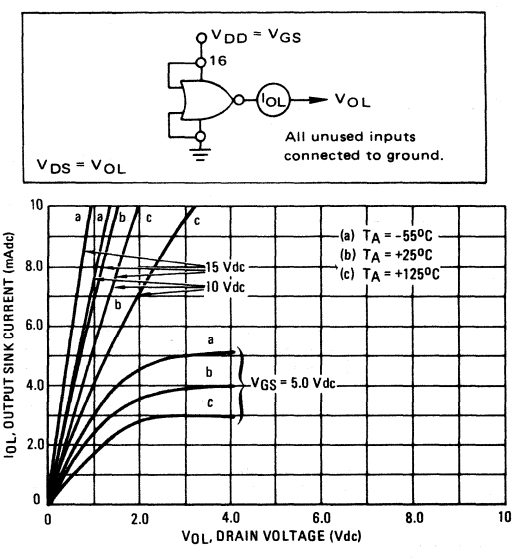


FIGURE 9 – TYPICAL OUTPUT SINK CHARACTERISTICS



7

2-INPUT "NOR" GATE (continued)

FIGURE 10 – TYPICAL POWER DISSIPATION versus FREQUENCY PER PACKAGE

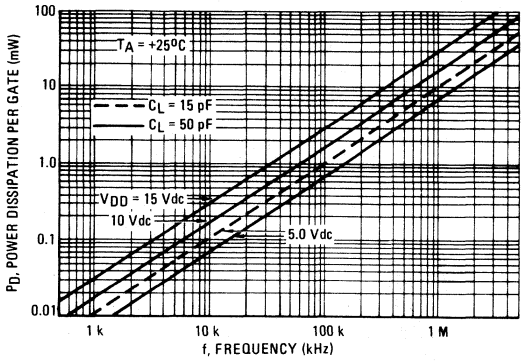
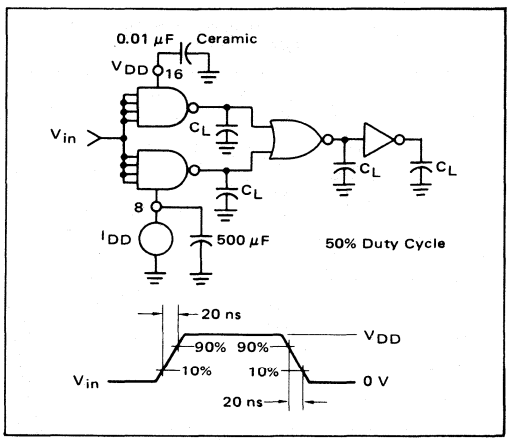
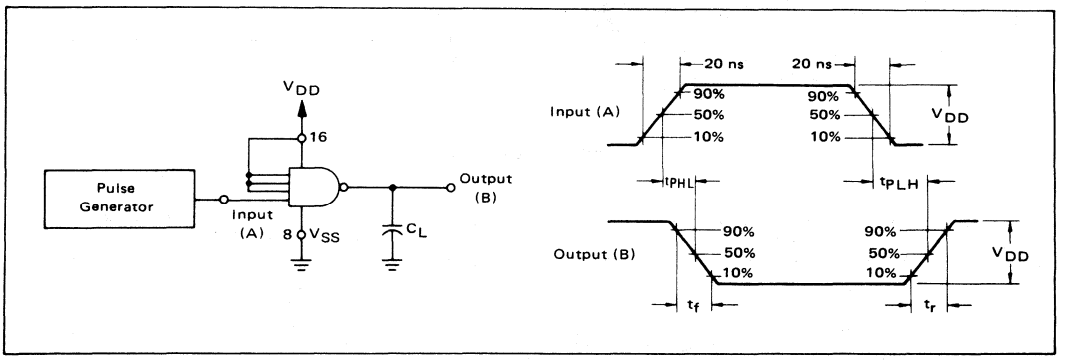


FIGURE 11 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



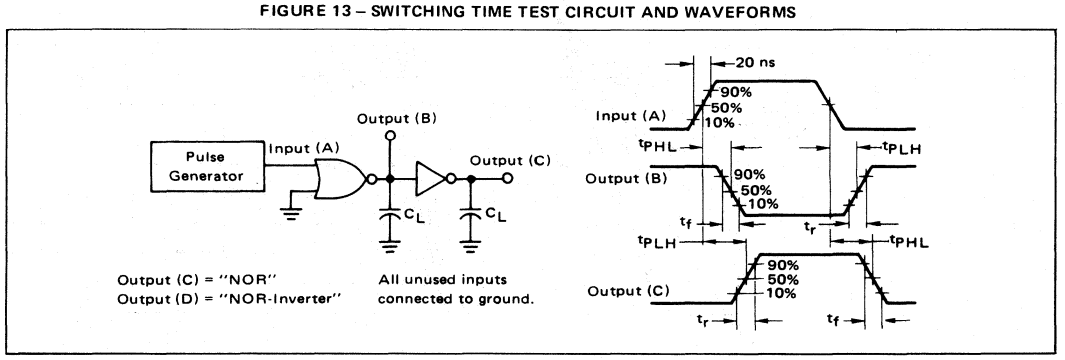
4-INPUT "NAND" GATE

FIGURE 12 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



"NOR" GATE and "NOR-INVERTER"

FIGURE 13 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

"NOR" GATE and "NOR-INVERTER" (continued)

FIGURE 14 – TYPICAL RISE TIME versus LOAD CAPACITANCE

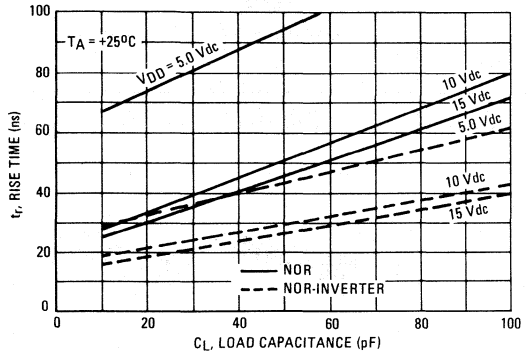


FIGURE 15 – TYPICAL FALL TIME versus LOAD CAPACITANCE

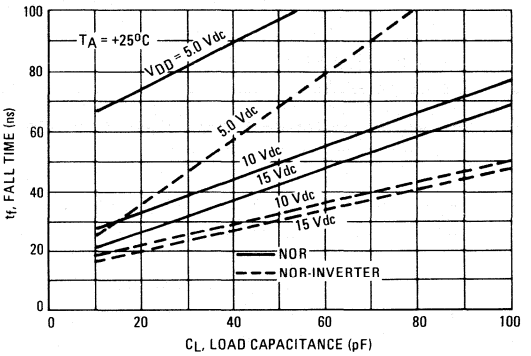


FIGURE 16 – TYPICAL TURN-ON DELAY TIME versus LOAD CAPACITANCE

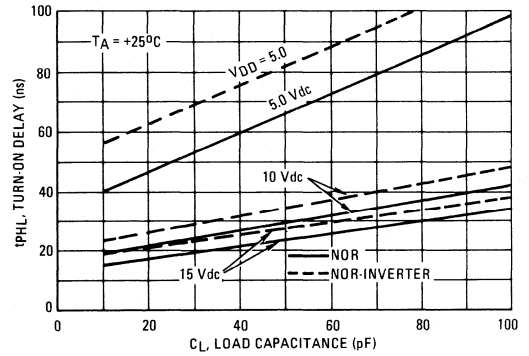
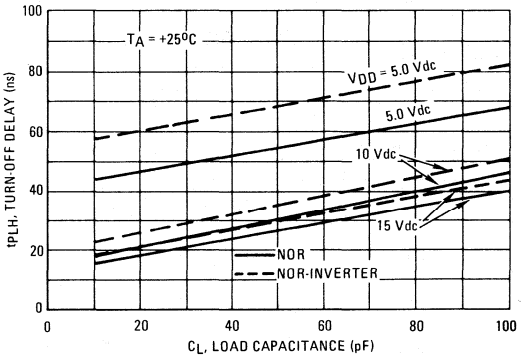


FIGURE 17 – TYPICAL TURN-OFF DELAY TIME versus LOAD CAPACITANCE



INPUT PROTECTION

Motorola McMOS circuits have built-in protection circuitry on all inputs to prevent device damage to the sensitive input gates that could result from improper testing or handling procedures prior to final assembly. This protection scheme is necessary because the extremely high impedance on the MOS gate oxide (approximately 10^{12} ohms) allows even a low energy source to generate a high enough potential (usually 100 volts) to rupture this gate oxide and thus destroy the device. While protection circuitry is effective in reducing over-voltages, it is expected that the user will take normal precautions to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

UNUSED INPUTS

Unused inputs must be connected to the supply voltage (V_{DD} or V_{SS}) that is appropriate for the system logic design.

MC14502AL
MC14502CL
MC14502CP

STROBED BUFFER

STROBED HEX INVERTER/BUFFER

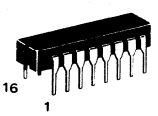
The MC14502 is a strobed hex buffer/inverter constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

This part has 3-state outputs, an output disable control, and guaranteed TTL drive over the temperature range. The 3-state output simplifies design by allowing common bus.

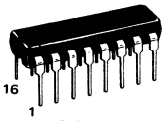
- Quiescent Power Dissipation = 100 nW/package typical
- Separate Output Disable Control
- 3-State Output
- TTL Output Drive Guaranteed Over the Temperature Range
- Output Impedance = 200 ohms @ 5.0 V Supply Guaranteed Over Full Temperature Range

McMOS
(LOW-POWER COMPLEMENTARY MOS)

STROBED HEX INVERTER/BUFFER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

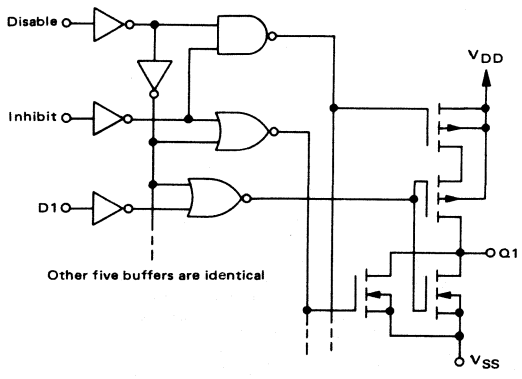
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14502AL MC14502CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range —	MC14502AL MC14502CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

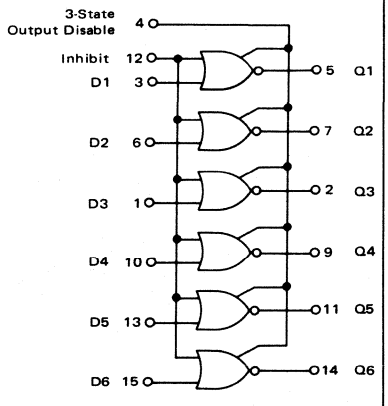
D_n	Inhibit	Disable	Q_n
0	0	0	1
1	0	0	0
X	1	0	0
X	X	1	High Impedance

X = Don't Care

CIRCUIT DIAGRAM



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14502AL -55°C Min	MC14502AL -55°C Max	MC14502AL +25°C Min	MC14502AL +25°C Typ	MC14502AL +25°C Max	MC14502AL +125°C Min	MC14502AL +125°C Max	MC14502CL/CP -40°C Min	MC14502CL/CP -40°C Max	MC14502CL/CP +25°C Min	MC14502CL/CP +25°C Typ	MC14502CL/CP +25°C Max	MC14502CL/CP +85°C Min	MC14502CL/CP +85°C Max	Unit
Output Voltage (V_{in} = V_{SS}, V_{DD}) "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–																	
(V_{out} = 3.5 Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} = 7.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} = 10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} = 1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} = 3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} = 4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	2,4	I_{OH}	5.0	-0.62	–	-0.5	-3.0	–	-0.8	–	-0.18	–	-0.2	-3.0	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.5	–	-0.75	–	-0.23	–	-0.2	-1.5	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-6.2	–	–	–	–	–	–	-6.2	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	3,5	I_{OL}	5.0	2.7	–	2.3	3.6	–	1.6	–	1.6	–	1.4	3.6	–	1.1	–	mAdc
(V_{OL} = 0.5 Vdc)			10	6.6	–	5.3	6.5	–	3.25	–	4.0	–	3.4	6.5	–	2.8	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	6,7	P_D	5.0	–	3.0	–	0.1	3.0	–	200	–	30	–	1.0	30	–	420	μW
			10	–	10	–	0.25	10	–	600	–	100	–	2.5	100	–	1400	
			15	–	–	–	0.4	–	–	–	–	–	–	4.0	–	–	–	
Output Rise Time**	8	t_r																ns
(C_L = 15 pF)																		
t_r = (1.2 ns/pF) C_L + 12 ns			5.0	–	–	–	60	175	–	–	–	–	–	60	200	–	–	
t_r = (0.56 ns/pF) C_L + 11 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (0.47 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	8	t_f																ns
(C_L = 15 pF)																		
t_f = (0.26 ns/pF) C_L + 16 ns			5.0	–	–	–	20	50	–	–	–	–	–	20	75	–	–	
t_f = (0.18 ns/pF) C_L + 12 ns			10	–	–	–	15	35	–	–	–	–	–	15	50	–	–	
t_f = (0.15 ns/pF) C_L + 9.0 ns			15	–	–	–	11	–	–	–	–	–	–	11	–	–	–	
Turn-On Delay Time**	8	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (0.18 ns/pF) C_L + 27 ns			5.0	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
t_{PHL} = (0.12 ns/pF) C_L + 18 ns			10	–	–	–	20	50	–	–	–	–	–	20	75	–	–	
t_{PHL} = (0.10 ns/pF) C_L + 15 ns			15	–	–	–	17	–	–	–	–	–	–	17	–	–	–	
Turn-Off Delay Time**	8	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (0.56 ns/pF) C_L + 31 ns			5.0	–	–	–	40	125	–	–	–	–	–	40	150	–	–	
t_{PLH} = (0.4 ns/pF) C_L + 24 ns			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
t_{PLH} = (0.36 ns/pF) C_L + 20 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
3-State Propagation Delay, Output "1" to High Impedance**	9	$t_{"1"H}$																ns
$t_{"1"H}$ = (0.6 ns/pF) C_L + 32 ns			5.0	–	–	–	40	125	–	–	–	–	–	40	150	–	–	
$t_{"1"H}$ = (0.5 ns/pF) C_L + 24 ns			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
$t_{"1"H}$ = (0.4 ns/pF) C_L + 20 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
3-State Propagation Delay, Output "0" to High Impedance**	9	$t_{"0"H}$																ns
$t_{"0"H}$ = (0.6 ns/pF) C_L + 32 ns			5.0	–	–	–	40	125	–	–	–	–	–	40	150	–	–	
$t_{"0"H}$ = (0.5 ns/pF) C_L + 24 ns			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
$t_{"0"H}$ = (0.4 ns/pF) C_L + 20 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
3-State Propagation Delay, High Impedance to "1" Level**	9	$t_{H"1"}$																ns
$t_{H"1"}$ = (0.4 ns/pF) C_L + 33 ns			5.0	–	–	–	40	125	–	–	–	–	–	40	150	–	–	
$t_{H"1"}$ = (0.26 ns/pF) C_L + 26 ns			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
$t_{H"1"}$ = (0.20 ns/pF) C_L + 22 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
3-State Propagation Delay, High Impedance to "1" Level**	9	$t_{H"0"}$																ns
$t_{H"0"}$ = (0.3 ns/pF) C_L + 35 ns			5.0	–	–	–	40	125	–	–	–	–	–	40	150	–	–	
$t_{H"0"}$ = (0.1 ns/pF) C_L + 28 ns			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
$t_{H"0"}$ = (0.09 ns/pF) C_L + 23 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

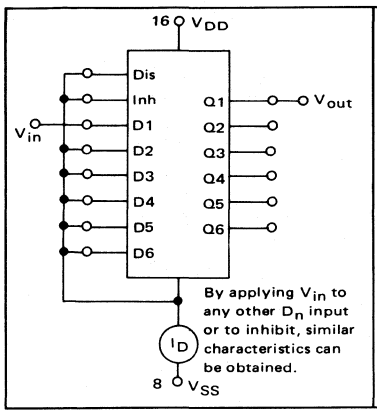


FIGURE 2 – TYPICAL OUTPUT SOURCE CURRENT TEST CIRCUIT (I_{OH})

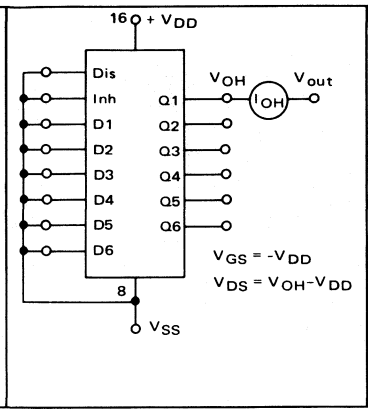


FIGURE 3 – TYPICAL OUTPUT SINK CURRENT TEST CIRCUIT (I_{OL})

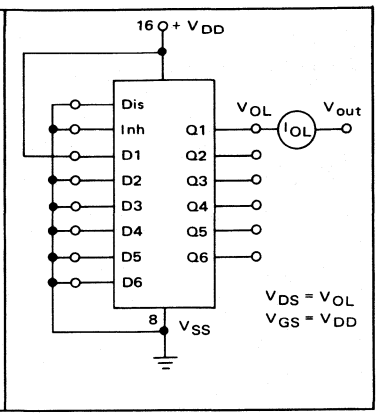


FIGURE 4 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

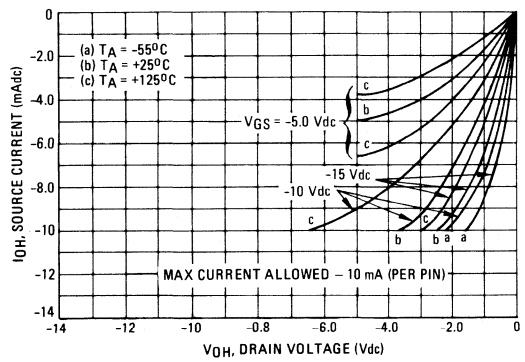


FIGURE 5 – TYPICAL OUTPUT SINK CHARACTERISTICS

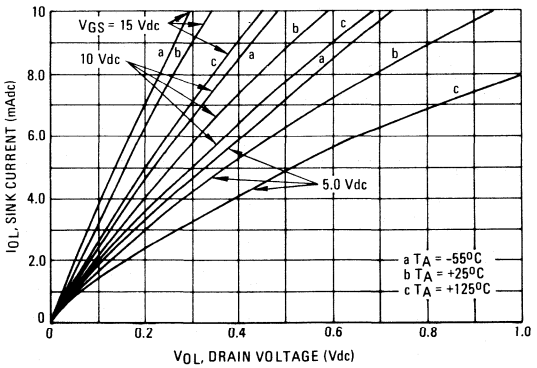


FIGURE 6 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

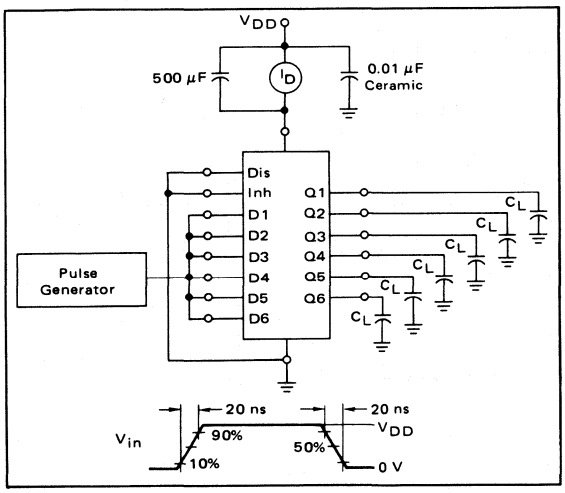


FIGURE 7 – POWER DISSIPATION CHARACTERISTICS

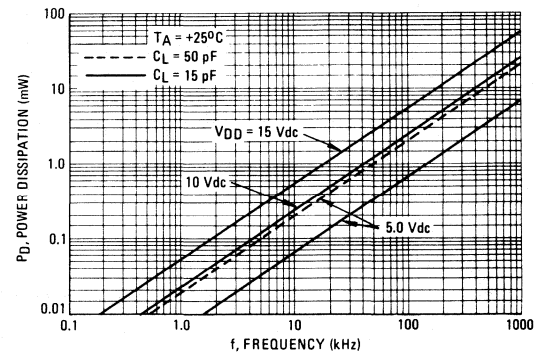


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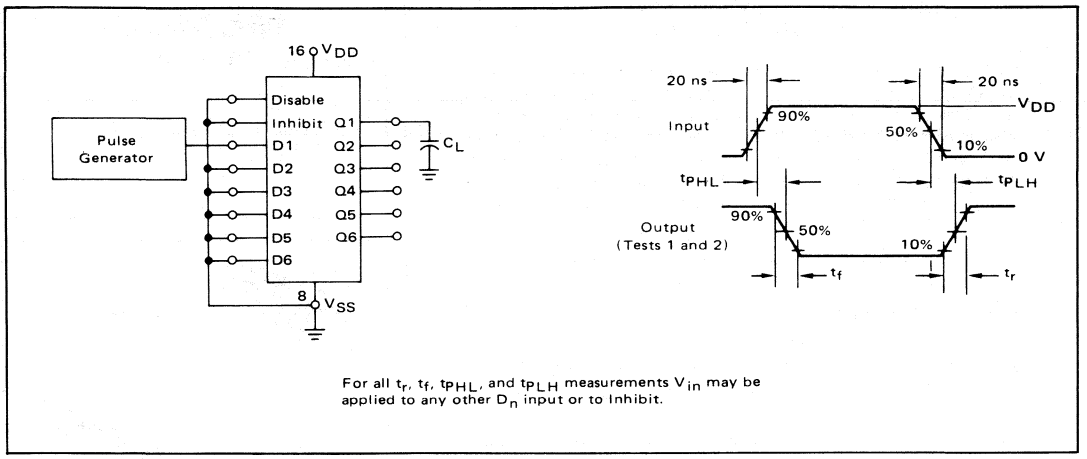
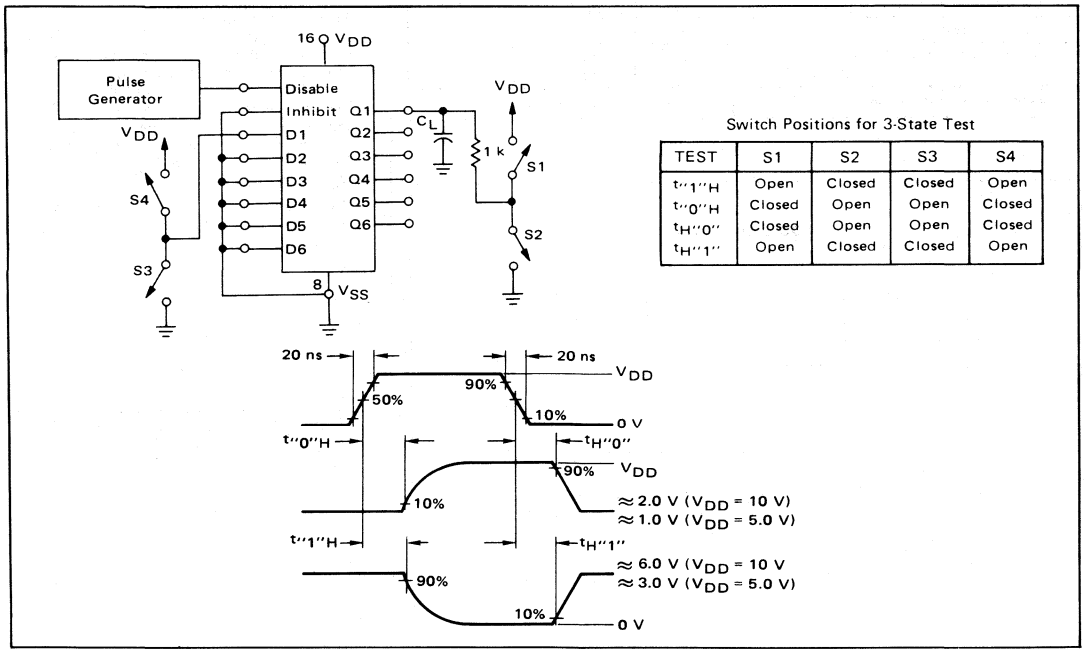
FIGURE 8 – AC TEST CIRCUIT AND WAVEFORMS
(t_r, t_f, t_{PHL}, and t_{PLH})



For all t_r, t_f, t_{PHL}, and t_{PLH} measurements V_{in} may be applied to any other D_n input or to Inhibit.

FIGURE 9 – 3-STATE AC TEST CIRCUIT AND WAVEFORMS
($t_{"1"H}$, $t_{H"1"}$, $t_{"0"H}$, and $t_{H"0"}$)



Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{"1"H}$	Open	Closed	Closed	Open
$t_{"0"H}$	Closed	Open	Open	Closed
$t_{H"0"}$	Closed	Open	Open	Closed
$t_{H"1"}$	Open	Closed	Closed	Open

7

MC14506AL
MC14506CL
MC14506CP

"AND-OR-INVERT" GATE

DUAL 2-WIDE, 2-INPUT EXPANDABLE AND-OR-INVERT GATE

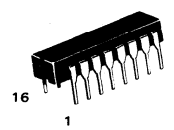
The MC14506 is an expandable AND-OR-INVERT gate with inhibit and 3-state output. The expand option allows cascading with any other gate, which may be carried as far as desired as long as the propagation delay added with each gate is considered. For example, the second AOI gate in this device may be used to expand the first gate, giving an expanded 4-wide, 2-input AOI gate. This device is useful in data control and digital multiplexing applications.

- Low Quiescent Power Dissipation = 0.1 μW/package typical
- 3-State Output
- Separate Inhibit Line
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14506AL)
  = 3.0 Vdc to 16 Vdc (MC14506CL/CP)

McMOS

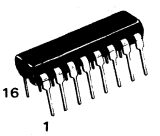
(LOW-POWER COMPLEMENTARY MOS)

DUAL EXPANDABLE AND-OR-INVERT GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



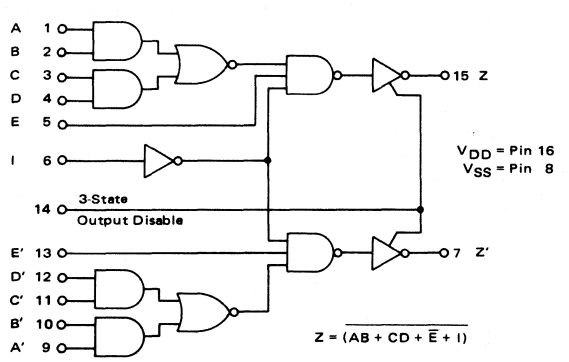
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14506AL — MC14506CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14506AL — MC14506CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

LOGIC DIAGRAM



TRUTH TABLE

A	B	C	D	E	INHIBIT	DISABLE	Z
0	0	0	0	1	0	0	1
0	X	0	X	1	0	0	1
0	X	X	0	1	0	0	1
X	0	0	X	1	0	0	1
X	0	X	0	1	0	0	1
1	1	X	X	X	X	0	0
X	X	1	1	X	X	0	0
X	X	X	X	0	X	0	0
X	X	X	X	X	1	0	0
X	X	X	X	X	X	1	High Impedance

X = Don't Care

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14506AL -55°C Min	MC14506AL -55°C Max	MC14506AL +25°C Min	MC14506AL +25°C Typ	MC14506AL +25°C Max	MC14506AL +125°C Min	MC14506AL +125°C Max	MC14506CL/CP -40°C Min	MC14506CL/CP -40°C Max	MC14506CL/CP +25°C Min	MC14506CL/CP +25°C Typ	MC14506CL/CP +25°C Max	MC14506CL/CP +85°C Min	MC14506CL/CP +85°C Max	Unit
Output Voltage "0" Level	1	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–																	
($V_{out} \geq 3.5$ Vdc) ($V_{out} \geq 7.0$ Vdc) ($V_{out} \geq 10.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc) ($V_{out} \leq 3.0$ Vdc) ($V_{out} \leq 4.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	2	I_{OH}	5.0	-0.62	–	-0.5	-2.0	–	-0.35	–	-0.23	–	-0.2	-2.0	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-5.0	–	–	–	–	–	–	-5.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	3	I_{OL}	5.0	0.5	–	0.4	1.0	–	0.28	–	0.23	–	0.2	1.0	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	3.0	–	0.65	–	0.6	–	0.5	3.0	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
3-State Output Leakage Current (C_L = 15 pF)	4	I_{TL}	5.0	–	±0.05	–	±0.0001	±0.05	–	±3.0	–	±0.5	–	±0.0001	±0.5	–	±7.0	μAdc
			10	–	±0.1	–	±0.0002	±0.1	–	±6.0	–	±1.0	–	±0.0002	±1.0	–	±14	
			15	–	–	–	±0.0005	–	–	–	–		–	±0.0005	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	5,6	P_D	5.0	–	2.5	–	0.05	2.5	–	150	–	25	–	0.05	25	–	750	μW
			10	–	10	–	0.1	10	–	600	–	100	–	0.1	100	–	3000	
Output Rise Time (C_L = 15 pF)**	7,8	t_r																ns
t_r = (2.3 ns/pF) C_L + 40 ns			5.0	–	–	–	75	140	–	–	–	–	–	75	200	–	–	
t_r = (1.0 ns/pF) C_L + 20 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (0.73 ns/pF) C_L + 15 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time (C_L = 15 pF)**	7,8	t_f																ns
t_f = (1.4 ns/pF) C_L + 54 ns			5.0	–	–	–	75	140	–	–	–	–	–	75	200	–	–	
t_f = (0.55 ns/pF) C_L + 27 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.33 ns/pF) C_L + 20 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Data Propagation Delay Time ** (C_L = 15 pF)	7																	
t_{PHL} = (1.1 ns/pF) C_L + 225 ns		t_{PHL}	5.0	–	–	–	240	360	–	–	–	–	–	240	480	–	–	ns
t_{PHL} = (0.41 ns/pF) C_L + 74 ns			10	–	–	–	80	135	–	–	–	–	–	80	175	–	–	
t_{PHL} = (0.26 ns/pF) C_L + 51 ns			15	–	–	–	55	–	–	–	–	–	–	55	–	–	–	
t_{PLH} = (1.0 ns/pF) C_L + 225 ns		t_{PLH}	5.0	–	–	–	240	360	–	–	–	–	–	240	480	–	–	ns
t_{PLH} = (0.53 ns/pF) C_L + 72 ns			10	–	–	–	80	135	–	–	–	–	–	80	175	–	–	
t_{PLH} = (0.36 ns/pF) C_L + 50 ns			15	–	–	–	55	–	–	–	–	–	–	55	–	–	–	
Expand Turn-On Delay Time (C_L = 15 pF)	8	t_{PHL}	5.0	–	–	–	170	270	–	–	–	–	–	170	330	–	–	ns
			10	–	–	–	65	90	–	–	–	–	–	65	110	–	–	
			15	–	–	–	45	–	–	–	–	–	–	45	–	–	–	
Expand Turn-Off Delay Time (C_L = 15 pF)	8	t_{PLH}	5.0	–	–	–	125	270	–	–	–	–	–	125	330	–	–	ns
			10	–	–	–	45	90	–	–	–	–	–	45	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Inhibit Turn-On Delay Time (C_L = 15 pF)	8	t_{PHL}	5.0	–	–	–	200	360	–	–	–	–	–	200	400	–	–	ns
			10	–	–	–	80	135	–	–	–	–	–	80	175	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Inhibit Turn-Off Delay Time (C_L = 15 pF)	8	t_{PLH}	5.0	–	–	–	165	360	–	–	–	–	–	165	400	–	–	ns
			10	–	–	–	70	135	–	–	–	–	–	70	175	–	–	
			15	–	–	–	45	–	–	–	–	–	–	45	–	–	–	
3-State Propagation Delay "1" to High Impedance (C_L = 15 pF)	8	$t_{"1"H}$	5.0	–	–	–	46	125	–	–	–	–	–	46	150	–	–	ns
			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
			15	–	–	–	23	–	–	–	–	–	–	23	–	–	–	
3-State Propagation Delay "0" to High Impedance (C_L = 15 pF)	8	$t_{"0"H}$	5.0	–	–	–	77	125	–	–	–	–	–	77	150	–	–	ns
			10	–	–	–	39	75	–	–	–	–	–	39	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
3-State Propagation Delay High Impedance to "1" (C_L = 15 pF)	8	$t_{H"1"}$	5.0	–	–	–	93	250	–	–	–	–	–	93	300	–	–	ns
			10	–	–	–	36	100	–	–	–	–	–	36	120	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
3-State Propagation Delay High Impedance to "0" (C_L = 15 pF)	8	$t_{H"0"}$	5.0	–	–	–	158	250	–	–	–	–	–	158	300	–	–	ns
			10	–	–	–	55	100	–	–	–	–	–	55	120	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level, before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS

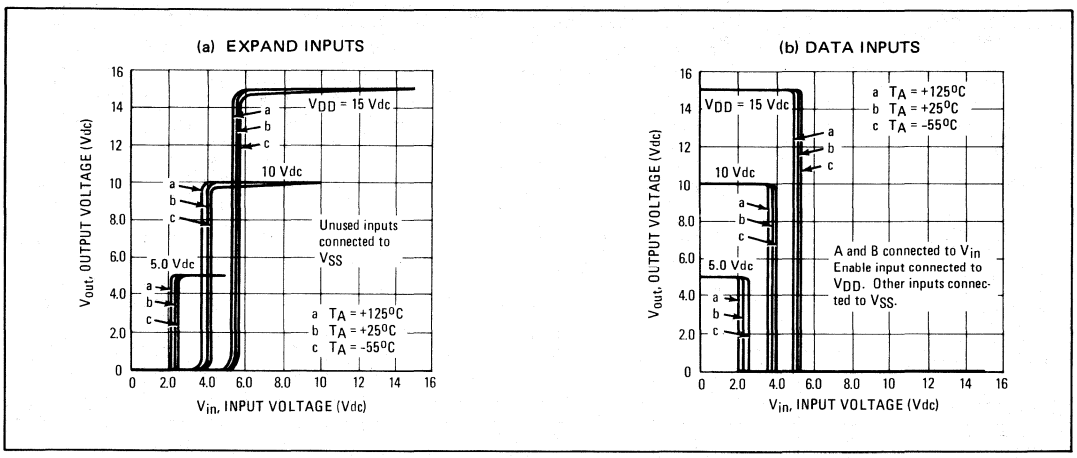


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

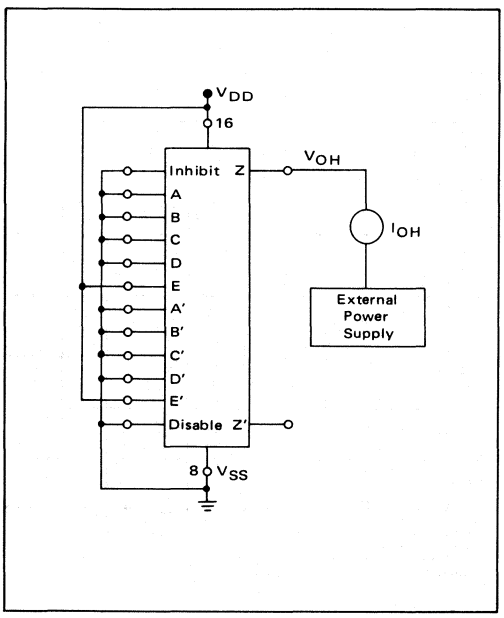


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

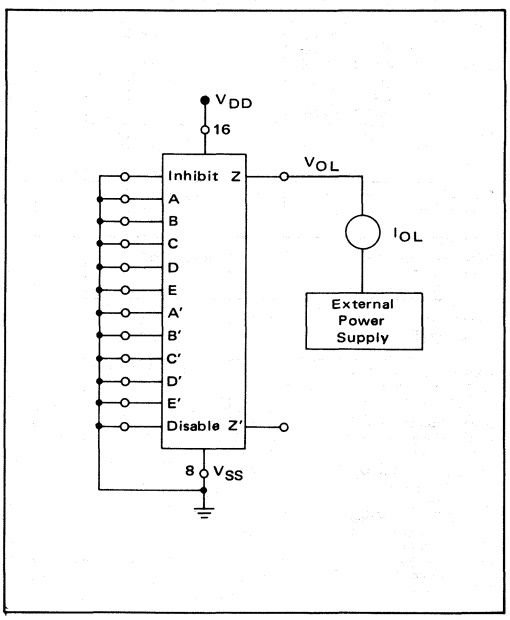


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FIGURE 4 – 3-STATE LEAKAGE CURRENT TEST CIRCUIT

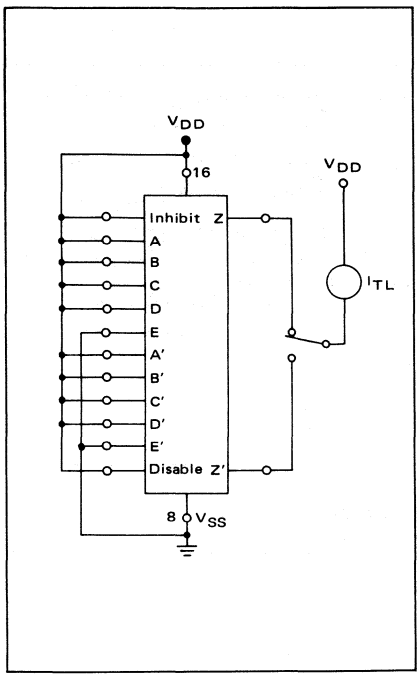


FIGURE 5 – TYPICAL POWER DISSIPATION TEST CIRCUIT

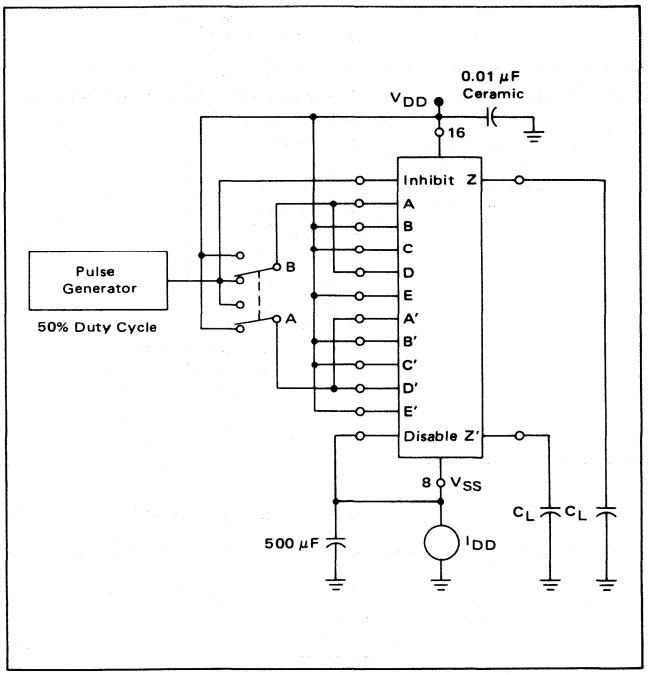


FIGURE 6 – TYPICAL POWER DISSIPATION CHARACTERISTICS

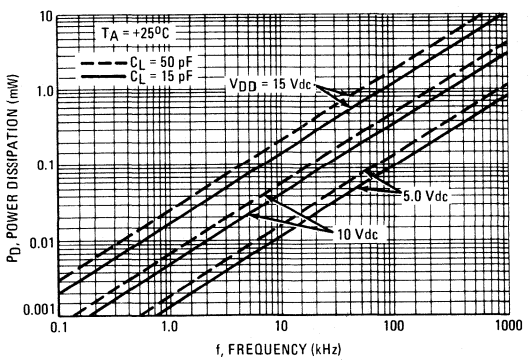


FIGURE 7 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(Data Inputs)

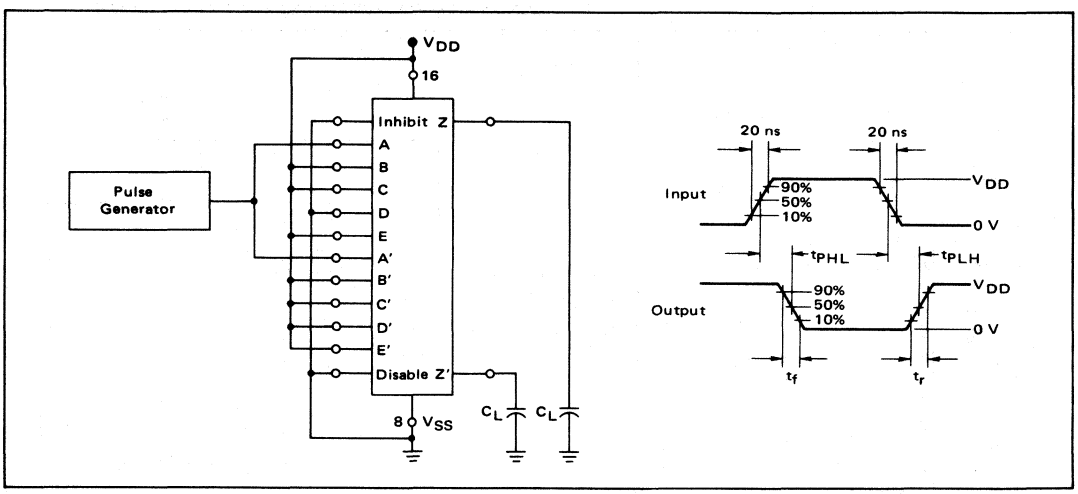
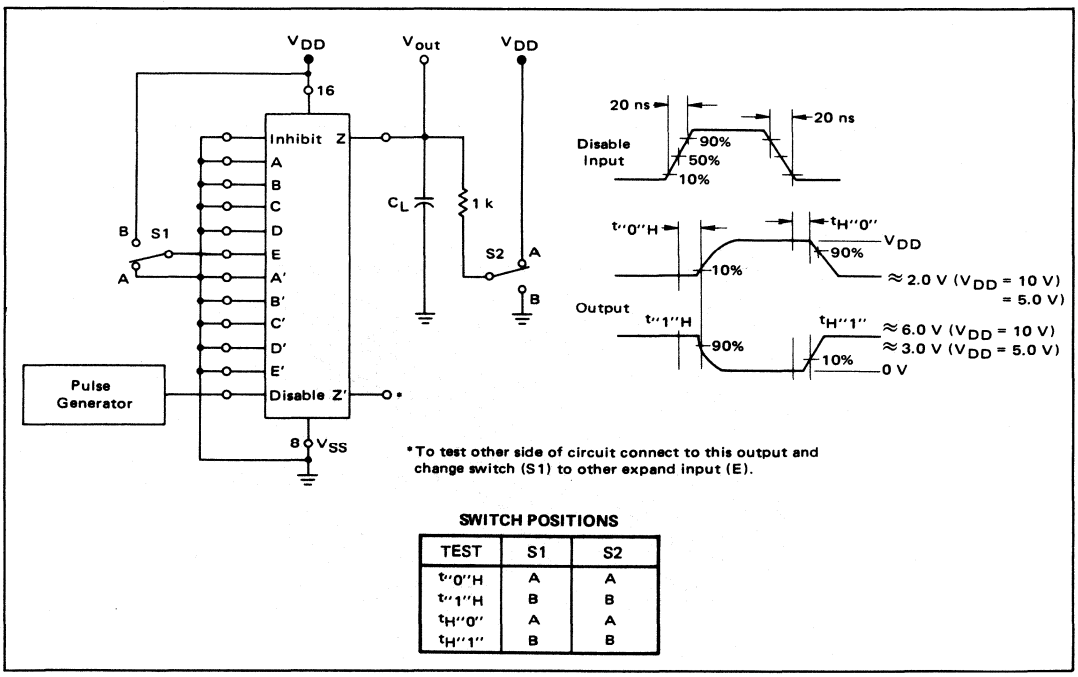


FIGURE 8 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
(For 3-State Output)



*To test other side of circuit connect to this output and change switch (S1) to other expand input (E).

SWITCH POSITIONS

TEST	S1	S2
t_{PHZ}	A	A
t_{PLZ}	B	B
t_{PZH}	A	A
t_{PZL}	B	B

7

MC14507AL
MC14507CL

(4030 TYPE)

EXCLUSIVE "OR" GATE

QUAD EXCLUSIVE "OR" GATE

The MC14507AL/CL quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14507AL)
  3.0 Vdc to 16 Vdc (MC14507CL)
- Single Supply Operation – Positive or Negative
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance – 500 ohms typical
- Pin-For-Pin Compatible with 4030 Type

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14507AL MC14507CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I_{DD}	10	mAdc
Operating Temperature Range	– MC14507AL – MC14507CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

McMOS

LOW-POWER COMPLEMENTARY MOS QUAD EXCLUSIVE "OR" GATE

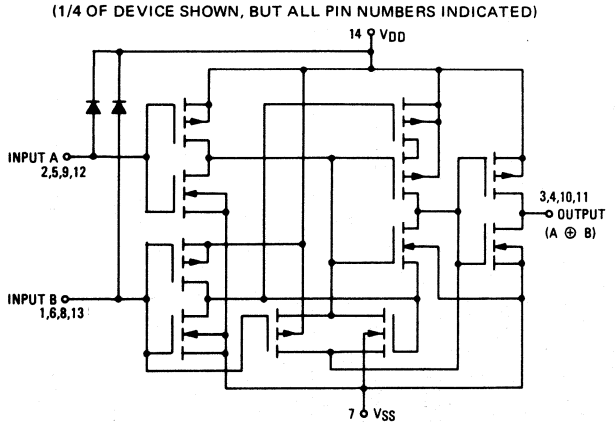
L SUFFIX
CERAMIC PACKAGE
CASE 632

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

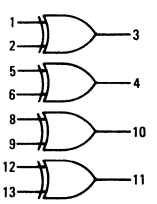
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

CIRCUIT SCHEMATIC

(1/4 OF DEVICE SHOWN, BUT ALL PIN NUMBERS INDICATED)



LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	MC14507AL							MC14507CL							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage		1,2,3,4,5																Vdc
(V_{DD} = 5.0 Vdc)	"0" Level		V_{OL}	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{DD} = 10 Vdc)				–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
(V_{DD} = 5.0 Vdc)	"1" Level		V_{OH}	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
(V_{DD} = 10 Vdc)				9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*		–																Vdc
($V_{out} \geq$ 3.5 Vdc, V_{DD} = 5.0 Vdc)			V_{NL}	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq$ 7.0 Vdc, V_{DD} = 10 Vdc)				3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \leq$ 1.5 Vdc, V_{DD} = 5.0 Vdc)			V_{NH}	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq$ 3.0 Vdc, V_{DD} = 10 Vdc)				2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
Output Drive Current			I_{OD}															mAdc
(V_{out} = 2.5 Vdc, V_{DS} = 5.0 Vdc)	P Channel	6		-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	
(V_{out} = 9.5 Vdc, V_{DS} = 10 Vdc)				-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{out} = 0.4 Vdc, V_{DS} = 5.0 Vdc)	N Channel	7		0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{out} = 0.5 Vdc, V_{DS} = 10 Vdc)				1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
Input Current		–	I_{in}	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		–	C_{in}	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation		8,9,10	P_D															μW
(V_{DD} = 5.0 Vdc)				–	0.25	–	0.005	0.25	–	15	–	0.25	–	0.025	2.5	–	75	
(V_{DD} = 10 Vdc)				–	1.0	–	0.01	1.0	–	60	–	10	–	0.05	10	–	300	
Output Rise Time		11,12	t_r															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	100	175	–	–	–	–	–	100	200	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Output Fall Time		11,13	t_f															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	100	175	–	–	–	–	–	100	200	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Turn-On Delay Time		11,14	t_{PHL}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	75	125	–	–	–	–	–	75	175	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	60	–	–	–	–	–	35	75	–	–	
Turn-Off Delay Time		11,15	t_{PLH}															ns
(C_L = 15 pF, V_{DD} = 5.0 Vdc)				–	–	–	75	125	–	–	–	–	–	75	175	–	–	
(C_L = 15 pF, V_{DD} = 10 Vdc)				–	–	–	35	60	–	–	–	–	–	35	75	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

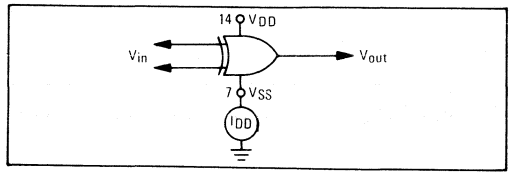


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

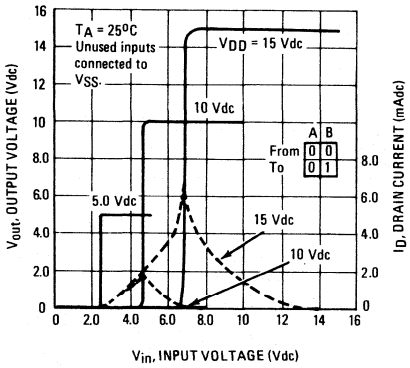


FIGURE 3 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

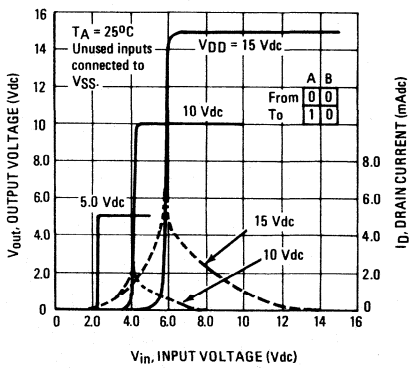


FIGURE 4 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

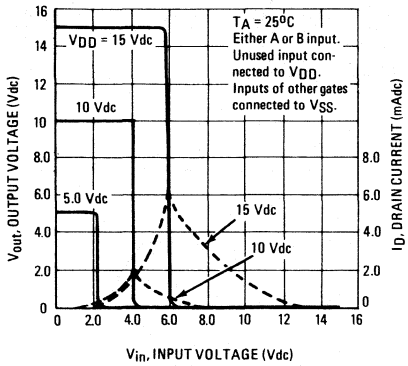


FIGURE 5 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

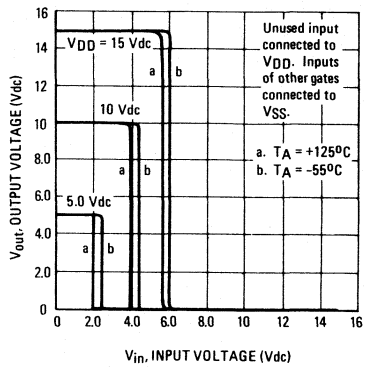


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FIGURE 6 – TYPICAL P-CHANNEL DRAIN CHARACTERISTICS

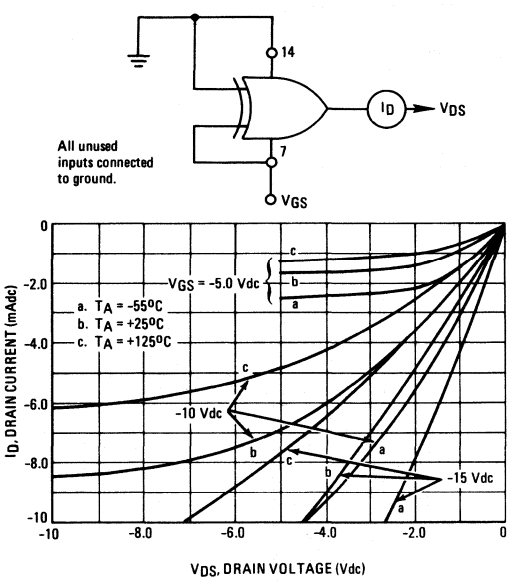


FIGURE 7 – TYPICAL N-CHANNEL DRAIN CHARACTERISTICS

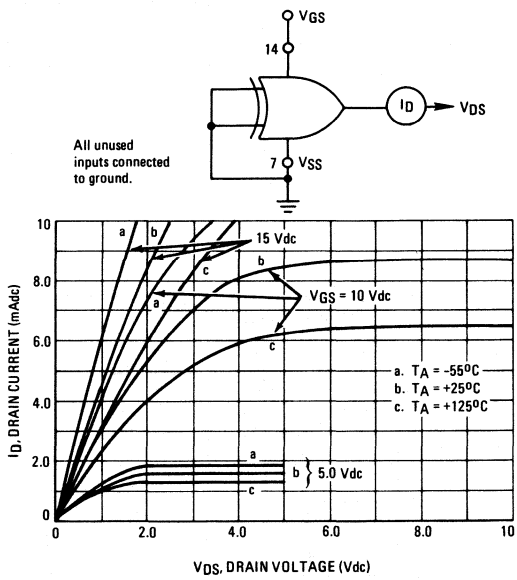


FIGURE 8 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

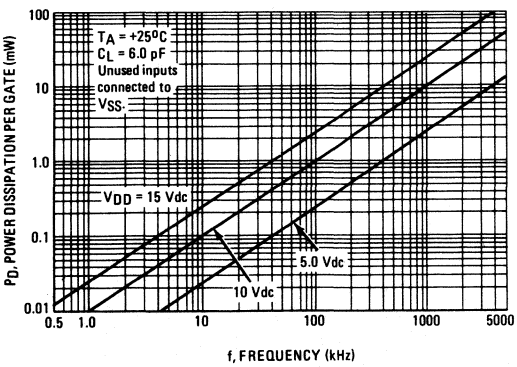


FIGURE 9 – TYPICAL GATE POWER DISSIPATION CHARACTERISTICS

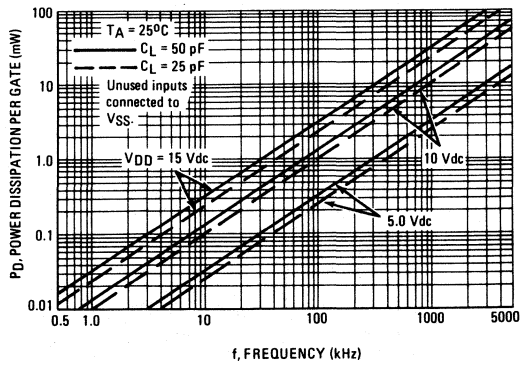


FIGURE 10 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

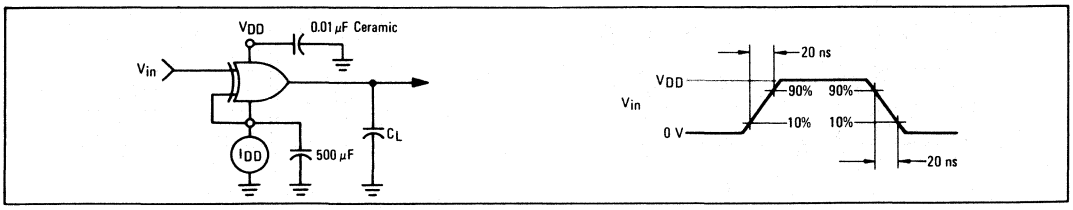


FIGURE 11 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

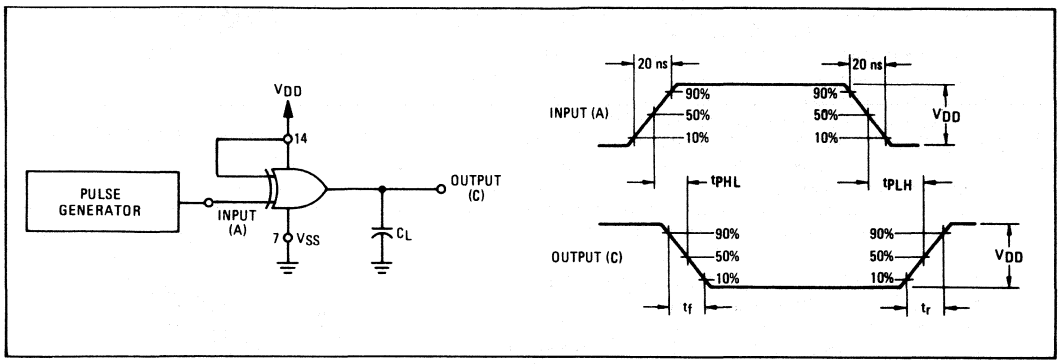


FIGURE 12 – TYPICAL RISE TIME versus LOAD CAPACITANCE

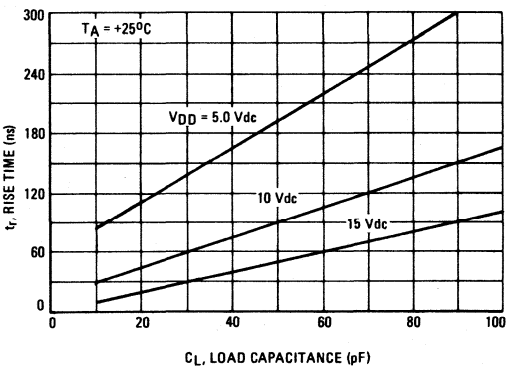


FIGURE 13 – TYPICAL FALL TIME versus LOAD CAPACITANCE

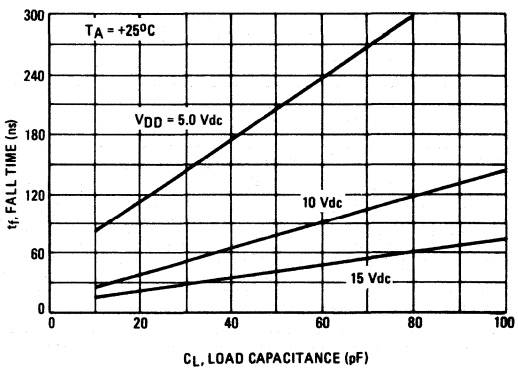


FIGURE 14 – TYPICAL TURN-ON-DELAY CHARACTERISTICS

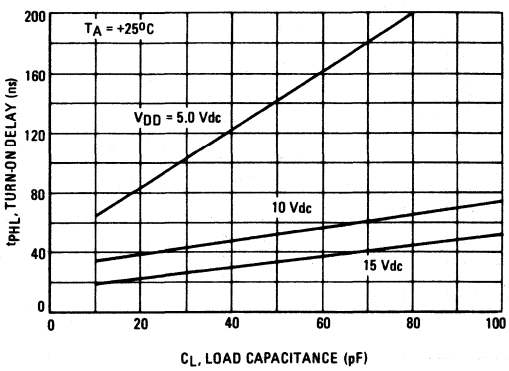
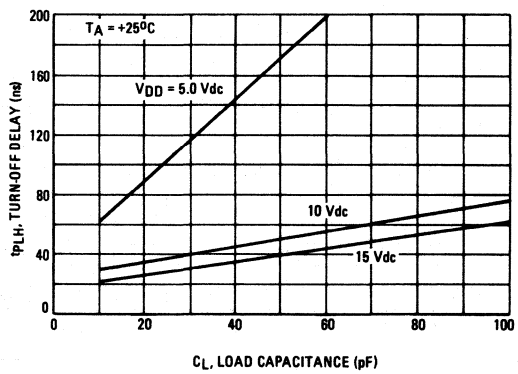


FIGURE 15 – TYPICAL TURN-OFF DELAY CHARACTERISTICS



MC14508AL
MC14508CL

Advance Information

DUAL 4-BIT LATCH

The MC14508AL/CL dual 4-bit latch is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The part consists of two identical, independent 4-bit latches with separate Strobe (ST) and Master Reset (MR) controls. Separate Disable inputs force the outputs to a high impedance state and allow the devices to be used in time sharing bus line applications.

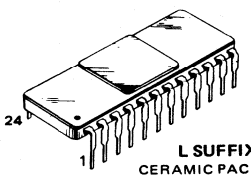
These complementary MOS latches find primary use in buffer storage, holding register, or general digital logic functions where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 0.5 μW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection of All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14508AL)
  = 3.0 Vdc to 16 Vdc (MC14508CL)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 7.0 pF typical
- Logic Swing Independent of Fanout
- 3-State Output

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-BIT LATCH



L SUFFIX
CERAMIC PACKAGE
CASE 684

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 12)

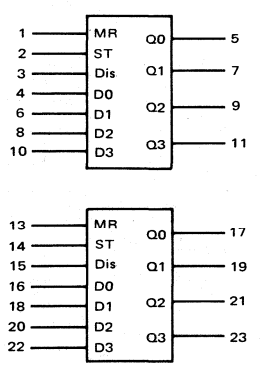
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14508AL MC14508CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14508AL – MC14508CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

MR	ST	DISABLE	D3	D2	D1	D0	Q3	Q2	Q1	Q0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	1
0	1	0	0	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	1	1
0	1	0	0	1	0	0	0	1	0	0
0	1	0	0	1	0	1	0	1	0	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	0	1	1	1	0	1	1	1
0	1	0	1	0	0	0	1	0	0	0
0	1	0	1	0	0	1	1	0	0	1
0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	1	1	0	1	1
0	1	0	1	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1	1	0	1
0	1	0	1	1	1	0	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1
0	0	0	X	X	X	X	LATCHED			
1	X	0	X	X	X	X	0	0	0	0
X	X	1	X	X	X	X	HIGH IMPEDANCE			

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12

This is advance information on a new introduction and specifications are subject to change without notice.
See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14508AL -55°C Min	MC14508AL -55°C Max	MC14508AL +25°C Min	MC14508AL +25°C Typ	MC14508AL +25°C Max	MC14508AL +125°C Min	MC14508AL +125°C Max	MC14508CL -40°C Min	MC14508CL -40°C Max	MC14508CL +25°C Min	MC14508CL +25°C Typ	MC14508CL +25°C Max	MC14508CL +85°C Min	MC14508CL +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	2	I_{OH}	5.0	-0.62	–	-0.50	-2.0	–	-0.35	–	-0.23	–	-0.20	-2.0	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.0	–	-0.35	–	-0.23	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	3	I_{OL}	5.0	0.50	–	0.40	0.6	–	0.28	–	0.23	–	0.20	0.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	1.1	–	0.65	–	0.60	–	0.50	1.1	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	7.0	–	–	–	–	–	–	7.0	–	–	–	pF
Quiescent Dissipation **†	1	P_Q																mW
(C_L = 15 pF, f = 0)			5.0	–	0.025	–	0.0005	0.025	–	1.5	–	0.25	–	0.5	0.25	–	3.5	
			10	–	0.10	–	0.001	0.10	–	6.0	–	1.0	–	1.0	1.0	–	14	
			15	–	–	–	0.0023	–	–	–	–	–	–	2.3	–	–	–	
Total Power Dissipation (Dynamic plus Quiescent) (C_L = 15 pF)	1	P_D																mW
			5.0				P_D = (10 mW/MHz) f + 0.0005 mW											
			10				P_D = (40 mW/MHz) f + 0.001 mW											
			15				P_D = (92 mW/MHz) f + 0.0023 mW											
Output Rise Time** (C_L = 15 pF)	4	t_r																ns
t_r = (2.3 ns/pF) C_L + 75 ns			5.0	–	–	–	110	250	–	–	–	–	–	110	300	–	–	
t_r = (1.1 ns/pF) C_L + 34 ns			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
t_r = (0.75 ns/pF) C_L + 24 ns			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Output Fall Time** (C_L = 15 pF)	4	t_f																ns
t_f = (2.0 ns/pF) C_L + 70 ns			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
t_f = (1.0 ns/pF) C_L + 35 ns			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
t_f = (0.7 ns/pF) C_L + 30 ns			15	–	–	–	40	–	–	–	–	–	–	35	–	–	–	
Turn-On Delay Time (C_L = 15 pF)	4	t_{PHL}																ns
t_{PHL} = (0.8 ns/pF) C_L +118 ns			5.0	–	–	–	130	350	–	–	–	–	–	130	400	–	–	
t_{PHL} = (0.5 ns/pF) C_L + 47 ns			10	–	–	–	55	175	–	–	–	–	–	55	200	–	–	
t_{PHL} = (0.3 ns/pF) C_L + 40 ns			15	–	–	–	45	–	–	–	–	–	–	45	–	–	–	
Turn-Off Delay Time (C_L = 15 pF)	4	t_{PLH}																ns
t_{PLH} = (0.75 ns/pF) C_L + 129 ns			5.0	–	–	–	140	350	–	–	–	–	–	140	400	–	–	
t_{PLH} = (0.5 ns/pF) C_L + 57 ns			10	–	–	–	65	175	–	–	–	–	–	65	200	–	–	
t_{PLH} = (0.25 ns/pF) C_L + 46 ns			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Minimum Master Reset Pulse Width (C_L = 15 pF)	4	PW_{MR}																ns
			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Minimum Strobe Pulse Width (C_L = 15 pF)	4	PW_{ST}																ns
			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Data Hold Time# (C_L = 15 pF)	4	t_{hold}																ns
			5.0	–	–	–	0	30	–	–	–	–	–	0	30	–	–	
			10	–	–	–	0	10	–	–	–	–	–	0	10	–	–	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

Data hold time decreases as strobe width increases.

† For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 4 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$

Where: P_T in mW (Per Gate), C_L in pF, V_{DD} in Vdc, and f in MHz.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14508AL							MC14508CL							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
3-State Output Leakage Current	5	I_{TL}	5.0	±0.05	–	–	±0.001	±0.05	–	±3.0	±0.50	–	–	±0.001	±0.50	–	±7.0	μA
			10	±0.10	–	–	±0.002	±0.10	–	±6.0	±1.0	–	–	±0.002	±1.0	–	±14	
			15	–	–	–	±0.005	–	–	–	–	–	–	±0.005	–	–	–	
3-State Propagation Delay (Output "1" to High Impedance) (C_L = 15 pF)	6	$t_{"1"H}$	5.0	–	–	–	60	125	–	–	–	–	–	60	150	–	–	ns
			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
3-State Propagation Delay (Output "0" to High Impedance) (C_L = 15 pF)	6	$t_{"0"H}$	5.0	–	–	–	60	125	–	–	–	–	–	60	150	–	–	ns
			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
3-State Propagation Delay (High Impedance to "1" Level) (C_L = 15 pF)	6	$t_{H"1"}$	5.0	–	–	–	60	125	–	–	–	–	–	60	150	–	–	ns
			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
3-State Propagation Delay (High Impedance to "0" Level) (C_L = 15 pF)	6	$t_{H"0"}$	5.0	–	–	–	60	125	–	–	–	–	–	60	150	–	–	ns
			10	–	–	–	30	75	–	–	–	–	–	30	100	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

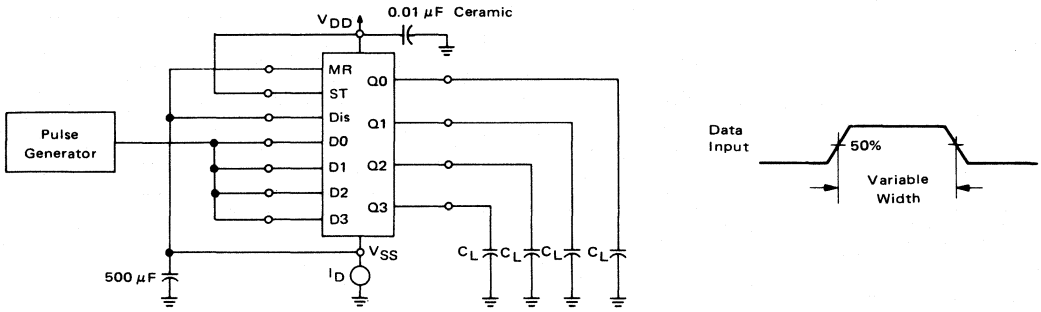


FIGURE 2 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

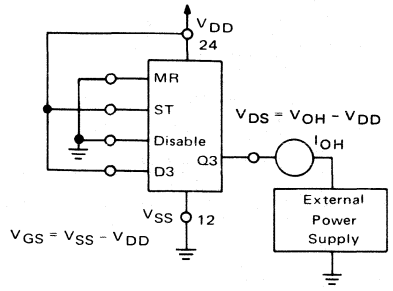
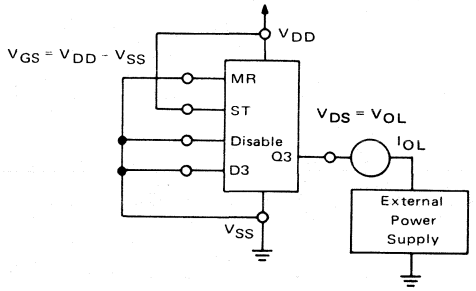
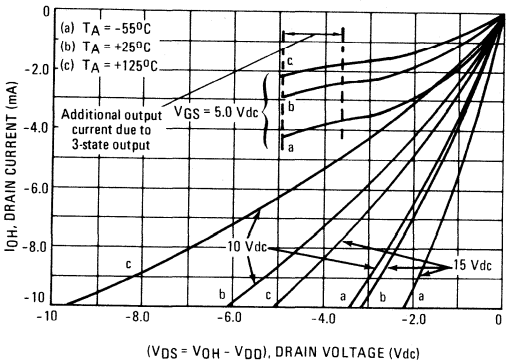


FIGURE 3 – TYPICAL OUTPUT SINK CHARACTERISTICS





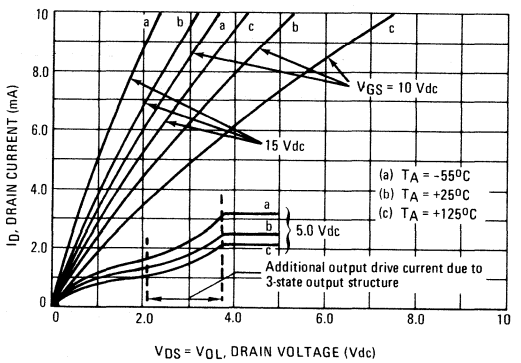
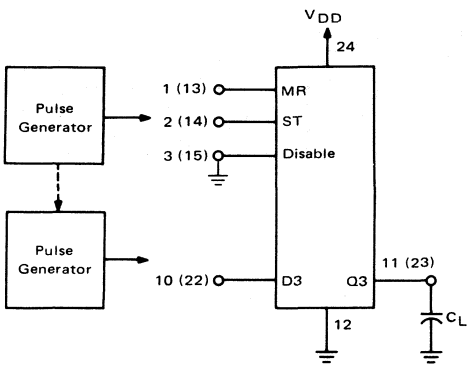
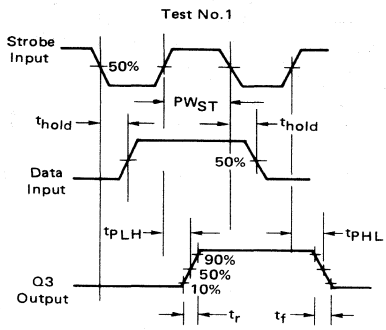


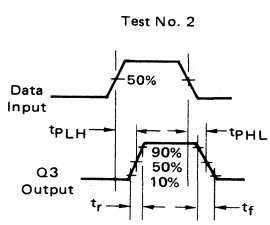
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

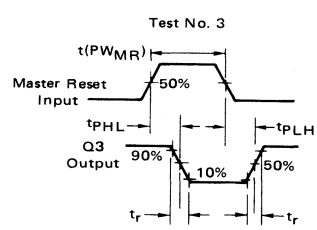




TEST CONNECTIONS

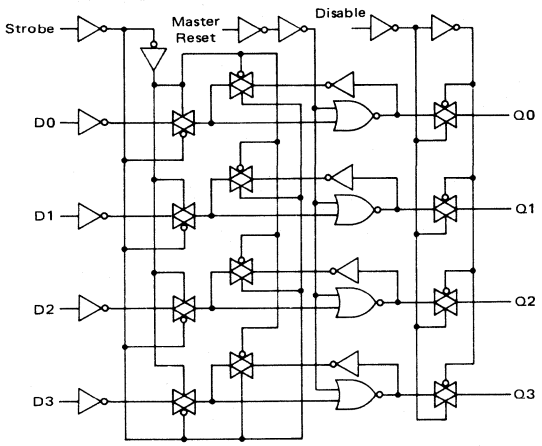
Parameter	Test No.	MR	ST	D3	Output
t_{hold}	1	Gnd	P.G.1	P.G.2	Q3
PW_{ST}	1	Gnd	P.G.1	P.G.2	Q3
PW_{MR}	3	P.G.1	V_{DD}	V_{DD}	Q3
t_{PLH} and t_{PHL}	1 or 2	Gnd	P.G.1	P.G.2	Q3
		Gnd	V_{DD}	P.G.1	Q3
t_r and t_f	3	P.G.1	V_{DD}	V_{DD}	Q3





7

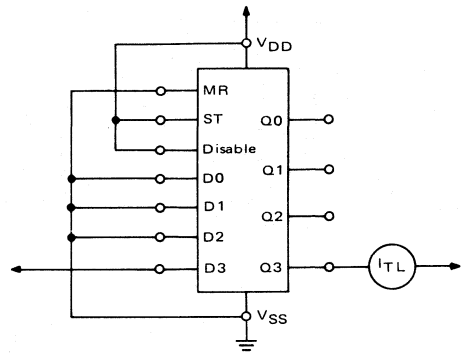
LOGIC DIAGRAM



Transmission Gate

A	CHARACTERISTICS
0	Bidirectional Open Circuit
1	Bidirectional Short Circuit

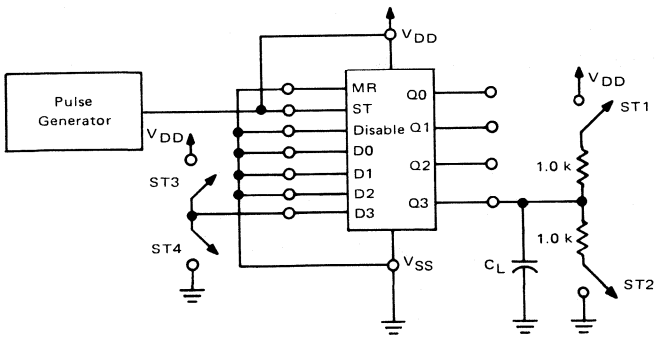
FIGURE 5 – 3-STATE LEAKAGE TEST



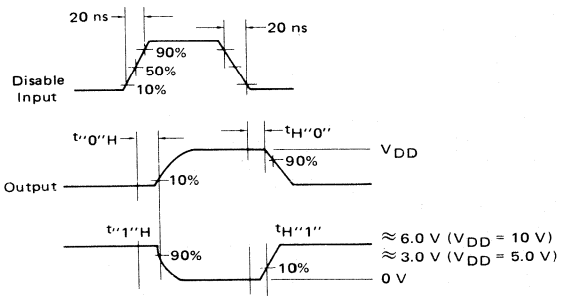
Test No. 1 measures $-I_{TL}$
D3 = 10 V, Q3 = 0 V

Test No. 2 measures $+I_{TL}$
D3 = 0 V, Q3 = $+V_{DD}$

FIGURE 6 – 3-STATE AC TEST CIRCUIT



TEST	ST1	ST2	ST3	ST4
$t_{"1"H}$	OPEN	CLOSE	CLOSE	OPEN
$t_{"0"H}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"0"}$	CLOSE	OPEN	OPEN	CLOSE
$t_{H"1"}$	OPEN	CLOSE	CLOSE	OPEN

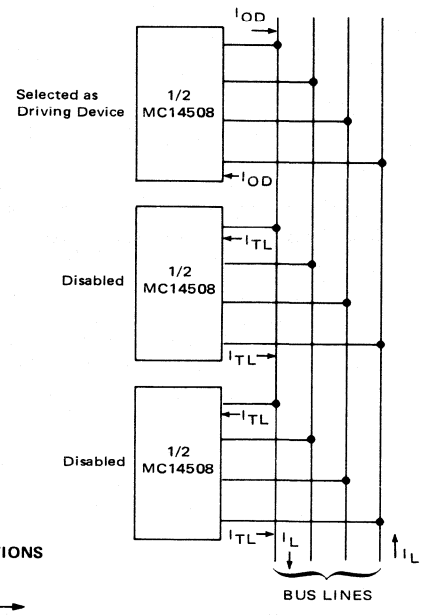


3-STATE MODE OF OPERATION

The MC14508AL/CL can be used in bussed systems as shown. The output terminals of N 4-bit latches can be directly wired to a bus line, and to one of the 4-bit latches selected. The selected latch controls the logic state of the bus line, and the remaining (N-1) 4-bit latches are disabled into a high impedance "off" state. The number of latches, N, which may be connected to a bus line is determined from the output drive current, I_{OD}, the 3-state or disabled output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs) and can be calculated by the following:

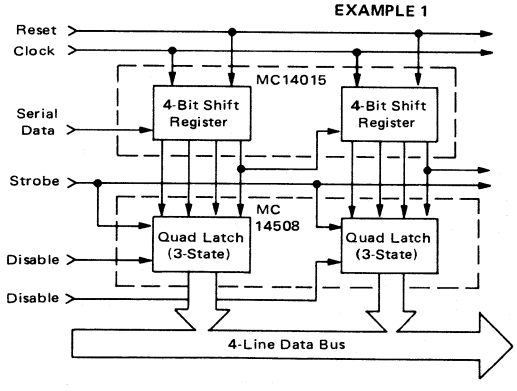
$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.

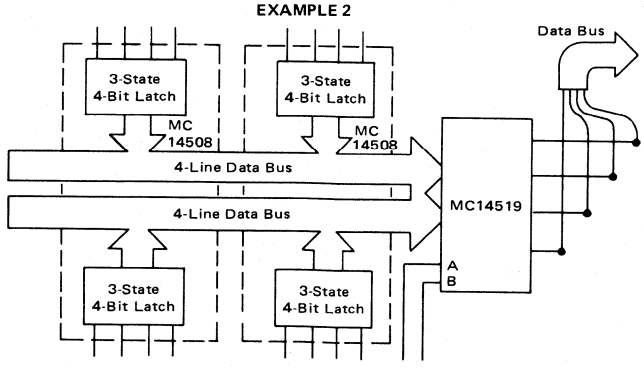


TYPICAL 3–STATE APPLICATIONS

EXAMPLE 1



EXAMPLE 2



7

MC14510AL
MC14510CL
MC14510CP

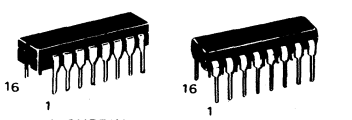
BCD UP/DOWN COUNTER

The MC14510 BCD up/down counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip-flop stages with a gating structure to provide type T flip-flop capability. The counter can be cleared by applying a high level on the Reset line. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14510AL)
  = 3.0 Vdc to 16 Vdc (MC14510CL/CP)
- Low Input Capacitance — 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design — Count Occurs on Positive Going Edge of Clock
- 6.0-MHz Counting Rate

McMOS
(LOW-POWER COMPLEMENTARY MOS)

BCD UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

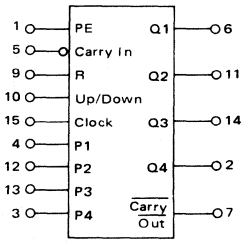
Rating	Symbol	Value	Unit
DC Supply Voltage — MC14510AL — MC14510CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14510AL — MC14510CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14510AL -55°C Min	MC14510AL -55°C Max	MC14510AL +25°C Min	MC14510AL +25°C Typ	MC14510AL +25°C Max	MC14510AL +125°C Min	MC14510AL +125°C Max	MC14510CL/CP -40°C Min	MC14510CL/CP -40°C Max	MC14510CL/CP +25°C Min	MC14510CL/CP +25°C Typ	MC14510CL/CP +25°C Max	MC14510CL/CP +85°C Min	MC14510CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	0.16		
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
		I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	–	P_Q																mW
(C_L = 15 pF, f = 0 MHz)			5.0	–	0.025	–	0.00025	0.025	–	1.5	–	0.25	–	0.00025	0.25	–	3.5	
			10	–	0.10	–	0.001	0.10	–	6.0	–	1.0	–	0.001	1.0	–	14	
			15	–	–	–	0.004	–	–	–	–	–	–	0.004	–	–	–	
Dynamic Power Dissipation	–	P_D																mW
(C_L = 15 pF)			5.0	P_D = (2.0 mW/MHz) f + 0.00025 mW														
			10	P_D = (8.0 mW/MHz) f + 0.001 mW														
			15	P_D = (18 mW/MHz) f + 0.004 mW														
Output Rise Time†	–	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 55 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r = (1.5 ns/pF) C_L + 17 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time†		t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 77 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock to Q Propagation Delay Time†	2	t_{PLH},																ns
(C_L = 15 pF)		t_{PLH}																
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 224 ns			5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 89 ns			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 67 ns			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Clock to Carry Out Propagation Delay Time†	2	t_{PHL},																ns
(C_L = 15 pF)		t_{PLH}																
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 274 ns			5.0	–	–	–	300	750	–	–	–	–	–	300	1200	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 114 ns			10	–	–	–	125	250	–	–	–	–	–	125	400	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 92 ns			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

†The formula given is for the typical characteristics only.

$$P_T(C_L) = P_D + 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14510AL							MC14510CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Carry In to Carry Out Propagation Delay Time† (C_L = 15 pF)	2	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 99 ns			5.0	–	–	–	125	250	–	–	–	–	–	125	500	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 39 ns			10	–	–	–	50	100	–	–	–	–	–	50	200	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 32 ns			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	2	PW_C																ns
			5.0	–	–	–	200	340	–	–	–	–	–	200	500	–	–	
			10	–	–	–	100	170	–	–	–	–	–	100	200	–	–	
			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)	2	PRF																MHz
			5.0	–	–	–	1.5	2.5	–	–	–	–	1.0	2.5	–	–	–	
			10	–	–	–	3.0	6.0	–	–	–	–	2.5	6.0	–	–	–	
Preset or Reset to Q_{out} Propagation Delay Time† (C_L = 15 pF)	2	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 299 ns			5.0	–	–	–	325	650	–	–	–	–	–	325	1000	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 104 ns			10	–	–	–	115	225	–	–	–	–	–	115	300	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 82 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Preset or Reset to Carry Out Propagation Delay Time† (C_L = 15 pF)	2	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 474 ns			5.0	–	–	–	500	850	–	–	–	–	–	500	1700	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 189 ns			10	–	–	–	200	300	–	–	–	–	–	200	600	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 142 ns			15	–	–	–	150	–	–	–	–	–	–	150	–	–	–	
Preset or Reset Removal Time** (C_L = 15 pF)	2	t_{rem}																ns
			5.0	–	–	–	325	650	–	–	–	–	–	325	1000	–	–	
			10	–	–	–	115	225	–	–	–	–	–	115	300	–	–	
			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Maximum Clock Rise and Fall Time (C_L = 15 pF)	2	t_r, t_f																µs
			5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
Carry In Setup Time (C_L = 15 pF)	2	t_{setup}																ns
			5.0	–	–	–	130	300	–	–	–	–	–	130	600	–	–	
			10	–	–	–	60	125	–	–	–	–	–	60	250	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Up/Down Setup Time (C_L = 15 pF)		t_{setup}																ns
			5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	
			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Minimum Preset Enable Pulse Width (C_L = 15 pF)	–	PW_{PE}																ns
			5.0	–	–	–	100	325	–	–	–	–	–	100	500	–	–	
			10	–	–	–	50	100	–	–	–	–	–	50	125	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

**The Preset or Reset signal must be low prior to a positive-going transition of the clock.

†The formula given is for the typical characteristics only.

$$P_T(C_L) = P_D + 10^{-3}(C_L - 15\text{ pF})V_{DD}{}^2 f$$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

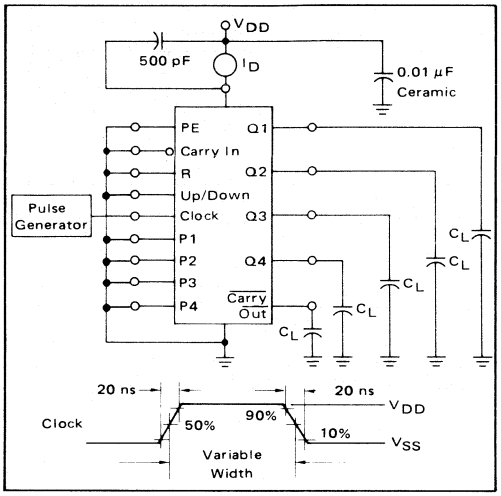
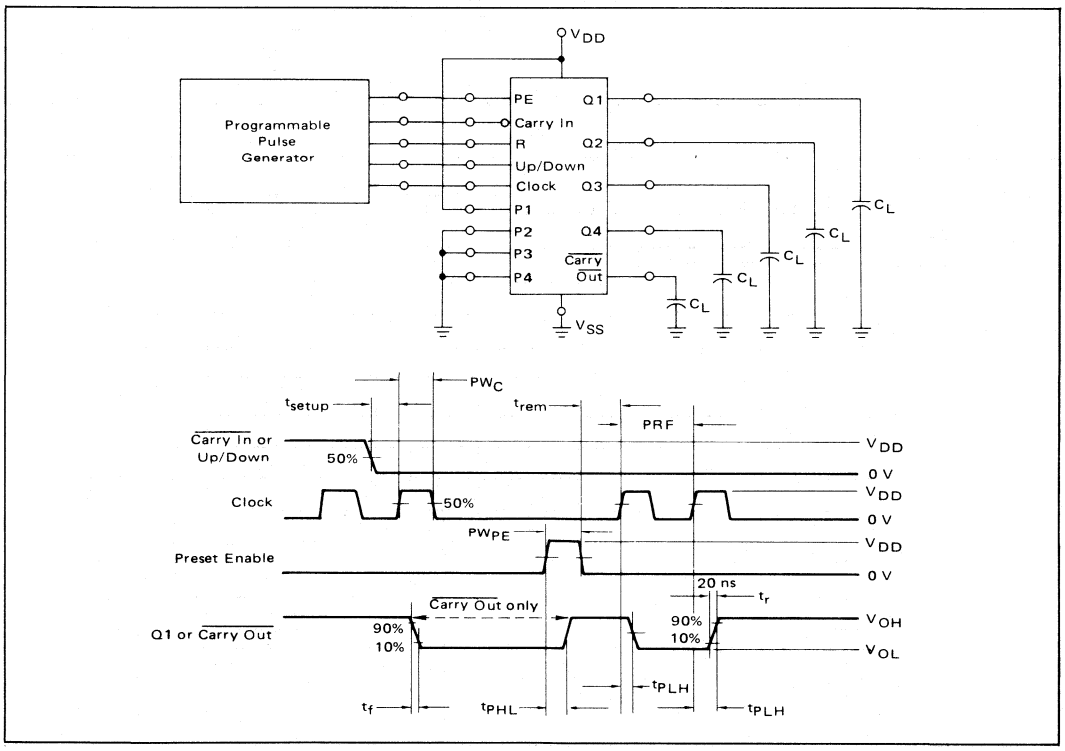
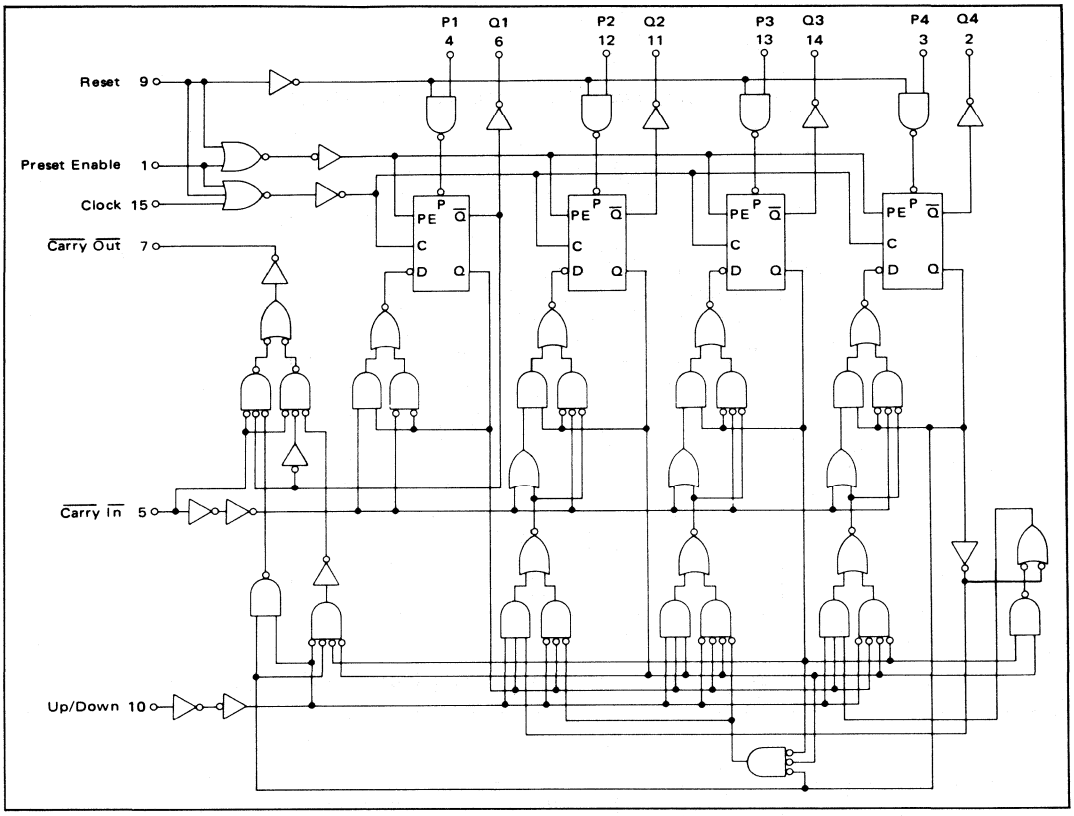


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

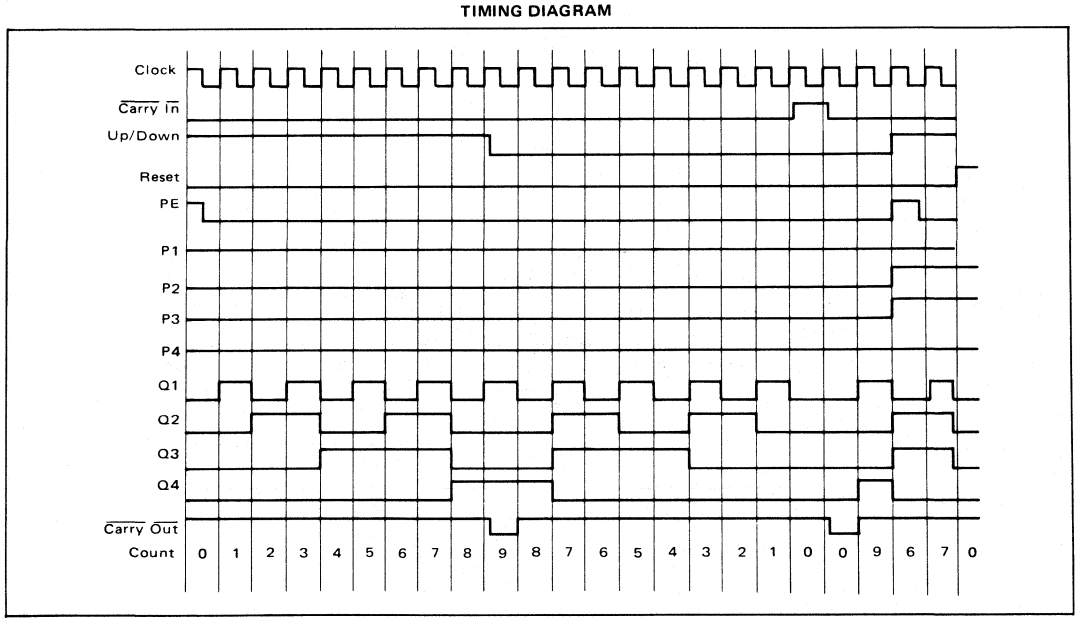


7

LOGIC DIAGRAM



TIMING DIAGRAM



7

MC14511AL
MC14511CL
MC14511CP

LATCH/DECODER/DRIVER

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

The MC14511 BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

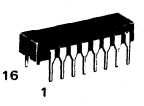
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility

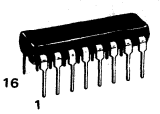
McMOS

(LOW-POWER COMPLEMENTARY MOS)

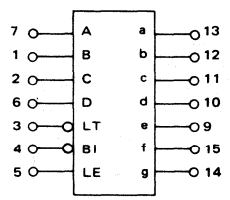
BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER

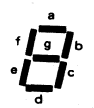


L SUFFIX
CERAMIC PACKAGE
CASE 620



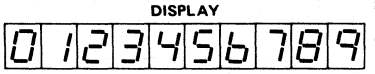
P SUFFIX
PLASTIC PACKAGE
CASE 648





V_{DD} = Pin 16
V_{SS} = Pin 8

DISPLAY



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14511AL — MC14511CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
Operating Temperature Range — MC14511AL — MC14511CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output†‡	P_{OHmax}	50	mW

† Please refer to derating curves. (Figure 1).

‡ $P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high current mode may occure if V_{in} and V_{out} is not constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't care

* Depends upon the BCD code applied during the 0 to 1 transition of LE.

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14511AL -55°C Min	MC14511AL -55°C Max	MC14511AL +25°C Min	MC14511AL +25°C Typ	MC14511AL +25°C Max	MC14511AL +125°C Min	MC14511AL +125°C Max	MC14511CL/CP -40°C Min	MC14511CL/CP -40°C Max	MC14511CL/CP +25°C Min	MC14511CL/CP +25°C Typ	MC14511CL/CP +25°C Max	MC14511CL/CP +85°C Min	MC14511CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.1	–	4.1	4.57	–	4.1	–	4.1	–	4.1	4.57	–	4.1	–	
			10	9.1	–	9.1	9.58	–	9.1	–	9.1	–	9.1	9.58	–	9.1	–	
			15	–	–	–	14.59	–	–	–	–	–	–	14.59	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Voltage																		Vdc
(I_{OH} = 0 mAdc) Source	1	V_{OH}	5.0	–	–	4.10	4.57	–	–	–	–	–	4.10	4.57	–	–	–	
(I_{OH} = 5.0 mAdc)				–	–	–	4.24	–	–	–	–	–	–	4.24	–	–	–	
(I_{OH} = 10 mAdc)				–	–	3.90	4.12	–	–	–	–	–	3.60	4.12	–	–	–	
(I_{OH} = 15 mAdc)				–	–	–	3.94	–	–	–	–	–	–	3.94	–	–	–	
(I_{OH} = 20 mAdc)				–	–	3.40	3.75	–	–	–	–	–	2.80	3.75	–	–	–	
(I_{OH} = 25 mAdc)				–	–	–	3.54	–	–	–	–	–	–	3.54	–	–	–	
(I_{OH} = 0 mAdc)			10	–	–	9.10	9.58	–	–	–	–	–	9.10	9.58	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)				–	–	–	9.26	–	–	–	–	–	–	9.26	–	–	–	
(I_{OH} = 10 mAdc)				–	–	9.0	9.17	–	–	–	–	–	8.75	9.17	–	–	–	
(I_{OH} = 15 mAdc)				–	–	–	9.04	–	–	–	–	–	–	9.04	–	–	–	
(I_{OH} = 20 mAdc)				–	–	8.60	8.90	–	–	–	–	–	8.10	8.90	–	–	–	
(I_{OH} = 25 mAdc) †				–	–	–	8.75	–	–	–	–	–	–	8.75	–	–	–	
(I_{OH} = 0 mAdc)			15	–	–	–	14.59	–	–	–	–	–	–	14.59	–	–	–	Vdc
(I_{OH} = 5.0 mAdc)				–	–	–	14.27	–	–	–	–	–	–	14.27	–	–	–	
(I_{OH} = 10 mAdc) †				–	–	–	14.18	–	–	–	–	–	–	14.18	–	–	–	
(I_{OH} = 15 mAdc) †				–	–	–	14.07	–	–	–	–	–	–	14.07	–	–	–	
(I_{OH} = 20 mAdc) †				–	–	–	13.95	–	–	–	–	–	–	13.95	–	–	–	
(I_{OH} = 25 mAdc) †				–	–	–	13.80	–	–	–	–	–	–	13.80	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	pF
Quiescent Dissipation**	–	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (88 mW/MHz) f+0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (350 mW/MHz) f+0.0001 mW			10	–	0.10	–	0.0001	0.10	–	6.0	–	1.0	–	0.0001	1.0	–	14	
P_D = (790 mW/MHz) f+0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**		t_r																ns
(C_L = 15 pF)	2(a)																	
t_r = (0.18 ns/pF) C_L + 27 ns			5.0	–	–	–	30	175	–	–	–	–	–	30	200	–	–	
t_r = (0.14 ns/pF) C_L + 15 ns			10	–	–	–	17	75	–	–	–	–	–	17	110	–	–	
t_r = (0.11 ns/pF) C_L + 13 ns			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Output Fall Time	2(a)	t_f																ns
(C_L = 15 pF)																		
			5.0	–	–	–	1000	–	–	–	–	–	–	1000	–	–	–	
			10	–	–	–	1000	–	–	–	–	–	–	1000	–	–	–	
			15	–	–	–	1000	–	–	–	–	–	–	1000	–	–	–	

†See Derating Curve (Figure 1).

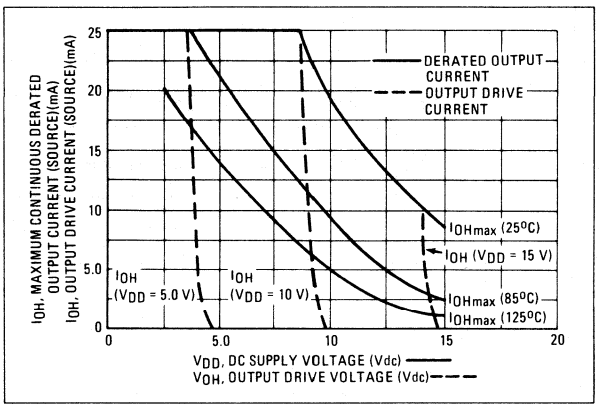
(Continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14511AL							MC14511CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Turn-Off Delay Time (Data)** (C_L = 15 pF)	2(a)	t_{PLH}																ns
t_{PLH} = (0.40 ns/pF) C_L + 635 ns			5.0	–	–	–	640	1500	–	–	–	–	–	640	2250	–	–	
t_{PLH} = (0.25 ns/pF) C_L + 245 ns			10	–	–	–	250	600	–	–	–	–	–	250	900	–	–	
t_{PLH} = (0.20 ns/pF) C_L + 170 ns			15	–	–	–	175	–	–	–	–	–	–	175	–	–	–	
Turn-On Delay Time (Data)** (C_L = 15 pF)	2(a)	t_{PHL}																ns
t_{PHL} = (1.3 ns/pF) C_L + 700 ns			5.0	–	–	–	720	1500	–	–	–	–	–	720	2250	–	–	
t_{PHL} = (0.60 ns/pF) C_L + 280 ns			10	–	–	–	290	600	–	–	–	–	–	290	900	–	–	
t_{PHL} = (0.35 ns/pF) C_L + 190 ns			15	–	–	–	195	–	–	–	–	–	–	195	–	–	–	
Turn-Off Delay Time (Blank)** (C_L = 15 pF)	2(a)	t_{PLH}																ns
t_{PLH} = (0.30 ns/pF) C_L + 315 ns			5.0	–	–	–	320	1000	–	–	–	–	–	320	1500	–	–	
t_{PLH} = (0.25 ns/pF) C_L + 125 ns			10	–	–	–	130	400	–	–	–	–	–	130	600	–	–	
t_{PLH} = (0.15 ns/pF) C_L + 95 ns			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Turn-On Delay Time (Blank)** (C_L = 15 pF)	2(a)	t_{PHL}																ns
t_{PHL} = (0.85 ns/pF) C_L + 470 ns			5.0	–	–	–	485	1000	–	–	–	–	–	485	1500	–	–	
t_{PHL} = (0.45 ns/pF) C_L + 195 ns			10	–	–	–	200	400	–	–	–	–	–	200	600	–	–	
t_{PHL} = (0.35 ns/pF) C_L + 155 ns			15	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
Turn-Off Delay Time (Lamp Test)** (C_L = 15 pF)	2(a)	t_{PLH}																ns
t_{PLH} = (0.45 ns/pF) C_L + 285 ns			5.0	–	–	–	290	625	–	–	–	–	–	290	940	–	–	
t_{PLH} = (0.25 ns/pF) C_L + 120 ns			10	–	–	–	125	250	–	–	–	–	–	125	375	–	–	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns			15	–	–	–	85	–	–	–	–	–	–	85	–	–	–	
Turn-On Delay Time (Lamp Test)** (C_L = 15 pF)	2(a)	t_{PHL}																ns
t_{PHL} = (1.3 ns/pF) C_L + 270 ns			5.0	–	–	–	290	625	–	–	–	–	–	290	940	–	–	
t_{PHL} = (0.45 ns/pF) C_L + 115 ns			10	–	–	–	120	250	–	–	–	–	–	120	375	–	–	
t_{PHL} = (0.35 ns/pF) C_L + 85 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Setup Time	2(b)	t_{setup}																ns
			5.0	–	–	180	90	–	–	–	–	–	270	90	–	–	–	
			10	–	–	76	38	–	–	–	–	–	114	38	–	–	–	
			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Hold Time	2(b)	t_{hold}																ns
			5.0	–	–	0	-90	–	–	–	–	–	90	-90	–	–	–	
			10	–	–	0	-38	–	–	–	–	–	38	-38	–	–	–	
			15	–	–	–	-20	–	–	–	–	–	–	-20	–	–	–	
Minimum Latch Enable Pulse Width	2(c)	PW_{LE}																ns
			5.0	–	–	520	260	–	–	–	–	–	780	260	–	–	–	
			10	–	–	220	110	–	–	–	–	–	330	110	–	–	–	
			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

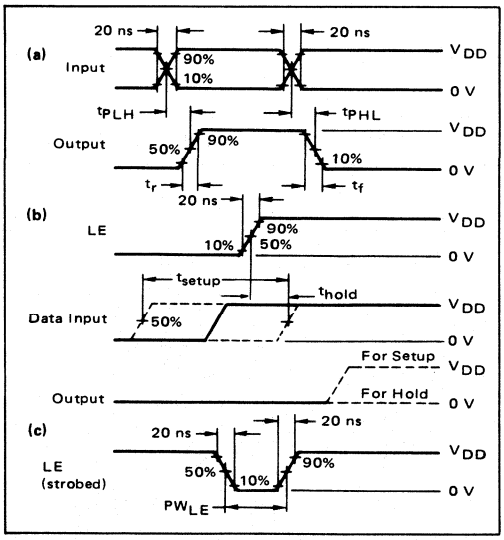
FIGURE 1 – DERATING AND OUTPUT DRIVE CURVES PER OUTPUT



The maximum continuous (worst case) derated output drive current applies to a single output with all other outputs sourcing an equal amount of current. Operation above the derating curve at a given temperature is not recommended.

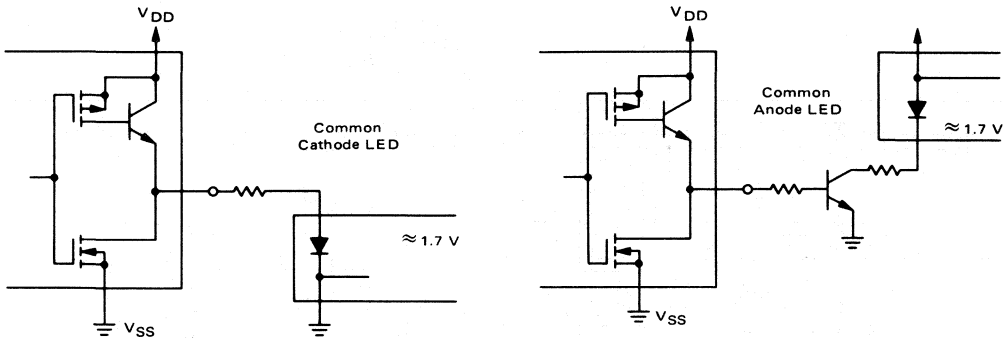
The output drive curves are typical values.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

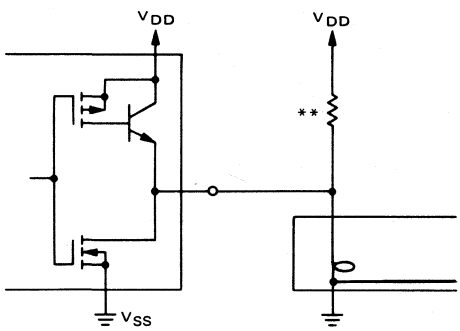


CONNECTIONS TO VARIOUS DISPLAY READOUTS

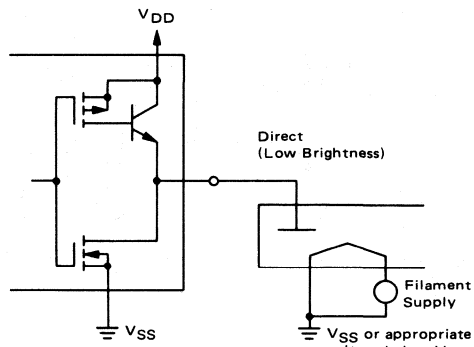
LIGHT EMITTING DIODE (LED) READOUT



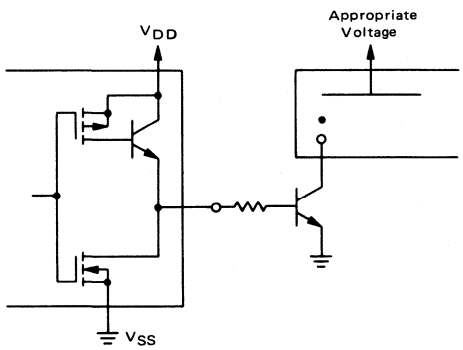
INCANDESCENT READOUT



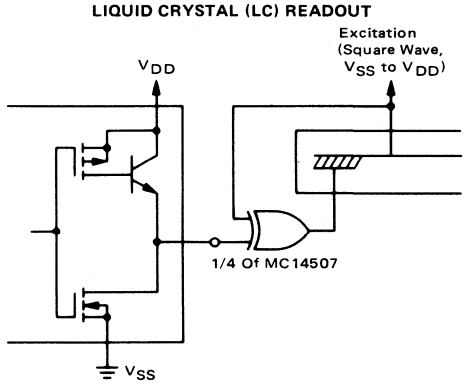
FLUORESCENT READOUT



GAS DISCHARGE READOUT



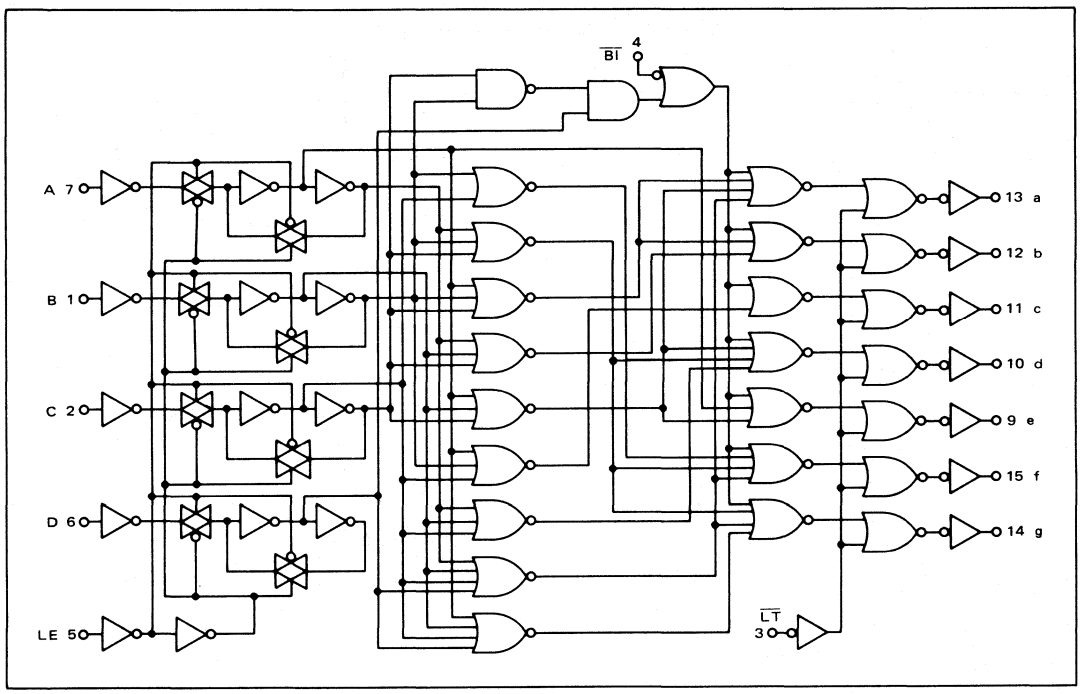
LIQUID CRYSTAL (LC) READOUT



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC's not recommended for life of LC readouts.

LOGIC DIAGRAM



MC14512AL
MC14512CL
MC14512CP

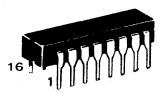
8-CHANNEL DATA SELECTOR

The MC14512 is an 8-channel data selector constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This data selector finds primary application in signal multiplexing functions. It may also be used for data routing, digital signal switching, signal gating, and number sequence generation.

- Quiescent Power Dissipation = 250 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- High Fanout > 50
- Single Supply Operation – Positive or Negative
- 3-State Output (Logic "1", Logic "0", High Impedance)

McMOS
(LOW-POWER COMPLEMENTARY MOS)

8-CHANNEL DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

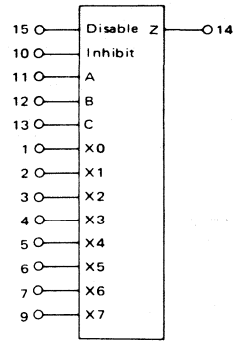
Rating		Symbol	Value	Unit
DC Supply Voltage	MC14512AL MC14512CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14512AL – MC14512CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

C	B	A	INHIBIT	DISABLE	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ϕ	ϕ	ϕ	1	0	0
ϕ	ϕ	ϕ	ϕ	1	High Impedance

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14512AL -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC14512CL/CP -40°C Min	-40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geqslant 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geqslant 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geqslant 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leqslant 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leqslant 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leqslant 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
3-State Output Leakage Current (C_L = 15 pF)	3	I_{TL}	5.0	–	±0.05	–	±0.0005	±0.05	–	±3.0	–	±0.5	–	±0.0005	±0.5	–	±7.0	µAdc
			10	–	±0.1	–	±0.001	±0.1	–	±6.0	–	±1.0	–	±0.001	±0.1	–	±14	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation **† (C_L = 15 pF, f = 0 Hz)	–	P_Q																mW
			5.0	–	0.025	–	0.00025	0.025	–	1.5	–	0.25	–	0.00025	0.25	–	3.5	
			10	–	0.1	–	0.001	0.1	–	6.0	–	1.0	–	0.001	1.0	–	14	
			15	–	–	–	0.0023	–	–	–	–	–	–	0.0023	–	–	–	
Total Power Dissipation (Dynamic Plus Quiescent) (C_L = 15 pF)	1	P_D	5.0	$P_D = (3.0\ mW/MHz)\ f + 0.00025\ mW$														mW
			10	$P_D = (13\ mW/MHz)\ f + 0.001\ mW$														
			15	$P_D = (29\ mW/MHz)\ f + 0.0023\ mW$														
Output Rise Time** (C_L = 15 pF)	2	t_r																ns
$t_r = (3.0\ ns/pF)\ C_L + 55\ ns$			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
$t_r = (1.5\ ns/pF)\ C_L + 27\ ns$			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
$t_r = (1.1\ ns/pF)\ C_L + 20\ ns$			15	–	–	–	37	–	–	–	–	–	–	37	–	–	–	
Output Fall Time** (C_L = 15 pF)	2	t_f																ns
$t_f = (1.5\ ns/pF)\ C_L + 77\ ns$			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
$t_f = (0.75\ ns/pF)\ C_L + 39\ ns$			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
$t_f = (0.55\ ns/pF)\ C_L + 29\ ns$			15	–	–	–	37	–	–	–	–	–	–	37	–	–	–	
Turn-Off Delay Time** (C_L = 15 pF)	2	t_{PLH}																ns
$t_{PLH} = (0.9\ ns/pF)\ C_L + 211\ ns$			5.0	–	–	–	225	500	–	–	–	–	–	225	750	–	–	
$t_{PLH} = (0.3\ ns/pF)\ C_L + 70\ ns$			10	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
$t_{PLH} = (0.23\ ns/pF)\ C_L + 54\ ns$			15	–	–	–	57	–	–	–	–	–	–	57	–	–	–	
Turn-On Delay Time** (C_L = 15 pF)	2	t_{PHL}																ns
$t_{PHL} = (2.7\ ns/pF)\ C_L + 184\ ns$			5.0	–	–	–	225	500	–	–	–	–	–	225	750	–	–	
$t_{PHL} = (0.9\ ns/pF)\ C_L + 61\ ns$			10	–	–	–	75	175	–	–	–	–	–	75	200	–	–	
$t_{PHL} = (0.68\ ns/pF)\ C_L + 47\ ns$			15	–	–	–	57	–	–	–	–	–	–	57	–	–	–	
3-State Output "1" to High Z (C_L = 15 pF)	3	$t_{"1"H}$																ns
			5.0	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			10	–	–	–	25	75	–	–	–	–	–	25	100	–	–	
			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	
3-State Output "0" to High Z (C_L = 15 pF)	3	$t_{"0"H}$																ns
			5.0	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			10	–	–	–	25	75	–	–	–	–	–	25	100	–	–	
			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	
3-State Output High Z to "1" (C_L = 15 pF)	3.	$t_{H"1"}$																ns
			5.0	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			10	–	–	–	25	75	–	–	–	–	–	25	100	–	–	
			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	
3-State Output High Z to "0" (C_L = 15 pF)	3	$t_{H"0"}$																ns
			5.0	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
			10	–	–	–	25	75	–	–	–	–	–	25	100	–	–	
			15	–	–	–	19	–	–	–	–	–	–	19	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refer to corresponding formula:

$P_T(C_L) = P_D + 1/2 \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

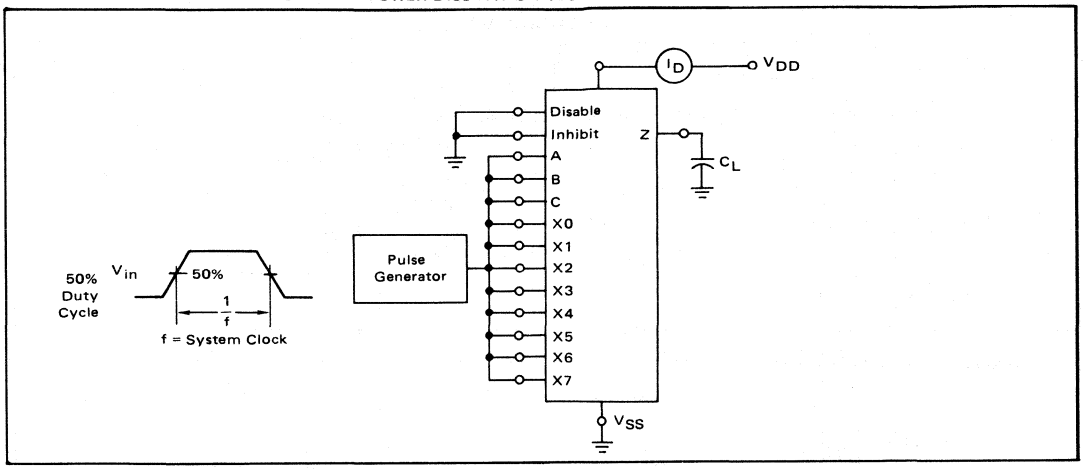
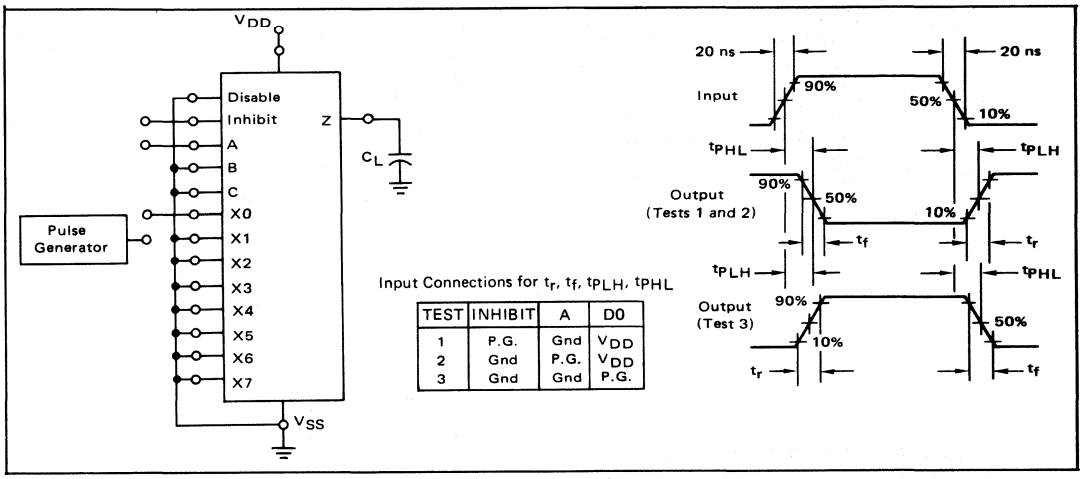


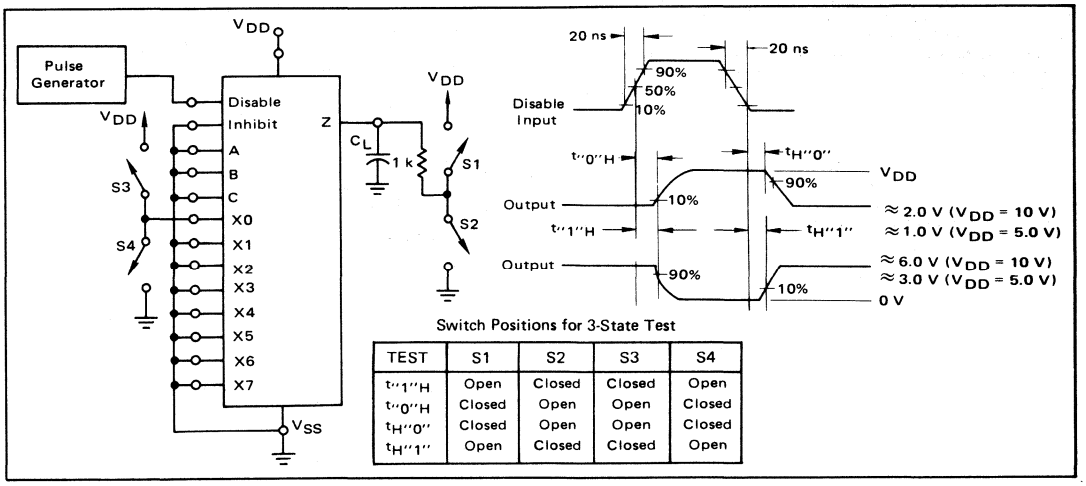
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

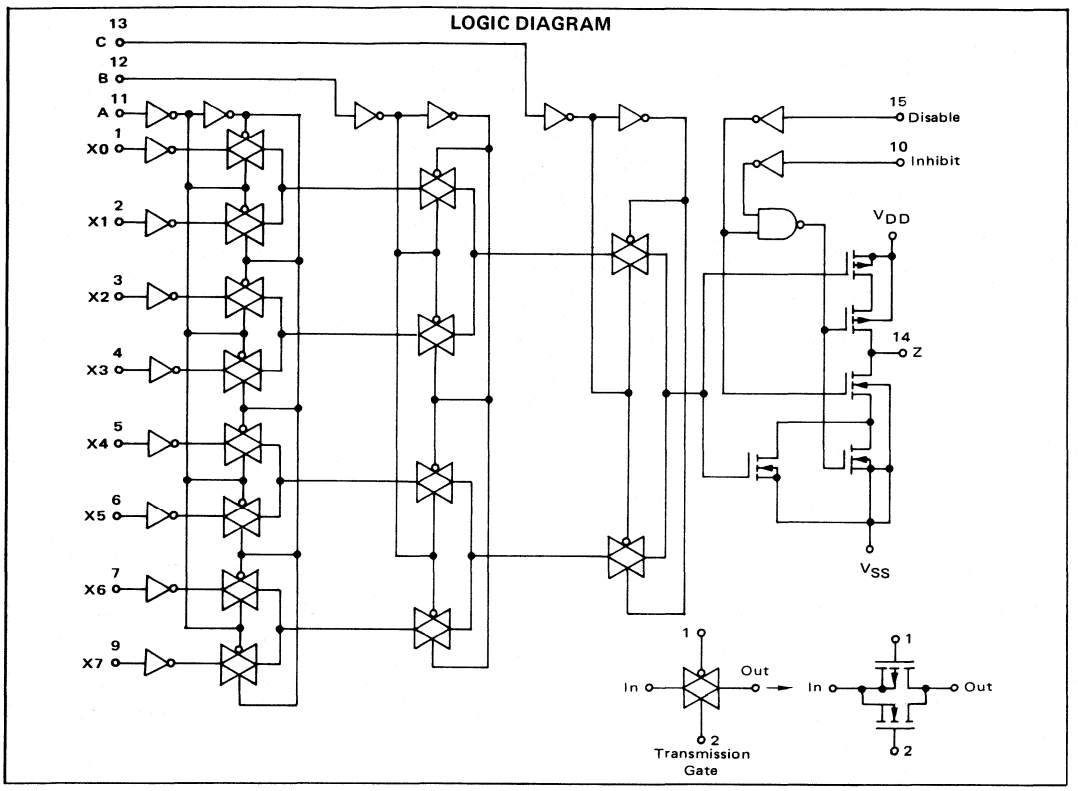
TEST	INHIBIT	A	D0
1	P.G.	Gnd	V_{DD}
2	Gnd	P.G.	V_{DD}
3	Gnd	Gnd	P.G.

FIGURE 3 – 3-STATE AC TEST CIRCUIT AND WAVEFORM



Switch Positions for 3-State Test

TEST	S1	S2	S3	S4
$t_{"1"H}$	Open	Closed	Closed	Open
$t_{"0"H}$	Closed	Open	Open	Closed
$t_{H"0"}$	Closed	Open	Open	Closed
$t_{H"1"}$	Open	Closed	Closed	Open

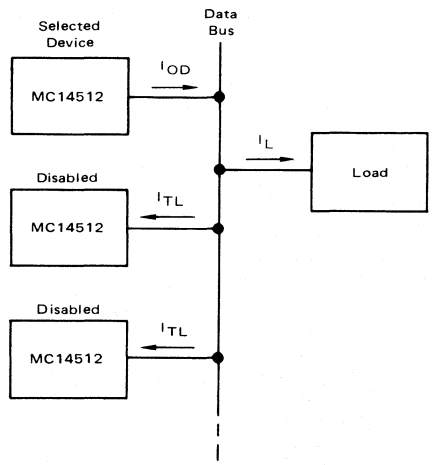


3-STATE MODE OF OPERATION

Output terminals of several MC14512 8-Bit Data Selectors can be connected to a single data bus as shown. One MC14512 is selected by the 3-state control, and the remaining devices are disabled into a high impedance "off" state. The number of 8-bit data selectors, N, that may be connected to a bus line is determined from the output drive current, I_{OD}, 3-state-or disable output leakage current, I_{TL}, and the load current, I_L, required to drive the bus line (including fanout to other device inputs), and can be calculated by:

$$N = \frac{I_{OD} - I_L}{I_{TL}} + 1$$

N must be calculated for both high and low logic states of the bus line.



MC14514AL
MC14514CL
MC14515AL
MC14515CL

4-BIT LATCH/4-TO-16 LINE DECODER

The MC14514AL/CL and MC14515AL/CL are two output options of a 4 to 16 line decoder with latched inputs. The MC14514 (output active high option) presents a logical "1" at the selected output, whereas the MC14515 (output active low option) presents a logical "0" at the selected output. The latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". These high and low options of a 4-bit latch/4 to 16 line decoder are constructed with N-channel and P-channel enhancement mode devices in a single monolithic structure. The latches are R-S type flip-flops and data is admitted upon a signal incident at the strobe input, decoded, and presented at the output.

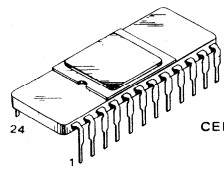
These complementary circuits find primary use in decoding applications where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 0.2 μW package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14514AL, MC14515AL)
  = 3.0 Vdc to 16 Vdc (MC14514CL, MC14515CL)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Low Input Capacitance – 5.0 pF typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT LATCH/4-TO-16 LINE DECODER



L SUFFIX
CERAMIC PACKAGE
CASE 684

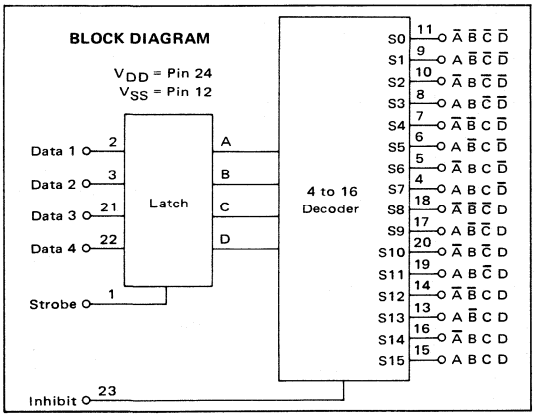
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14514AL,MC14515AL MC14514CL,MC14515CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain Per Pin		I	10	mAdc
Operating Temperature Range	MC14514AL,MC14515AL MC14514CL,MC14515CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS D	C	B	A	SELECTED OUTPUT MC14514 = Logic "1" MC14515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, MC14514 All Outputs = 1, MC14515

X = Don't Care

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14514AL, MC14515AL							MC14514CL, MC14515CL							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	1																	mAdc
(V_{OH} = 2.5 Vdc) Source		I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF, f = 0 Hz)	–	P_Q																mW
			5.0	–	0.025	–	0.0001	0.025	–	1.5	–	0.25	–	0.0001	0.25	–	3.5	
			10	–	0.10	–	0.0002	0.10	–	6.0	–	1.0	–	0.0002	1.0	–	14	
			15	–	–	–	0.0004	–	–	–	–	–	–	0.0004	–	–	–	
Total Power Dissipation† (Quiescent Plus Dynamic) (C_L = 15 pF)	2	P_D																mW
			5.0	P_D = (5.0 mW/MHz) f + 0.0001 mW														
			10	P_D = (20 mW/MHz) f + 0.0002 mW														
			15	P_D = (45 mW/MHz) f + 0.0004 mW														
Output Rise Time** (C_L = 15 pF)	3	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time** (C_L = 15 pF)	3	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L +17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off, Turn-On Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 774 ns			5.0	–	–	–	800	1350	–	–	–	–	–	800	2000	–	–	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 289 ns			10	–	–	–	300	500	–	–	–	–	–	300	750	–	–	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 217 ns			15	–	–	–	225	–	–	–	–	–	–	225	–	–	–	
Setup Time (C_L = 15 pF)	3	t_{setup}																ns
			5.0	–	–	–	150	250	–	–	–	–	–	150	400	–	–	
			10	–	–	–	60	100	–	–	–	–	–	60	150	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Strobe Pulse Width (C_L = 15 pF)	3	PW_{ST}																ns
			5.0	–	–	–	200	350	–	–	–	–	–	200	500	–	–	
			10	–	–	–	60	100	–	–	–	–	–	60	150	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Inhibit Propagation Times** Turn-Off, Turn-On Delay Time (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.75 ns/pF) C_L + 324 ns			5.0	–	–	–	350	700	–	–	–	–	–	350	1000	–	–	
t_{PLH}, t_{PHL} = (0.70 ns/pF) C_L + 139 ns			10	–	–	–	150	250	–	–	–	–	–	150	400	–	–	
t_{PLH}, t_{PHL} = (0.53 ns/pF) C_L + 112 ns			15	–	–	–	120	–	–	–	–	–	–	120	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†$P_T(C_L) = P_D + 2.0 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$

Where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

7

FIGURE 1 – DRAIN CHARACTERISTICS TEST CIRCUIT

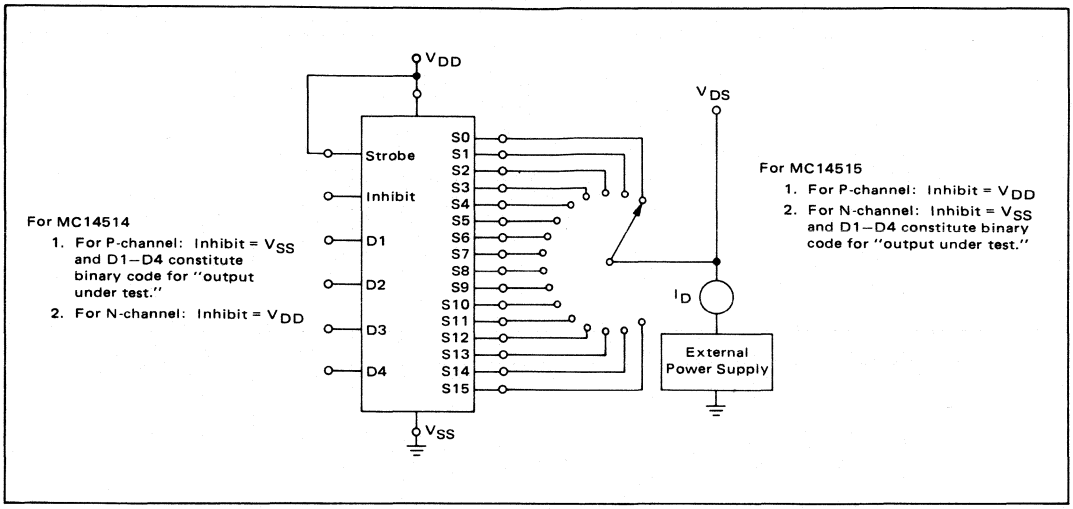


FIGURE 2 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

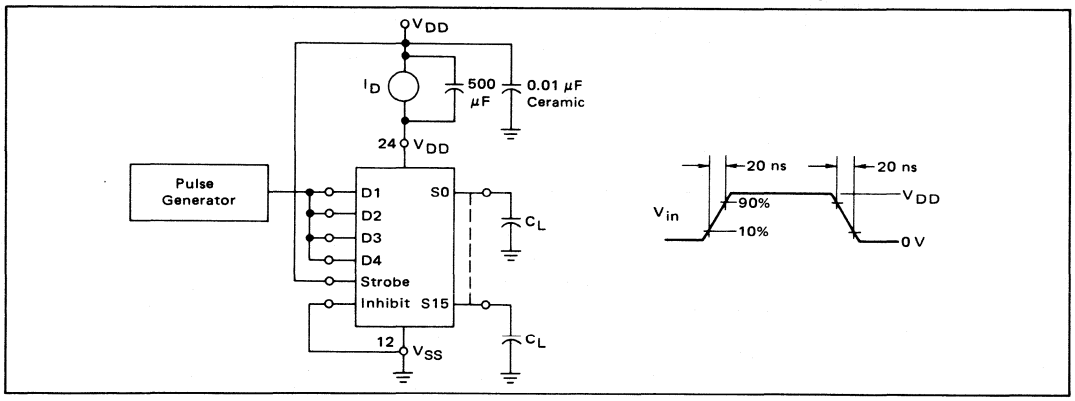
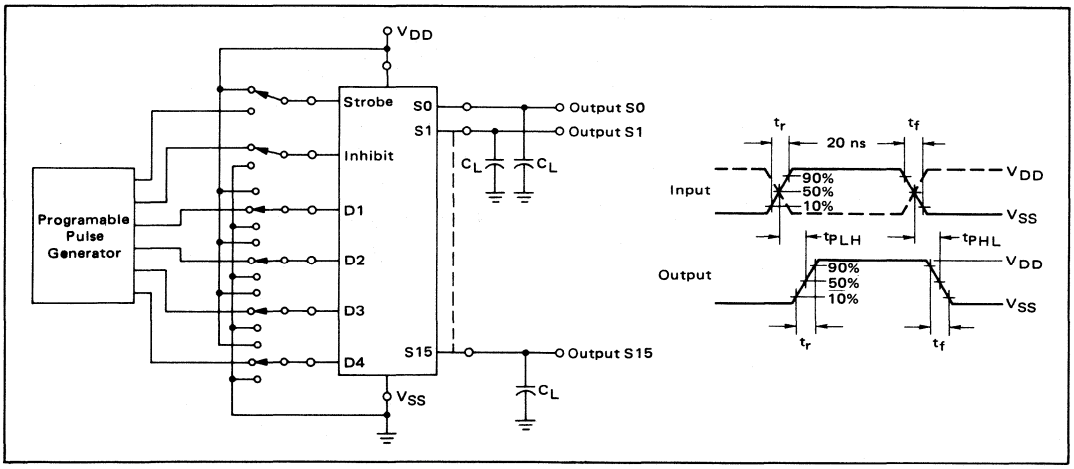
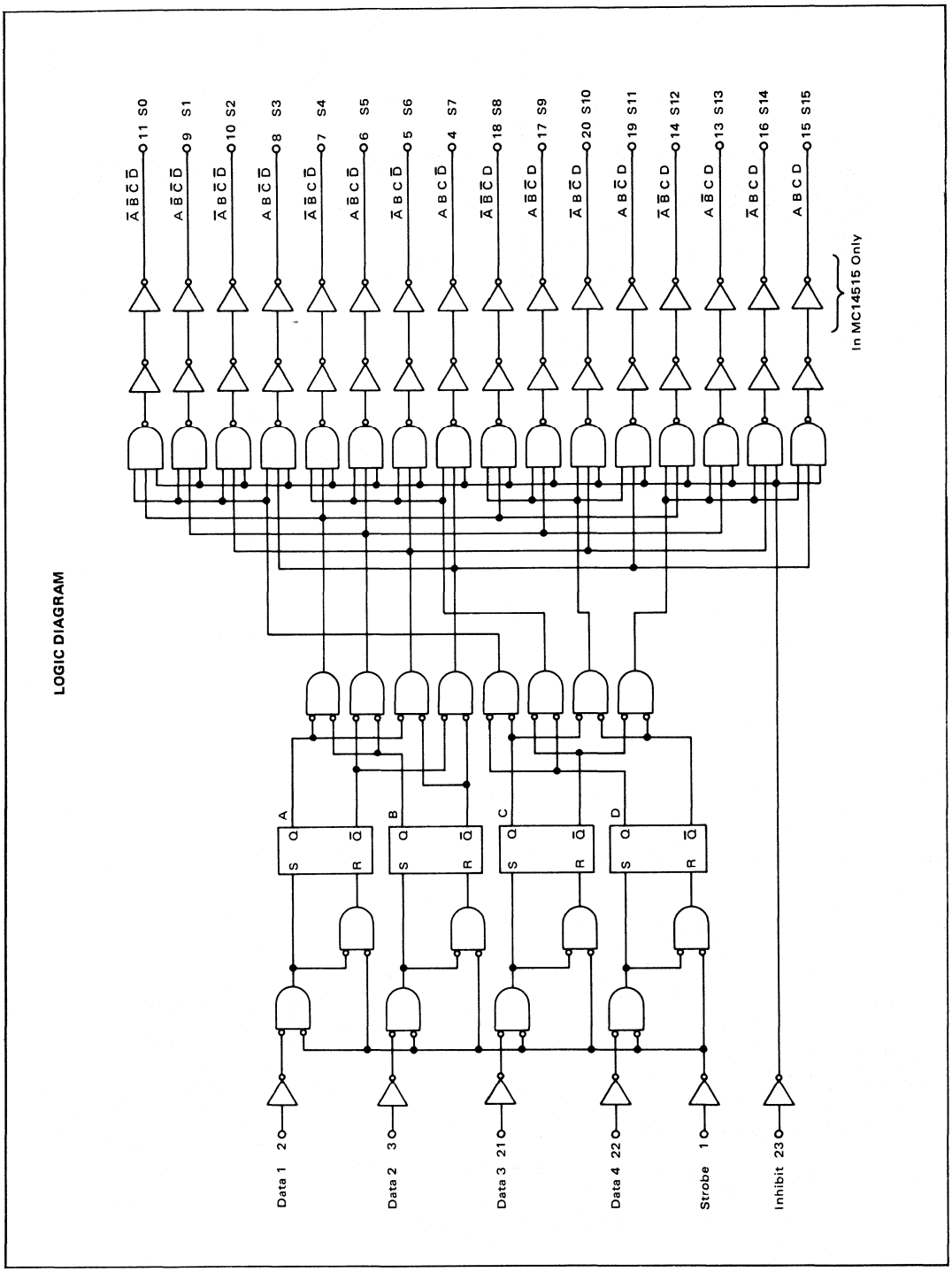


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM



COMPLEX DATA ROUTING

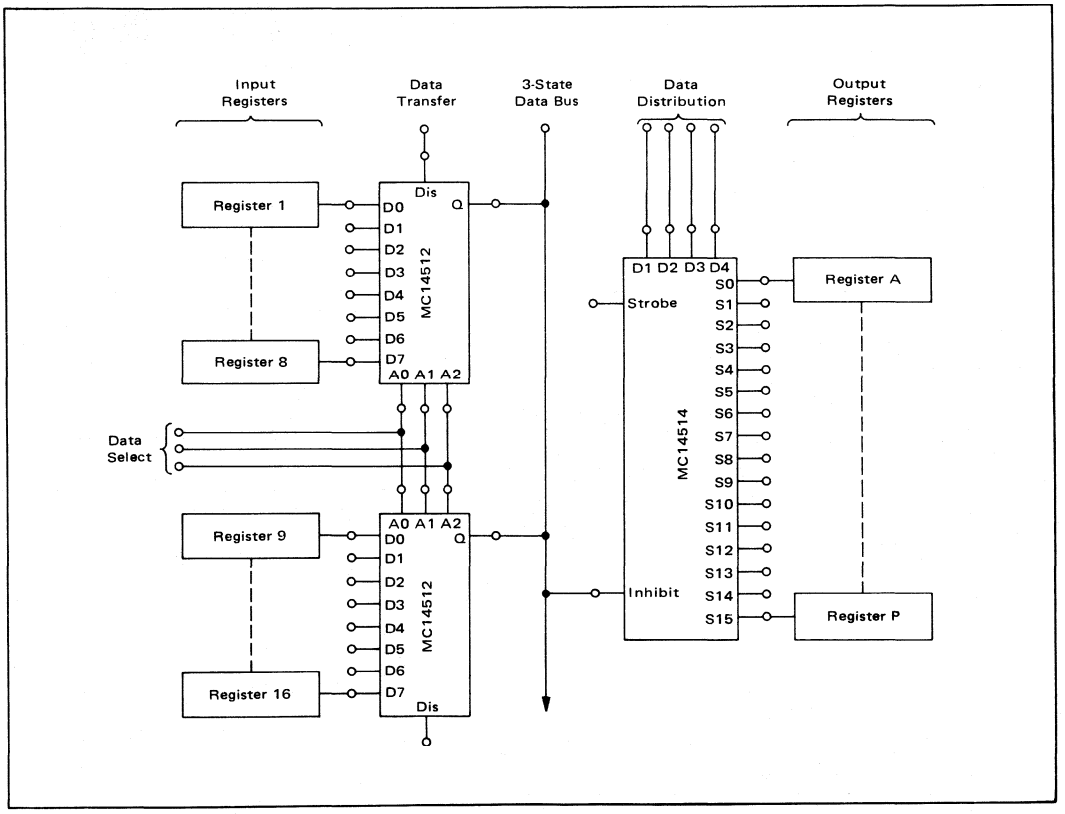
Two MC14512 eight-channel data selectors are used here with the MC14514 four-bit latched-decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a 3-state data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the eight inputs on both MC14512 data selectors. One register is assigned to each input. The signals on A0, A1, and A2 choose one of eight inputs for transfer out to the 3-state data bus. A fourth signal, labelled Dis, disables one of the MC14512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1 thru 16, the rate of transfer of the sequential information can also be varied. That is, if the MC14512 were addressed at a rate that is eight times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the 3-state bus is redistributed by the MC14514 four-bit latch-decoder. Using the four-bit address, D1 thru D4, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A thru P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.

DATA ROUTING SYSTEM



MC14516AL
MC14516CL
MC14516CP

COUNTER

BINARY UP/DOWN COUNTER

The MC14516 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This complementary MOS circuit finds primary use where low power dissipation and/or high noise immunity is desired.

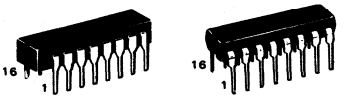
This binary presettable up/down counter may be used as a counting/frequency synthesizer, in A/D and D/A conversion, for up/down counting, for magnitude and sign generation, and for difference counting.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14516AL)
  = 3.0 Vdc to 16 Vdc (MC14516CL/CP)
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Logic Edge-Clocked Design – Count Occurs on Positive Going Edge of Clock
- 6.0-MHz Counting Rate
- Single Pin Reset

McMOS

(LOW-POWER COMPLEMENTARY MOS)

BINARY UP/DOWN COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

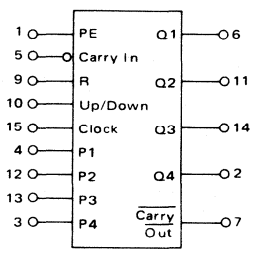
Rating	Symbol	Value	Unit
DC Supply Voltage — MC14516AL —MC14516CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range— MC14516AL -MC14516CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

$\overline{\text{CARRY IN}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
1	X	0	0	No Count
0	1	0	0	Count Up
0	0	0	0	Count Down
X	X	1	0	Preset
X	X	X	1	Reset

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

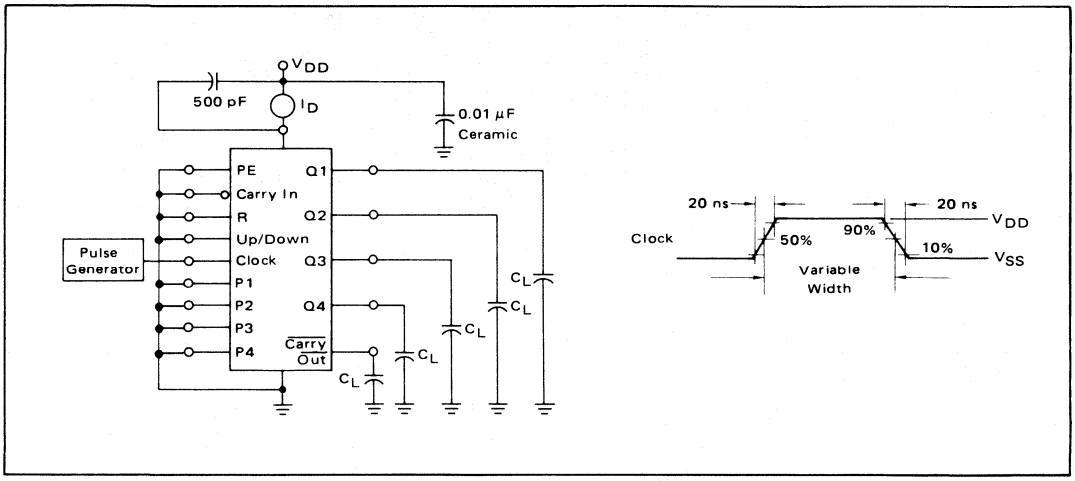
Characteristic	Figure	Symbol	V_{DD}	MC14516AL						MC14516CL/CP						Unit
				-55°C		+25°C			+125°C	-40°C		+25°C			+85°C	
			Vdc	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 25. Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.5	-1.3	–	-0.35	–	-0.23	–	-0.2	-1.3	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.4	0.6	–	0.28	–	0.23	–	0.2	0.6	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.6	–	0.65	–	0.6	–	0.5	1.6	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}																pF
Reset			–	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
All other inputs			–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Quiescent Dissipation	1	P_D	5.0	–	25	–	0.25	25	–	1500	–	250	–	0.25	250	–	3500	μW
			10	–	100	–	1.0	100	–	6000	–	1000	–	1.0	1000	–	14000	
Output Rise and Fall Time**	2	t_r, t_f																ns
(C_L = 15 pF)																		
t_r, t_f = (2.9 ns/pF) C_L + 57 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (1.0 ns/pF) C_L + 10 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock to Q Propagation Delay Time**	2	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF)																		
t_{PHL}, t_{PLH} = (1.8 ns/pF) C_L + 222 ns			5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	
t_{PHL}, t_{PLH} = (0.8 ns/pF) C_L + 88 ns			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 66 ns			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Clock to $\overline{\text{Carry Out}}$	2	t_{PHL}, t_{PLH}	5.0	–	–	–	300	750	–	–	–	–	–	300	1200	–	–	ns
Propagation Delay Time (C_L = 15 pF)			10	–	–	–	125	250	–	–	–	–	–	125	400	–	–	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	2	t_{PHL}, t_{PLH}	5.0	–	–	–	100	250	–	–	–	–	–	100	500	–	–	ns
Propagation Delay Time (C_L = 15 pF)			10	–	–	–	40	100	–	–	–	–	–	40	200	–	–	
Minimum Clock Pulse Width	2	PW_C	5.0	–	–	–	125	340	–	–	–	–	–	125	500	–	–	ns
			10	–	–	–	50	170	–	–	–	–	–	50	200	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)	2	PRF	5.0	–	–	1.5	3.0	–	–	–	–	–	1.0	3.0	–	–	–	MHz
			10	–	–	3.0	7.0	–	–	–	–	–	2.5	7.0	–	–	–	
Preset or Reset to Q_{out}	2	t_{PHL}, t_{PLH}	5.0	–	–	–	325	650	–	–	–	–	–	325	1000	–	–	ns
Propagation Delay Time (C_L = 15 pF)			10	–	–	–	115	225	–	–	–	–	–	115	300	–	–	
Preset or Reset to Carry Out	2	t_{PHL}, t_{PLH}	5.0	–	–	–	500	850	–	–	–	–	–	500	1700	–	–	ns
Propagation Delay Time (C_L = 15 pF)			10	–	–	–	200	300	–	–	–	–	–	200	600	–	–	
Preset or Reset Removal Time†	2	t_{rem}	5.0	–	–	–	325	650	–	–	–	–	–	325	1000	–	–	ns
			10	–	–	–	115	225	–	–	–	–	–	115	300	–	–	
Maximum Clock Rise and Fall Time	2	t_r, t_f	5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	μs
			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
Carry In Setup Time	2	t_{setup}	5.0	–	–	–	130	300	–	–	–	–	–	130	600	–	–	ns
			10	–	–	–	60	125	–	–	–	–	–	60	250	–	–	
Up/Down Setup Time	2	t_{setup}	5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	ns
			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
Minimum Preset Enable or Reset Pulse Width	2	PW_{PE}, PW_R	5.0	–	–	–	100	325	–	–	–	–	–	100	500	–	–	ns
			10	–	–	–	50	100	–	–	–	–	–	50	125	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

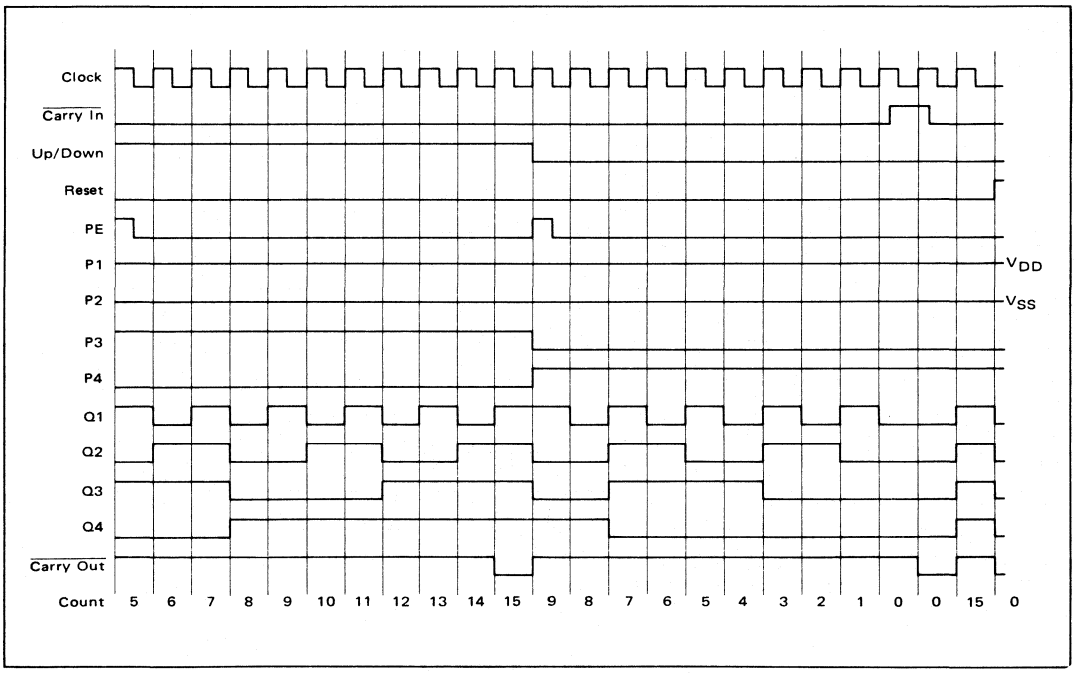
**The formula given is for the typical characteristics only.

†The Preset or Reset signal must be low prior to a positive-going transition of the clock.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

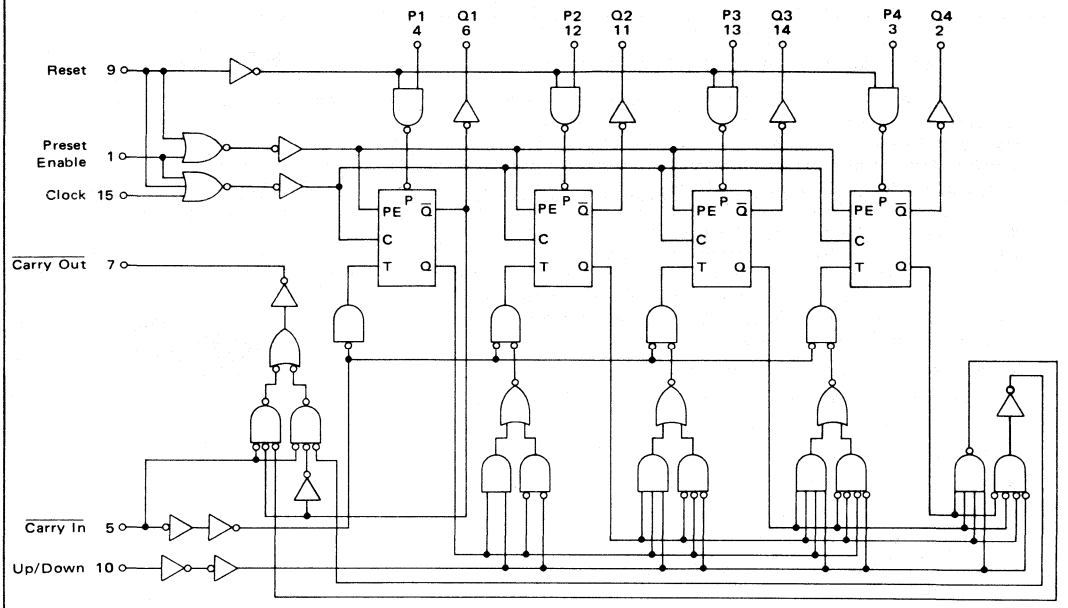


TIMING DIAGRAM

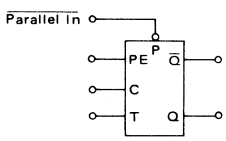


7

LOGIC DIAGRAM



TOGGLE FLIP-FLOP

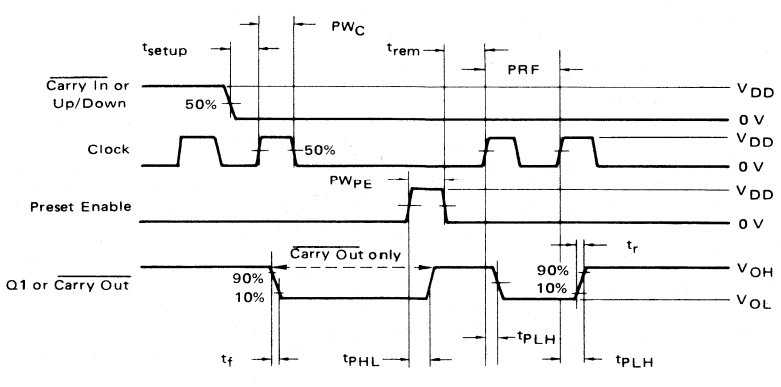


FLIP-FLOP FUNCTIONAL TRUTH TABLE

PRESET ENABLE	CLOCK	TOGGLE ENABLE	Q_{n+1}
1	X	X	Parallel In
0	⎍	0	Q_n
0	⎍	1	$\overline{Q}_n$
0	⎎	X	Q_n

X = Don't Care

FIGURE 2 – SWITCHING TIME WAVEFORMS



MC14517AL
MC14517CL

SHIFT REGISTER

DUAL 64-BIT STATIC SHIFT REGISTER

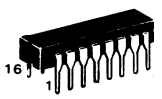
The MC14517 dual 64-bit static shift register consists of two identical, independent, 64-bit registers. Each register has separate clock and write enable inputs, as well as outputs at bits 16, 32, 48, and 64. Data at the data input is entered by clocking, regardless of the state of the write enable input. An output is disabled (open circuited) when the write enable input is high. During this time, data appearing at the data input as well as the 16-bit, 32-bit, and 48-bit taps may be entered into the device by application of a clock pulse. This feature permits the register to be loaded with 64 bits in 16 clock periods, and also permits bus logic to be used. This device is useful in time delay circuits, temporary memory storage circuits, and other serial shift register applications.

- Quiescent Power Dissipation = 10 μW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Fully Static Operation
- Output Transitions Occur on the Rising Edge of the Clock Pulse
- 6.7 MHz Operation @ V_{DD} = 10 Vdc
- Cascadable to Provide Longer Shift Register Lengths
- Exceedingly Slow Input Transition Rates May Be Applied to the Clock Input
- 3-State Output at 64th-Bit Allows Use in Bus Logic Applications
- Shift Registers of any Length may be Fully Loaded with 16 Clock Pulses

McMOS

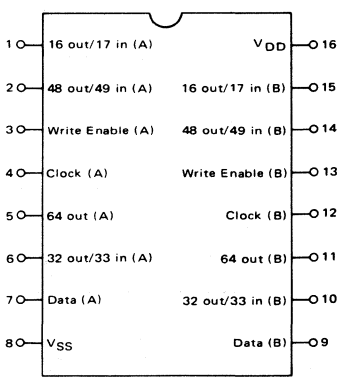
(LOW-POWER COMPLEMENTARY MOS)

DUAL 64-BIT STATIC SHIFT REGISTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14517AL –MC14517CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14517AL –MC14517CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

FUNCTIONAL TRUTH TABLE

CLOCK	WRITE ENABLE	DATA	16-BIT TAP	32-BIT TAP	48-BIT TAP	64-BIT TAP
0	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
0	1	X	High Impedance	High Impedance	High Impedance	High Impedance
1	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
1	1	X	High Impedance	High Impedance	High Impedance	High Impedance
↓	0	Data entered into 1st Bit	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↓	1	Data entered into 1st Bit	Data at tap entered into 17-Bit	Data at tap entered into 33-Bit	Data at tap entered into 49-Bit	High Impedance
↑	0	X	Content of 16-Bit Displayed	Content of 32-Bit Displayed	Content of 48-Bit Displayed	Content of 64-Bit Displayed
↑	1	X	High Impedance	High Impedance	High Impedance	High Impedance

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14517AL -55°C Min	MC14517AL -55°C Max	MC14517AL +25°C Min	MC14517AL +25°C Typ	MC14517AL +25°C Max	MC14517AL +125°C Min	MC14517AL +125°C Max	MC14517CL -40°C Min	MC14517CL -40°C Max	MC14517CL +25°C Min	MC14517CL +25°C Typ	MC14517CL +25°C Max	MC14517CL +85°C Min	MC14517CL +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} ≥3.5 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≥7.0 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≥10.5 Vdc)																		
(V_{out} ≤1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≤4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**† (C_L = 15 pF)	3	P_D																
$P_D = [0.25 + 1.75 \times 10^{-2} f_o + 1.25 \times 10^{+7} f_o C_L]$			5.0	–	25	–	0.25	25	–	450	–	50	–	0.5	250	–	3900	μW
$P_D = [0.5 + 7.4 \times 10^{-2} f_o + 5 \times 10^{+7} f_o C_L]$			10	–	100	–	0.5	100	–	1800	–	200	–	1.0	1000	–	10000	
$P_D = [1.0 + 1.74 \times 10^{-1} f_o + 1.25 \times 10^{+8} f_o C_L]$			15	–	–	–	1.0	–	–	–	–	–	–	2.0		–	–	
Output Rise and Fall Time** (C_L = 15 pF)	4	t_r, t_f																ns
t_r, t_f = (4.8 ns/pF) C_L + 28 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (2.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (2.2 ns/pF) C_L + 2.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On, Turn-Off Delay Time** (C_L = 15 pF)	4	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (2.0 ns/pF) C_L + 390 ns			5.0	–	–	–	420	500	–	–	–	–	–	420	670	–	–	
t_{PHL}, t_{PLH} = (0.9 ns/pF) C_L + 167.5 ns			10	–	–	–	180	200	–	–	–	–	–	180	250	–	–	
t_{PHL}, t_{PLH} = (0.7 ns/pF) C_L + 109.5 ns			15	–	–	–	120	–	–	–	–	–	–	120	–	–	–	
Minimum Clock Pulse Width PCW = NCW = PW_C	4	PW_C																ns
			5.0	–	–	–	170	250	–	–	–	–	–	170	330	–	–	
			10	–	–	–	75	100	–	–	–	–	–	75	125	–	–	
			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)	4	PRF																MHz
			5.0	–	–	2.0	3.0	–	–	–	–	–	1.5	3.0	–	–	–	
			10	–	–	5.0	6.7	–	–	–	–	–	4.0	6.7	–	–	–	
			15	–	–	–	8.3	–	–	–	–	–	–	8.3	–	–	–	
Maximum Clock Pulse Rise and Fall Time‡	4	t_r, t_f																μs
			5.0	No Maximum Limit							–	–	100	∞	–	–	–	
			10								–	–	100	∞	–	–	–	
			15								–	–	100	∞	–	–	–	
Data to Clock Setup Time	4	t_{setup}																ns
			5.0	–	–	–	-40	-10	–	–	–	–	–	-40	0	–	–	
			10	–	–	–	-15	0	–	–	–	–	–	-15	10	–	–	
			15	–	–	–	0	5	–	–	–	–	–	0	15	–	–	
Data to Clock Hold Time	4	t_{hold}																ns
			5.0	–	–	–	75	120	–	–	–	–	–	75	150	–	–	
			10	–	–	–	25	50	–	–	–	–	–	25	75	–	–	
			15	–	–	–	10	25	–	–	–	–	–	10	35	–	–	
Write Enable to Clock Setup Time	4	t_{setup}																ns
			5.0	–	–	–	170	300	–	–	–	–	–	170	400	–	–	
			10	–	–	–	65	130	–	–	–	–	–	65	200	–	–	
			15	–	–	–	50	80	–	–	–	–	–	50	110	–	–	
Write Enable to Clock Release Time	4	t_{rel}																ns
			5.0	–	–	–	160	280	–	–	–	–	–	160	380	–	–	
			10	–	–	–	55	120	–	–	–	–	–	55	180	–	–	
			15	–	–	–	40	70	–	–	–	–	–	40	100	–	–	

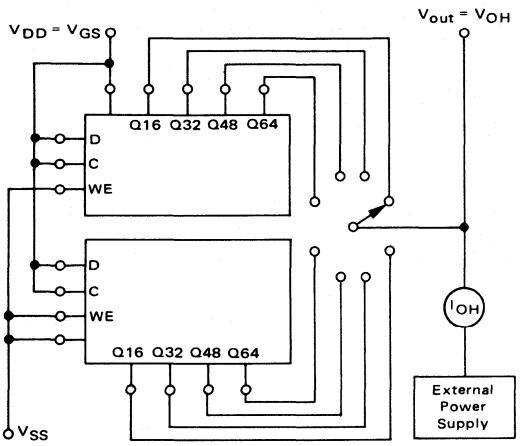
*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†Power dissipation figures and equations are for the package.

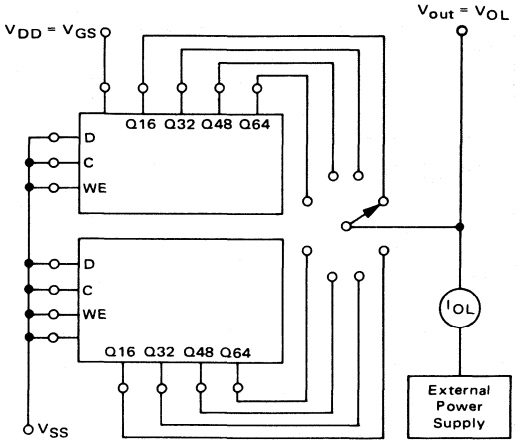
‡When shift register sections are cascaded, the maximum rise and fall time of the clock input should be equal to or less than the rise and fall time of the data outputs, driving data inputs, plus the propagation delay of the output driving stage for the output capacitance load.

FIGURE 1 – TYPICAL OUTPUT SOURCE CURRENT CHARACTERISTICS TEST CIRCUIT



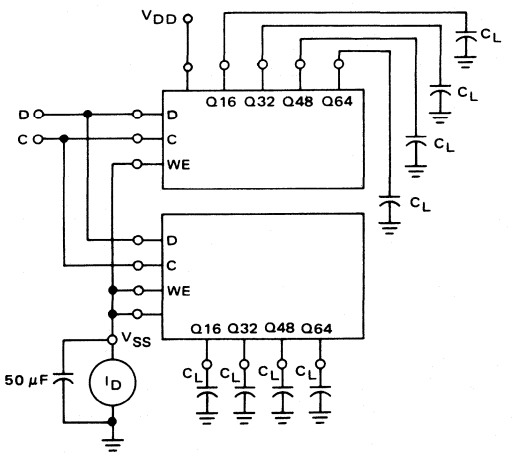
(Output being tested should be in the high-logic state).

FIGURE 2 – TYPICAL OUTPUT SINK CURRENT CHARACTERISTICS TEST CIRCUIT



(Output being tested should be in the low-logic state).

FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



REPETITIVE WAVEFORM

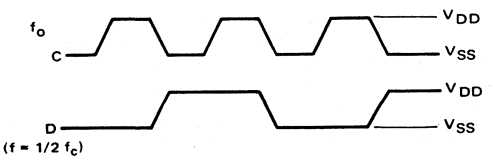


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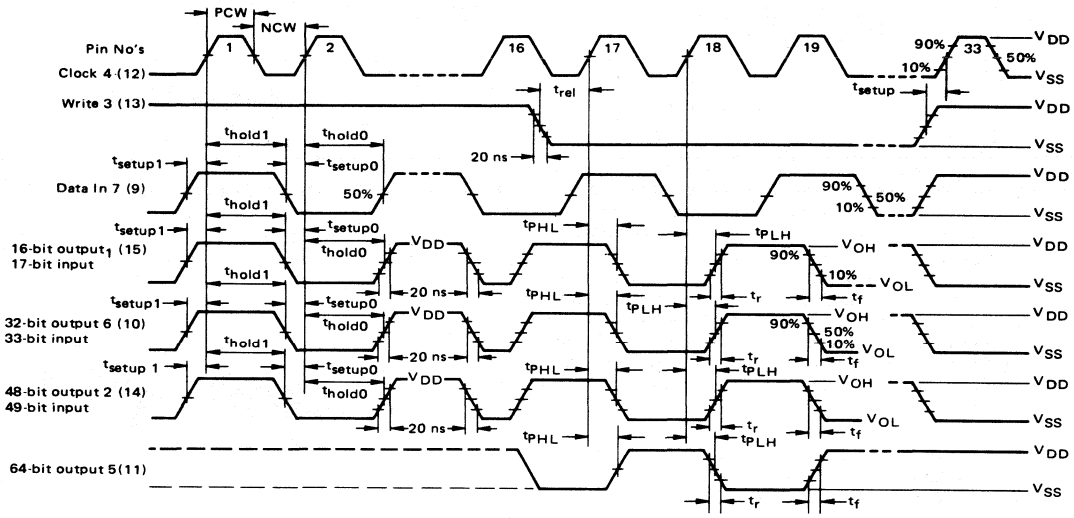
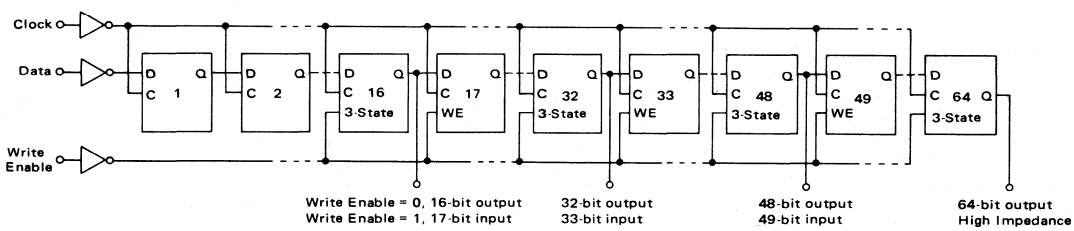
FIGURE 4 – AC TEST WAVEFORMS



EXPANDED BLOCK DIAGRAM
(1/2 OF DEVICE SHOWN)



MC14518AL
MC14518CL
MC14518CP
MC14520AL
MC14520CL
MC14520CP

DUAL UP COUNTERS

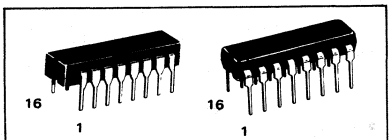
The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14518AL and MC14520AL)
  = 3.0 Vdc to 16 Vdc (MC14518CL,CP and MC14520CL,CP)
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design – Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL BCD UP COUNTER (MC14518)
DUAL BINARY UP COUNTER (MC14520)



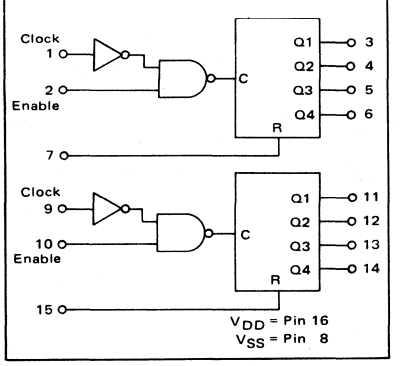
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14518AL/520AL —MC14518CL,CP/520CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range MC14518AL/520AL MC14518CL,CP/520CL,CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⌐¬	1	0	Increment Counter
0	¬⌐	0	Increment Counter
¬⌐	X	0	No Change
X	⌐¬	0	No Change
⌐¬	0	0	No Change
1	¬⌐	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14518AL/MC14520AL							MC14518CL,CP/MC14520CL,CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{out} = 2.5 Vdc) Source	1		5.0	-0.62	–	-0.5	-1.3	–	-0.35	–	-0.23	–	-0.2	-1.3	–	-0.16	–	
(V_{out} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{out} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{out} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.5	–	0.4	0.6	–	0.28	–	0.23	–	0.2	0.6	–	0.16	–	mAdc
(V_{out} = 0.5 Vdc)			10	1.1	–	0.9	1.6	–	0.65	–	0.6	–	0.5	1.6	–	0.4	–	
(V_{out} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	3,4	P_D	5.0	–	25	–	1.0	25	–	1500	–	250	–	1.0	250	–	3500	μW
			10	–	100	–	4.0	100	–	6000	–	1000	–	4.0	1000	–	14000	
Output Rise Time (C_L = 15 pF)	5,6	t_r	5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	ns
			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Output Fall Time (C_L = 15 pF)	5,6	t_f	5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	ns
			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
Clock Turn-On Delay Time (C_L = 15 pF)	7	t_{PHL}	5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	ns
			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
Clock Turn-Off Delay Time (C_L = 15 pF)	7	t_{PLH}	5.0	–	–	–	250	650	–	–	–	–	–	250	1000	–	–	ns
			10	–	–	–	100	225	–	–	–	–	–	100	300	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	–	PW_C	5.0	–	–	–	120	200	–	–	–	–	–	120	300	–	–	ns
			10	–	–	–	50	100	–	–	–	–	–	50	120	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)		PRF	5.0	–	–	1.5	2.5	–	–	–	–	–	1.0	2.5	–	–	–	MHz
			10	–	–	3.0	6.0	–	–	–	–	–	2.5	6.0	–	–	–	
Clock or Enable Rise and Fall Time (C_L = 15 pF, V_{DD} = 5.0 to 15 Vdc)	–	t_r,t_f	–	–	–	–	–	15	–	–	–	–	–	–	15	–	–	μs
Reset Turn-Off Delay Time (C_L = 15 pF)		t_{PHL}	5.0	–	–	–	300	650	–	–	–	–	–	300	1000	–	–	ns
			10	–	–	–	125	225	–	–	–	–	–	125	300	–	–	
Minimum Enable Pulse Width (C_L = 15 pF)	–	PW_E	5.0	–	–	–	260	440	–	–	–	–	–	260	660	–	–	ns
			10	–	–	–	110	220	–	–	–	–	–	110	260	–	–	
Minimum Reset Pulse Width (C_L = 15 pF)	–	PW_R	5.0	–	–	–	125	325	–	–	–	–	–	100	500	–	–	ns
			10	–	–	–	50	100	–	–	–	–	–	50	125	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

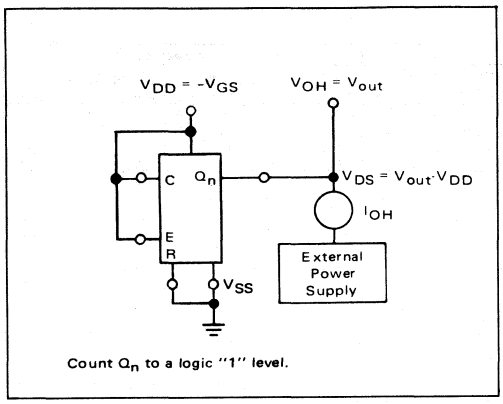
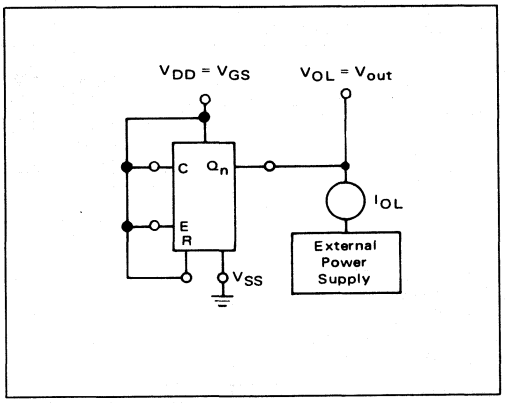
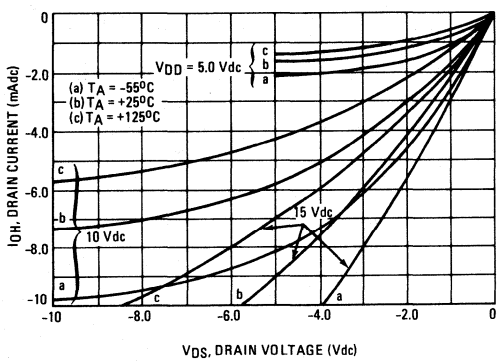


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT





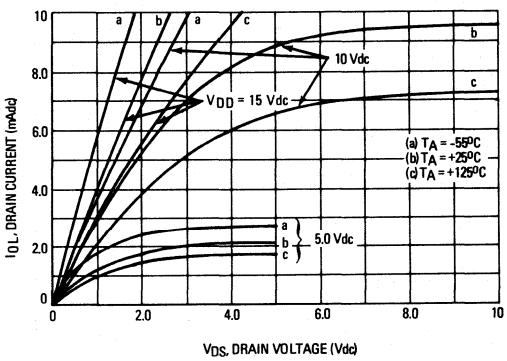


FIGURE 3 – TYPICAL POWER DISSIPATION CHARACTERISTICS

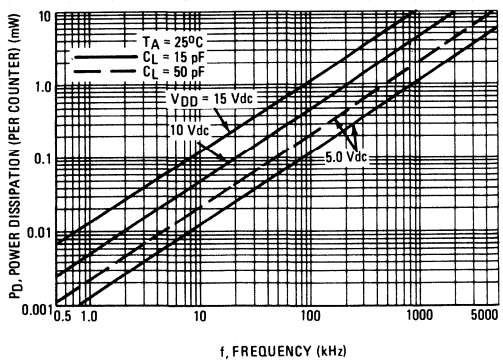


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

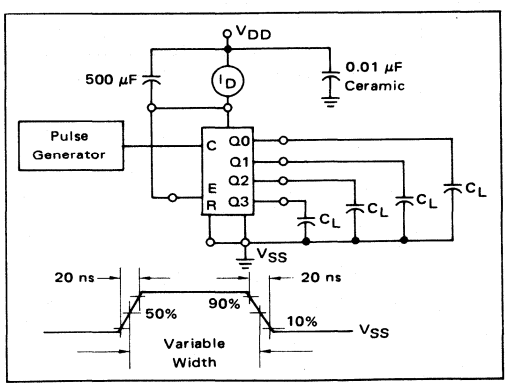


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FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

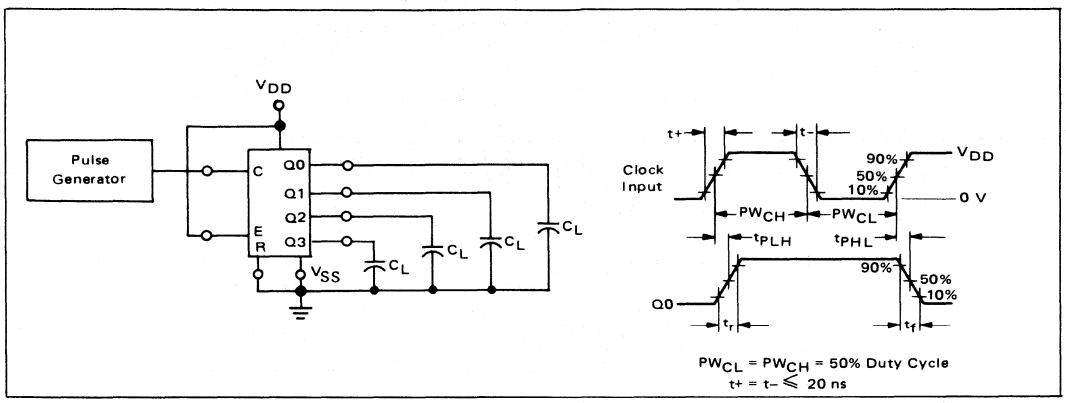

FIGURE 6 – TYPICAL RISE AND FALL TIME versus LOAD CAPACITANCE

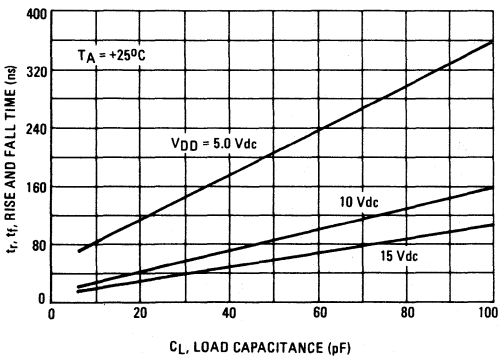

FIGURE 7 – TYPICAL TURN-ON AND TURN-OFF DELAY TIME versus LOAD CAPACITANCE

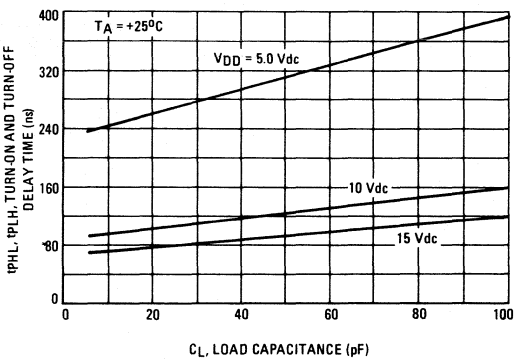

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FIGURE 8 – TIMING DIAGRAM

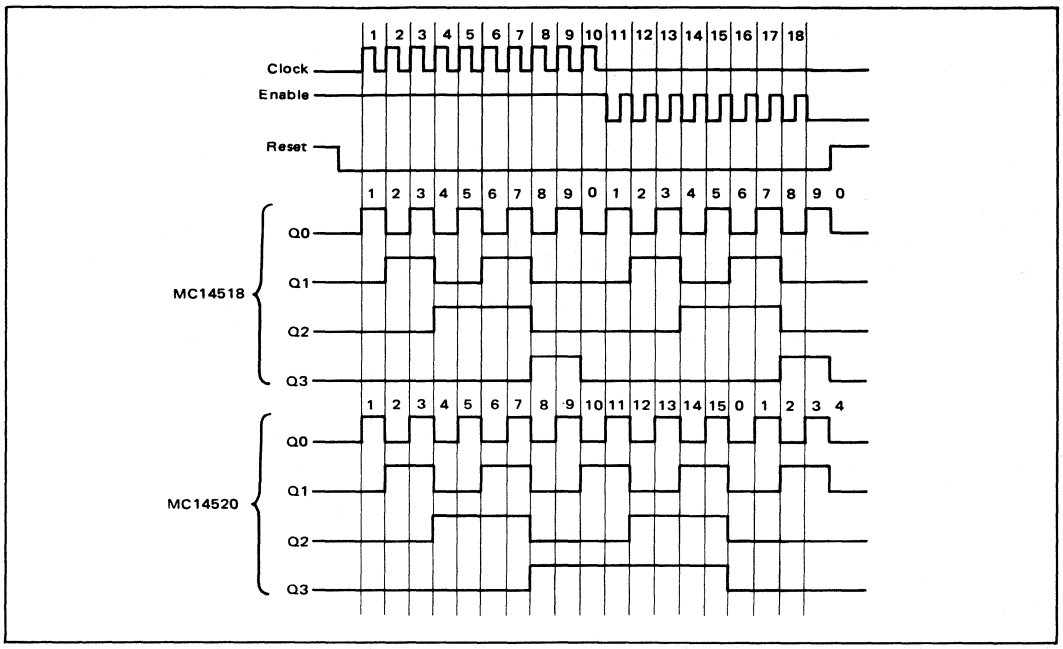


FIGURE 9 – DECADE COUNTER (MC14518) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)

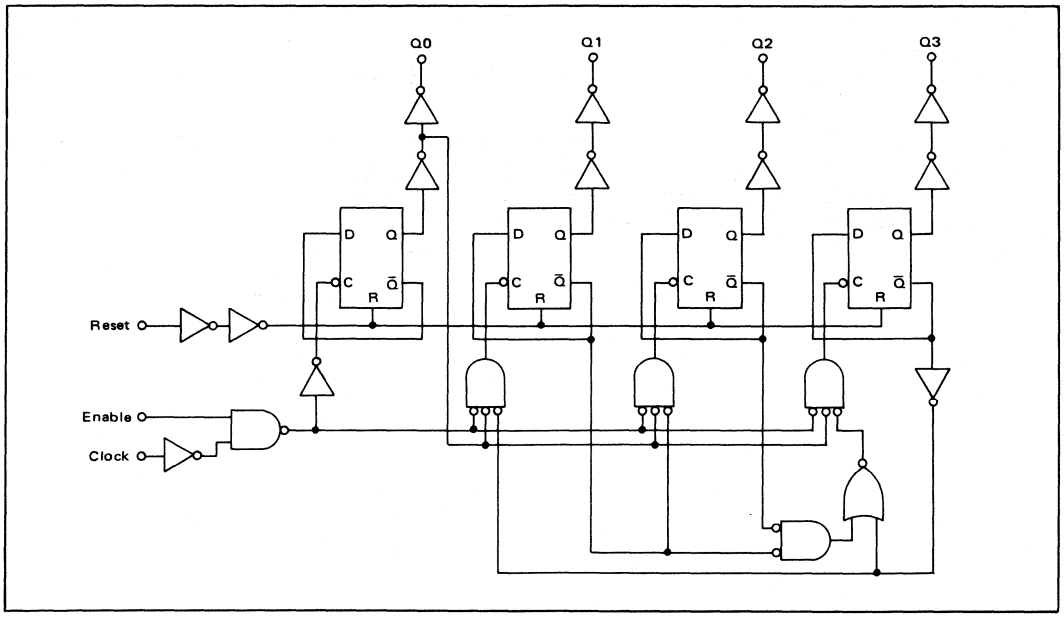
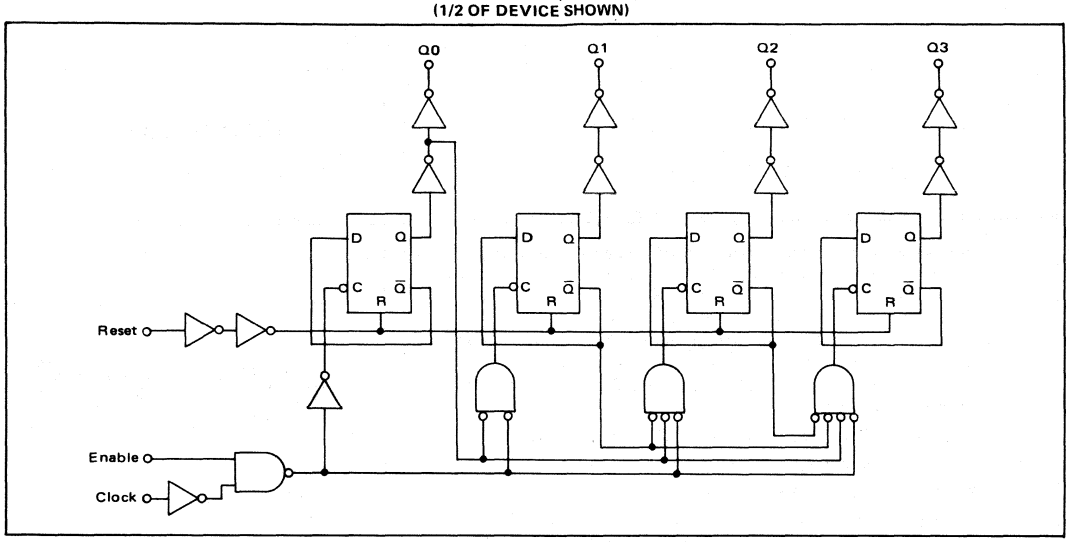


FIGURE 10 – BINARY COUNTER (MC14520) LOGIC DIAGRAM
(1/2 OF DEVICE SHOWN)



MC14519AL
MC14519CL
MC14519CP

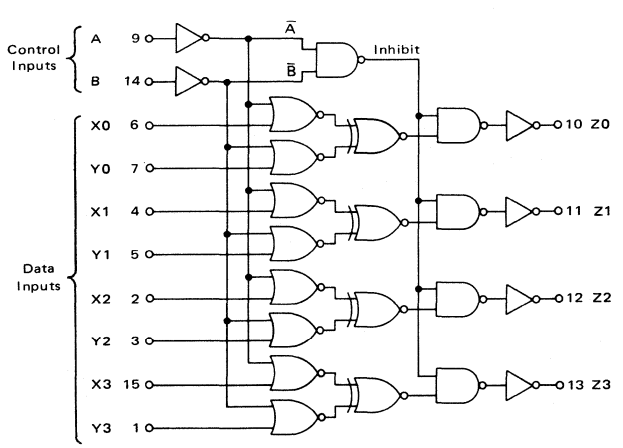
4-BIT AND/OR SELECTOR
or
QUAD 2-CHANNEL DATA SELECTOR
or
QUAD EXCLUSIVE "NOR" GATE

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package; a **4-Bit AND/OR Selector,** a **Quad 2-Channel Data Selector,** or a **Quad Exclusive NOR Gate.**

- Quiescent Power Dissipation = 100 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14519AL)
  3.0 Vdc to 16 Vdc (MC14519CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications

LOGIC DIAGRAM
(Positive Logic)



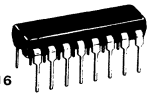
V_{DD} = Pin 16
V_{SS} = Pin 8

McMOS

(LOW-POWER COMPLEMENTARY MOS)

4-BIT AND/OR SELECTOR

L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

TRUTH TABLE

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \circledcirc Y_n$

Note:
$X_n \circledcirc Y_n$ means X_n (Exclusive-NOR) Y_n

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See Mechanical Data Section for package dimensions.

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14519AL —MC14519CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14519AL —MC14519CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14519AL -55°C Min	MC14519AL -55°C Max	MC14519AL +25°C Min	MC14519AL +25°C Typ	MC14519AL +25°C Max	MC14519AL +125°C Min	MC14519AL +125°C Max	MC14519CL/CP -40°C Min	MC14519CL/CP -40°C Max	MC14519CL/CP +25°C Min	MC14519CL/CP +25°C Typ	MC14519CL/CP +25°C Max	MC14519CL/CP +85°C Min	MC14519CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	–	P_Q																mW
(C_L = 15 pF, f = 0 Hz)			5.0	–	0.0025	–	0.00005	0.0025	–	0.15	–	0.025	–	0.00005	0.025	–	0.75	
			10	–	0.01	–	0.0001	0.01	–	0.6	–	0.1	–	0.0001	0.1	–	3.0	
			15	–	–	–	0.0003	–	–	–	–	–	–	0.0003	–	–	–	
Dynamic Power Dissipation †	1	P_D																mW
(C_L = 15 pF)			5.0	P_D = (2.5 mW/MHz) f + 0.00005 mW														
			10	P_D = (10 mW/MHz) f + 0.0001 mW														
			15	P_D = (23 mW/MHz) f + 0.0003 mW														
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L +12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On, Turn-Off Delay Time	2	t_{PHL}, t_{PLH}																ns
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 172 ns			5.0	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 74 ns			10	–	–	–	85	135	–	–	–	–	–	85	175	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 62 ns			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refer to corresponding formula:

$$P_T(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

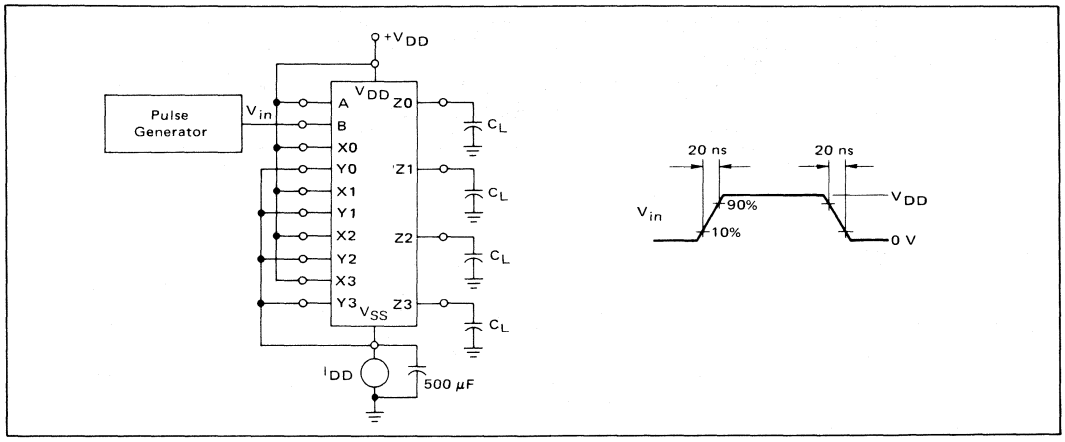
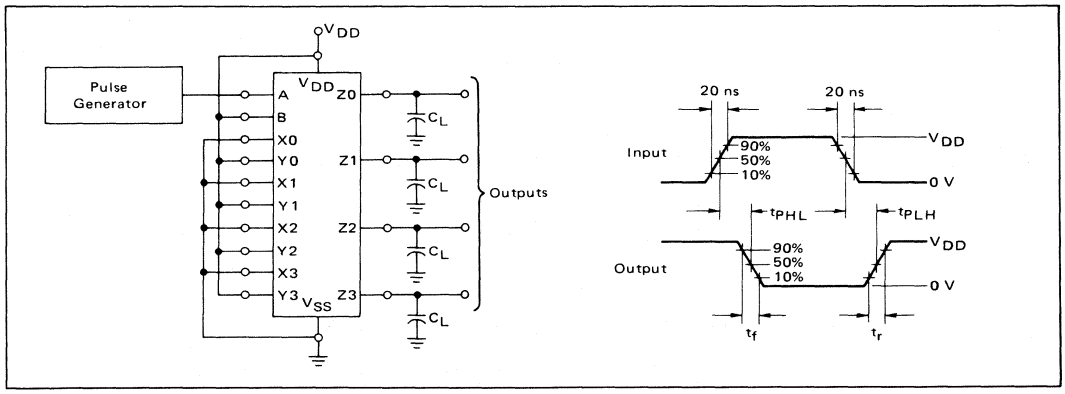
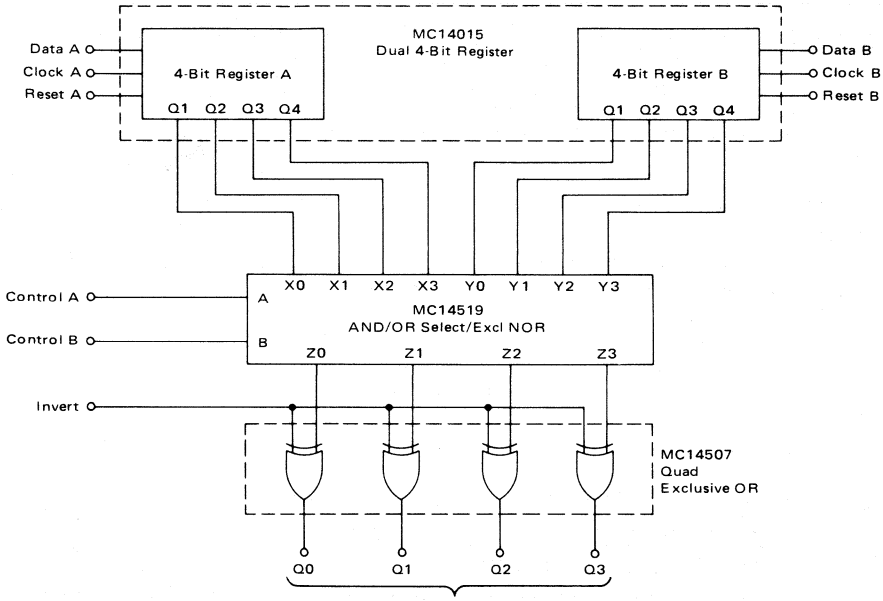


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TYPICAL CIRCUIT APPLICATIONS

DATA REGISTER SELECTION COMPARISON



CONVERSION TABLE

OPERATION CODE			OUTPUT				FUNCTION
A	B	INV	Q0	Q1	Q2	Q3	
0	0	0	0	0	0	0	Inhibit, all zeros
0	0	1	1	1	1	1	Inhibit, all ones
1	0	0	X0	X1	X2	X3	Control A
1	0	1	$\overline{X0}$	$\overline{X1}$	$\overline{X2}$	$\overline{X3}$	Control A and Invert
0	1	0	Y0	Y1	Y2	Y3	Control B
0	1	1	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	Control B and Invert
1	1	0	X0 ⊙ Y0	X1 ⊙ Y1	X2 ⊙ Y2	X3 ⊙ Y3	Exclusive NOR
1	1	1	X0 ⊕ Y0	X1 ⊕ Y1	X2 ⊕ Y2	X3 ⊕ Y3	Exclusive OR

MC14521AL
MC14521CL
MC14521CP

FREQUENCY DIVIDER

Advance Information

24-STAGE FREQUENCY DIVIDER

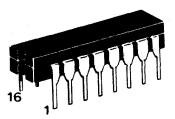
The MC14521 consists of a chain of 24 flip-flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently this part will count up to 2^{24} = 16,777,216. The count advances on the negative going edge of the clock. The outputs of the last seven-stages are available for added flexibility.

- $f_{(max)}$ = 9.0 MHz typical @ V_{DD} = 10 V
- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- V_{DD}' and V_{SS}' Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low-Power Operation

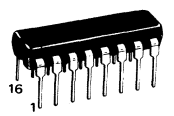
McMOS

(LOW-POWER COMPLEMENTARY MOS)

24-STAGE FREQUENCY DIVIDER

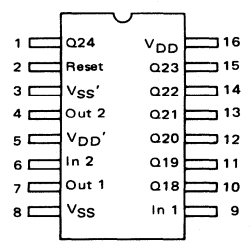


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

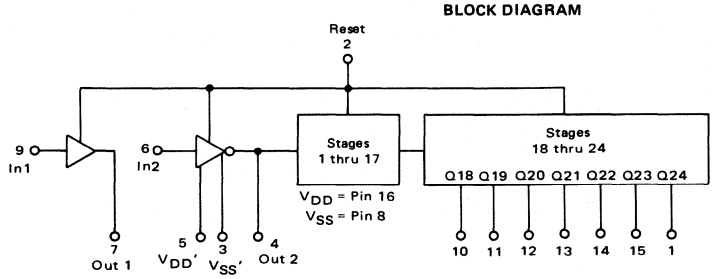
PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14521AL — MC14521CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14521AL — MC14521CL/CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



OUTPUT	COUNT CAPACITY
Q18	2^{18} = 262,144
Q19	2^{19} = 524,288
Q20	2^{20} = 1,048,576
Q21	2^{21} = 2.097,152
Q22	2^{22} = 4,194,304
Q23	2^{23} = 8,388,608
Q24	2^{24} = 16,777,216

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

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ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14521AL							MC14521CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source		I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation** (C_L = 15 pF)	1	P_D																mW
P_D = (1.2 mW/MHz) f + 0.0001 mW			5.0	–	0.025	–	0.0001	0.025	–	1.5	–	0.25	–	0.0001	0.25	–	3.5	
P_D = (5.0 mW/MHz) f + 0.0004 mW			10	–	0.10	–	0.0004	0.10	–	6.0	–	1.0	–	0.0004	1.0	–	14	
P_D = (13.0 mW/MHz) f + 0.001 mW			15	–	–	–	0.001	–	–	–	–	–	–	0.001	–	–	–	
Output Rise Time** (C_L = 15 pF)	2	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time** (C_L = 15 pF)	2	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On, Turn-Off Delay Time** (C_L = 15 pF) Clock to Q18	2	t_{PHL}, t_{PLH}																µs
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 4474 ns			5.0	–	–	–	4.5	9.0	–	–	–	–	–	4.5	13.5	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 1690 ns			10	–	–	–	1.7	3.5	–	–	–	–	–	1.7	5.2	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 1192 ns			15	–	–	–	1.2	–	–	–	–	–	–	1.2	–	–	–	
Turn-On, Turn-Off Delay Time** (C_L = 15 pF) Clock to Q24	2	t_{PHL}, t_{PLH}																µs
t_{PHL}, t_{PLH} = (1.75 ns/pF) C_L + 5974 ns			5.0	–	–	–	6.0	12	–	–	–	–	–	6.0	18	–	–	
t_{PHL}, t_{PLH} = (0.70 ns/pF) C_L + 2190 ns			10	–	–	–	2.2	4.5	–	–	–	–	–	2.2	6.5	–	–	
t_{PHL}, t_{PLH} = (0.53 ns/pF) C_L + 1442 ns			15	–	–	–	1.5	–	–	–	–	–	–	1.5	–	–	–	
Turn-On Delay Time** (C_L = 15 pF) Reset to Q_n	2	t_{PHL}																ns
t_{PHL} = (1.75 ns/pF) C_L + 1274 ns			5.0	–	–	–	1300	2600	–	–	–	–	–	1300	4000	–	–	
t_{PHL} = (0.70 ns/pF) C_L + 490 ns			10	–	–	–	500	1000	–	–	–	–	–	500	1500	–	–	
t_{PHL} = (0.53 ns/pF) C_L + 342 ns			15	–	–	–	350	–	–	–	–	–	–	350	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	2	PW_c																ns
			5.0	–	–	–	140	250	–	–	–	–	–	140	385	–	–	
			10	–	–	–	55	100	–	–	–	–	–	55	150	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)		PRF																MHz
			5.0	–	–	2.0	3.5	–	–	–	–	–	1.5	3.5	–	–	–	
			10	–	–	5.0	9.0	–	–	–	–	–	3.5	9.0	–	–	–	
			15	–	–	–	12	–	–	–	–	–	–	12	–	–	–	
Maximum Clock Rise and Fall Time (C_L = 15 pF)		t_r, t_f																µs
			5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
			15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Minimum Reset Pulse Width (C_L = 15 pF)		PW_R																ns
			5.0	–	–	–	700	1400	–	–	–	–	–	700	1800	–	–	
			10	–	–	–	300	600	–	–	–	–	–	300	900	–	–	
			15	–	–	–	200	–	–	–	–	–	–	200	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

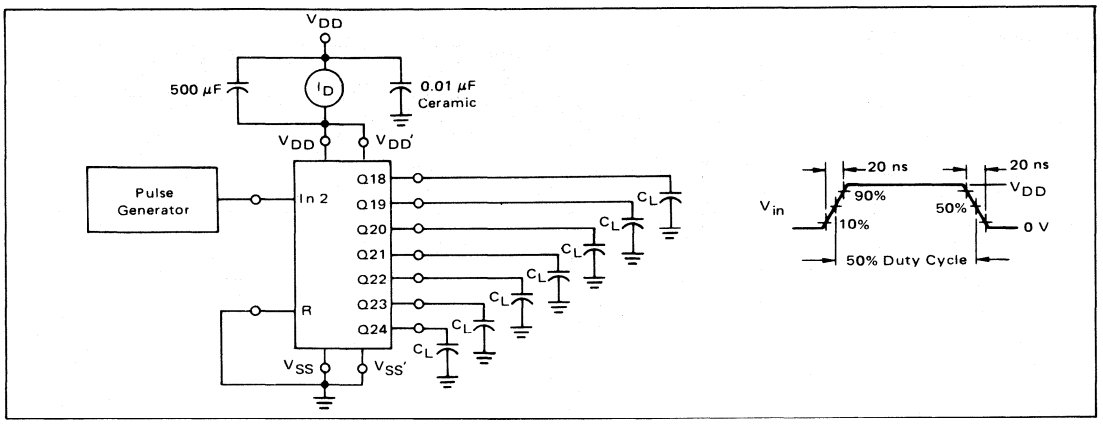


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

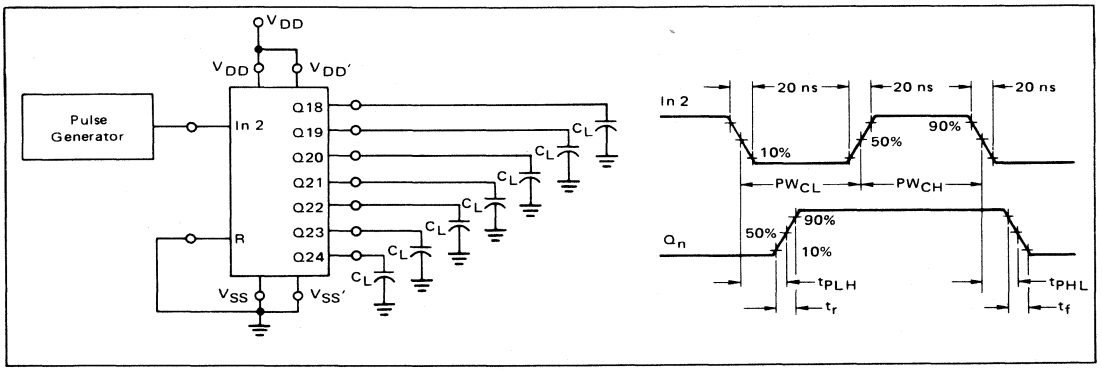
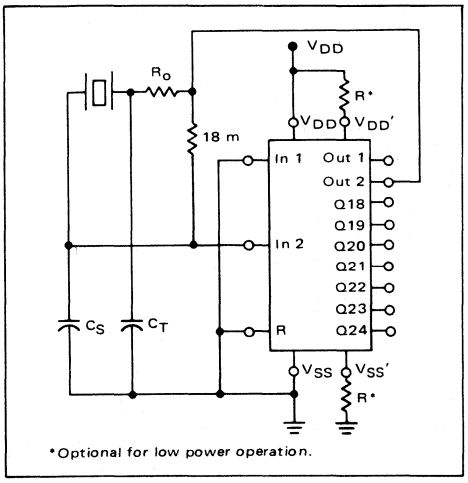


FIGURE 3 – CRYSTAL OSCILLATOR CIRCUIT



*Optional for low power operation.

FIGURE 4 – TYPICAL DATA FOR CRYSTAL OSCILLATOR CIRCUIT

CHARACTERISTIC	500 kHz CIRCUIT	50 kHz CIRCUIT	UNIT
Crystal Characteristics			
Resonant Frequency	500	50	kHz
Cut	S	N	–
Equivalent Resistance, R_S	1.0	6.2	kΩ
External Resistor/Capacitor Values			
R_o	47	750	kΩ
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Change as a Function of V_{DD} (T_A = 25°C)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature (V_{DD} = 10 V)			
T_A Change from -55°C to +25°C			
MC14521 only	-4.0	-2.0	ppm
Complete Oscillator*	+100	+120	ppm
T_A Change from +25°C to +125°C			
MC14521 only	-2.0	-2.0	ppm
Complete Oscillator*	-160	-560	ppm

*Complete oscillator includes crystal, capacitors, and resistors.

FIGURE 5 – RC OSCILLATOR STABILITY

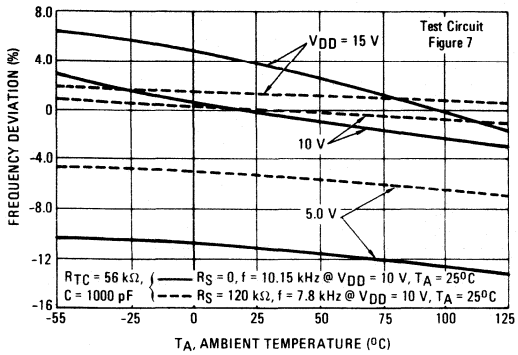


FIGURE 6 – RC OSCILLATOR FREQUENCY AS A FUNCTION OF R_{TC} AND C

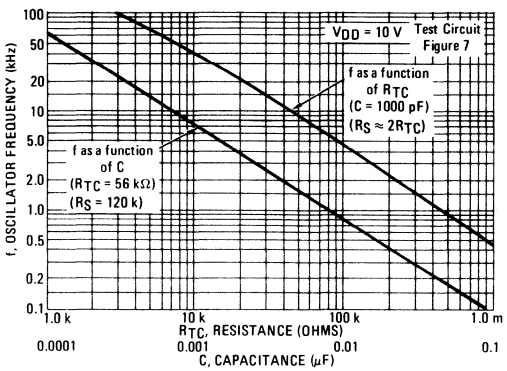


FIGURE 7 – RC OSCILLATOR CIRCUIT

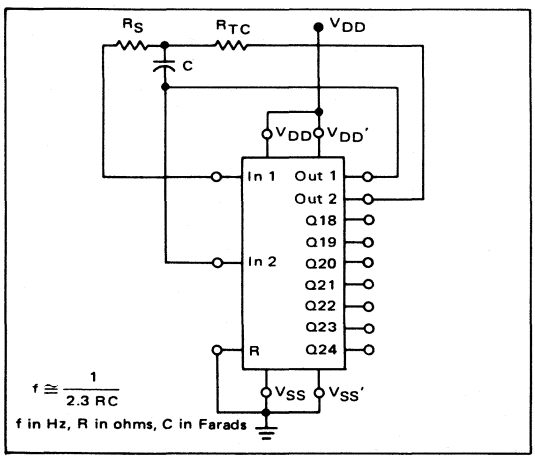
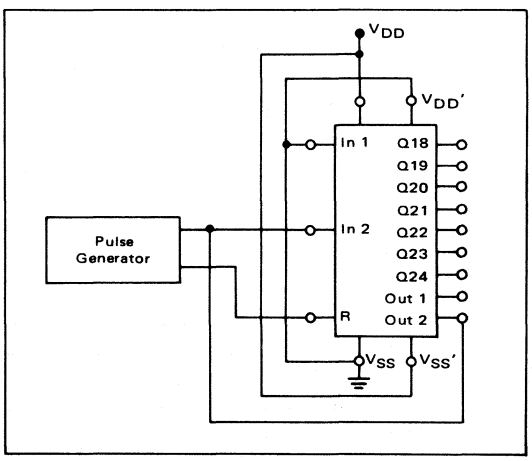


FIGURE 8 – FUNCTIONAL TEST CIRCUIT

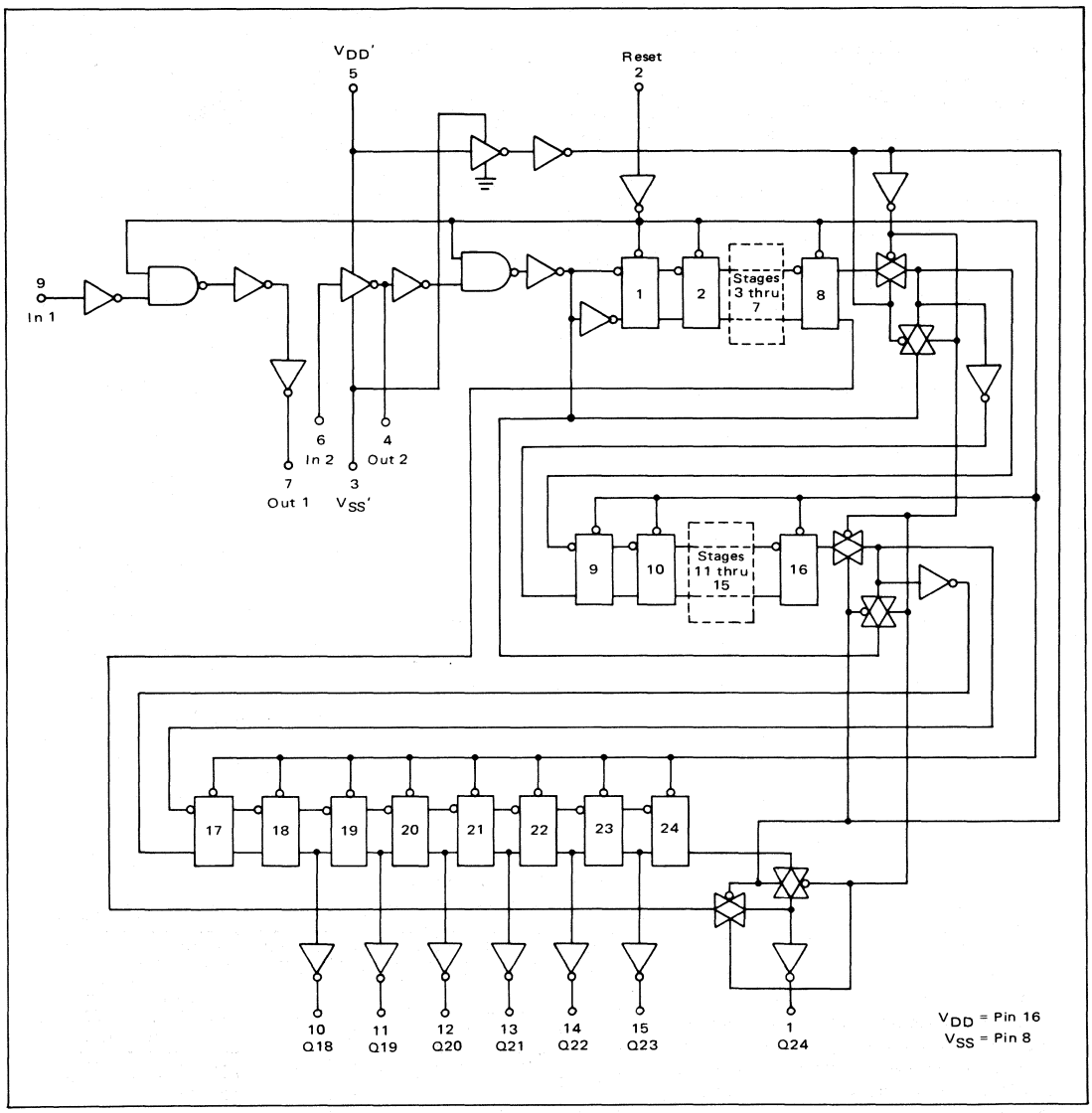


FUNCTIONAL TEST SEQUENCE

A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections, and 255 counts are loaded in each of the 8-stage sections in parallel. All flip-flops are now at a logic "1". The counter is now returned to the normal 24-stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all "1" state to an all "0" state.

INPUTS		OUTPUTS				COMMENTS
Reset	In 2	Out 2	V_{SS}'	V_{DD}'	Q18 thru Q24	
1	0	0	V_{DD}	Gnd	0	Counter is in three 8-stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together
0	1	1				First "0" to "1" transition on In 2, Out 2 node.
	0 1 – – –	0 1 – – –				255 "0" to "1" transitions are clocked into this In 2, Out 2 node.
	1	1			1	The 255th "0" to "1" transition.
	0 0	0 0	Gnd		1 1	
	1	0		V_{DD}	1	Counter converted back to 24-stages in series mode.
	1				1	Out 2 converts back to an output.
	0				0	Counter ripples from an all "1" state to an all "0" stage.

LOGIC DIAGRAM



MC14522AL
MC14522CL
MC14522CP
MC14526AL
MC14526CL
MC14526CP

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

The MC14522 BCD counter and the MC14526 binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure.

These devices are programmable, cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications the "0" output is applied to the Preset Enable input. The Cascade Feedback input allows cascade divide-by-N operation with no additional gates required. The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

These complementary MOS counters can be used in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

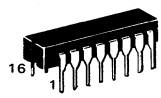
- Quiescent Power Dissipation = 1.0 μW/package typical
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (AL Version)
  = 3.0 Vdc to 16 Vdc (CL, CP Version)
- Internally Synchronous for High Internal and External Speeds.
- Logic Edge-Clocked Design — Incremented on Positive Transition of Clock or Negative Transition of Clock Inhibit
- 5.0 MHz Counting Rate

McMOS

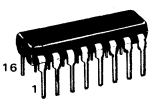
(LOW-POWER COMPLEMENTARY MOS)

PROGRAMMABLE DIVIDE-BY-N 4-BIT COUNTERS

BCD — MC14522AL/CL/CP
Binary — MC14526AL/CL/CP



L SUFFIX
CERAMIC PACKAGE
CASE 620

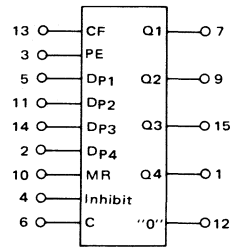


P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — AL Version — CL, CP Version	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Version — CL, CP Version	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

TRUTH TABLES

MC14522

COUNT	OUTPUT Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

MC14526

COUNT	OUTPUT Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14522AL/MC14526AL							MC14522CL/CP/MC14526CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	0.05	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc)	Source	1	5.0	-0.62	–	-0.5	-1.1	–	-0.35	–	-0.23	–	-0.2	-1.1	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.75	–	-0.35	–	-0.23	–	-0.2	-0.75	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-2.9	–	–	–	–	–	–	-2.9	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}															mAdc
(V_{OL} = 0.5 Vdc)			5.0	0.5	–	0.4	0.9	–	0.28	–	0.23	–	0.2	0.9	–	0.16	–	
(V_{OL} = 1.5 Vdc)			10	1.1	–	0.9	2.0	–	0.65	–	0.6	–	0.5	2.0	–	0.4	–	
			15	–	–	–	8.0	–	–	–	–	–	–	8.0	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	3,4	P_D	5.0	–	25	–	0.5	25	–	1500	–	250	–	0.5	250	–	3500	μW
			10	–	100	–	1.0	100	–	6000	–	1000	–	1.0	1000	–	14000	
Output Rise Time (C_L = 15 pF)**	5,6	t_r																ns
t_r = (6.3 ns/pF) C_L + 5.0 ns			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
t_r = (2.25 ns/pF) C_L + 15 ns			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
t_r = (2.22 ns/pF) C_L + 2.0 ns			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	

(Continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14522AL/MC14526AL							MC14522CL/CP/MC14526CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Fall Time (C_L = 15 pF)	5,6	t_f																ns
t_f = (2.84 ns/pF) C_L + 58 ns			5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
t_f = (1.03 ns/pF) C_L + 35 ns			10	–	–	–	50	125	–	–	–	–	–	50	150	–	–	
t_f = (1.00 ns/pF) C_L + 20 ns			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Turn-Off Delay Time	5,6	t_{PLH}																ns
"0" Output (C_L = 30 pF)			5.0	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
			10	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
Q Outputs (C_L = 15 pF)**																		
t_{PLH} = (3.02 ns/pF) C_L + 455 ns			5.0	–	–	–	500	750	–	–	–	–	–	500	1000	–	–	ns
t_{PLH} = (1.13 ns/pF) C_L + 183 ns			10	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
t_{PLH} = (1.0 ns/pF) C_L + 115 ns			15	–	–	–	130	–	–	–	–	–	–	130	–	–	–	
Turn-On Delay Time	5,6	t_{PHL}																ns
"0" Output (C_L = 30 pF)			5.0	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
			10	–	–	–	100	250	–	–	–	–	–	100	300	–	–	
Q Outputs (C_L = 15 pF)**																		
t_{PHL} = (1.58 ns/pF) C_L + 476 ns			5.0	–	–	–	500	750	–	–	–	–	–	500	1000	–	–	ns
t_{PHL} = (0.67 ns/pF) C_L + 190 ns			10	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
t_{PHL} = (0.50 ns/pF) C_L + 133 ns			15	–	–	–	140	–	–	–	–	–	–	140	–	–	–	
Minimum Clock Pulse Width	5,6	PW_C	5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	ns
			10	–	–	–	50	100	–	–	–	–	–	50	150	–	–	
Maximum Clock Pulse Frequency	5,6	PRF	5.0	–	–	1.5	2.0	–	–	–	–	–	1.0	2.0	–	–	–	MHz
(C_L = 15 pF)			10	–	–	3.0	5.0	–	–	–	–	–	2.5	5.0	–	–	–	
Clock or Inhibit Rise and Fall Time	5,6	t_r,t_f	5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	μs
(C_L = 15 pF)			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
Hold Time (C_L = 15 pF)	5,6	t_{hold}	5.0	–	–	–	75	125	–	–	–	–	–	75	150	–	–	ns
			10	–	–	–	25	50	–	–	–	–	–	25	75	–	–	
Minimum Preset Enable Pulse Width	5,6	PW_{PE}	5.0	–	–	–	100	250	–	–	–	–	–	100	300	–	–	ns
			10	–	–	–	50	100	–	–	–	–	–	50	150	–	–	
Minimum Master Reset Pulse Width	5,6	PW_{MR}	5.0	–	–	–	200	300	–	–	–	–	–	200	350	–	–	ns
			10	–	–	–	100	250	–	–	–	–	–	100	300	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS TEST CIRCUIT

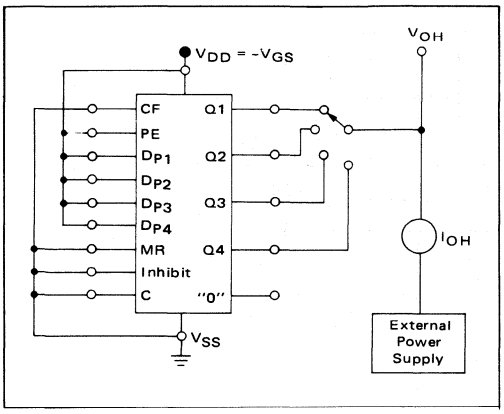


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS TEST CIRCUIT

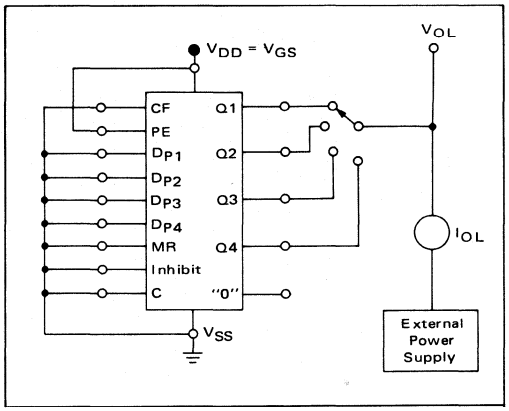


FIGURE 3 – TYPICAL POWER DISSIPATION CHARACTERISTICS

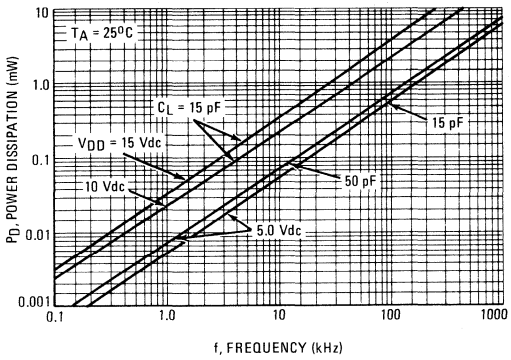


FIGURE 4 – POWER DISSIPATION

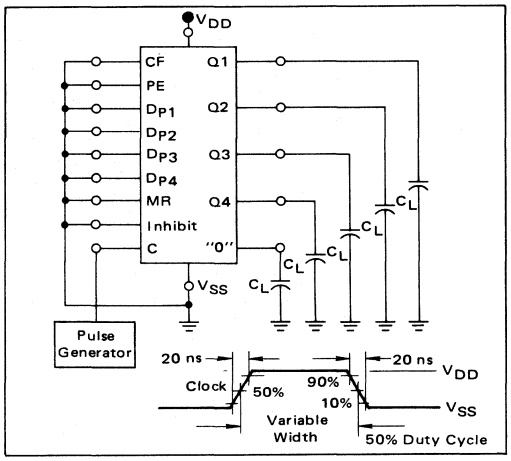


FIGURE 5 – AC TEST CIRCUITS

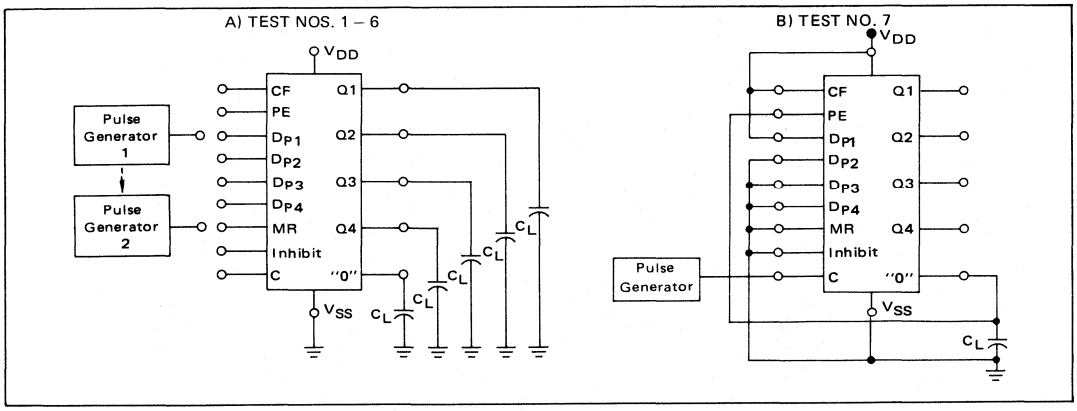
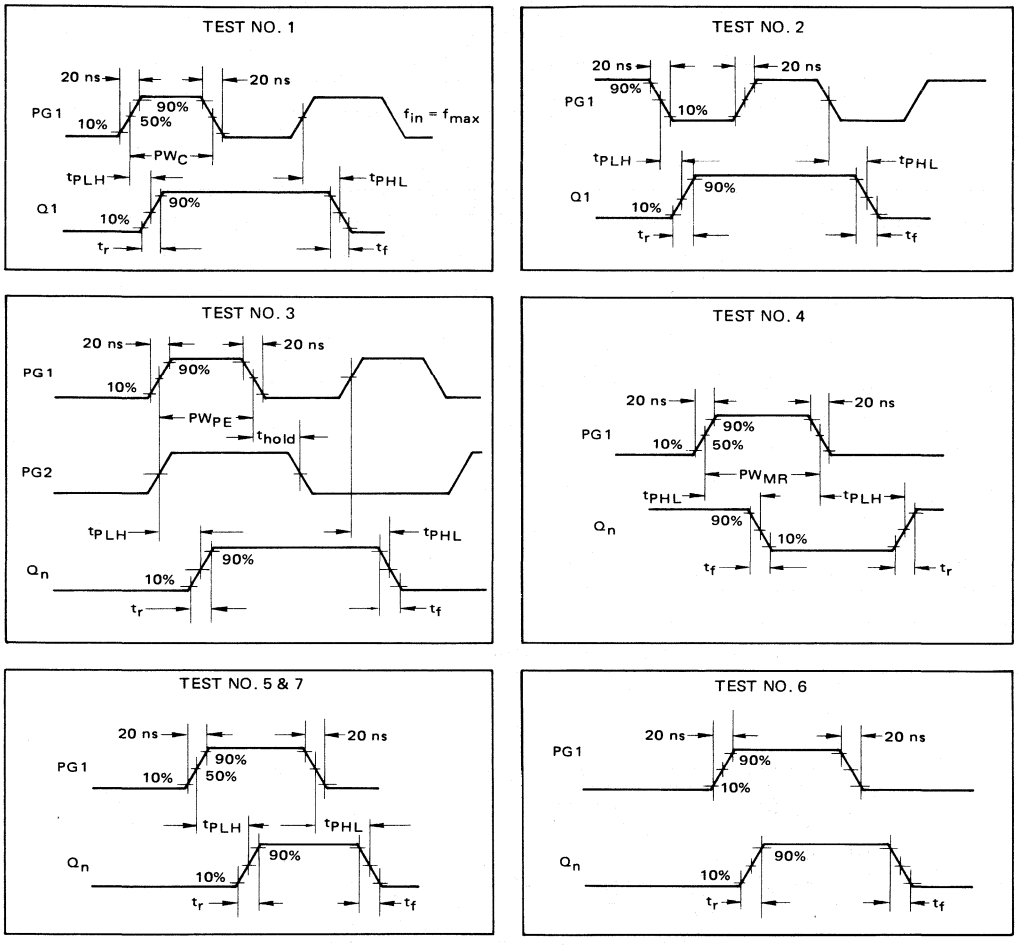


FIGURE 6 – AC TEST CONNECTIONS AND WAVEFORMS



CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	D_{Pn}	CF	OUTPUT
$t_r, t_f, t_{PLH}, t_{PHL}$	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{Max}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{hold}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	Fig 5B	V_{SS}	Fig 5B	V_{DD}	"0"

7

FIGURE 7 – MC14522 LOGIC DIAGRAM (BCD Divide-by-N Counter)

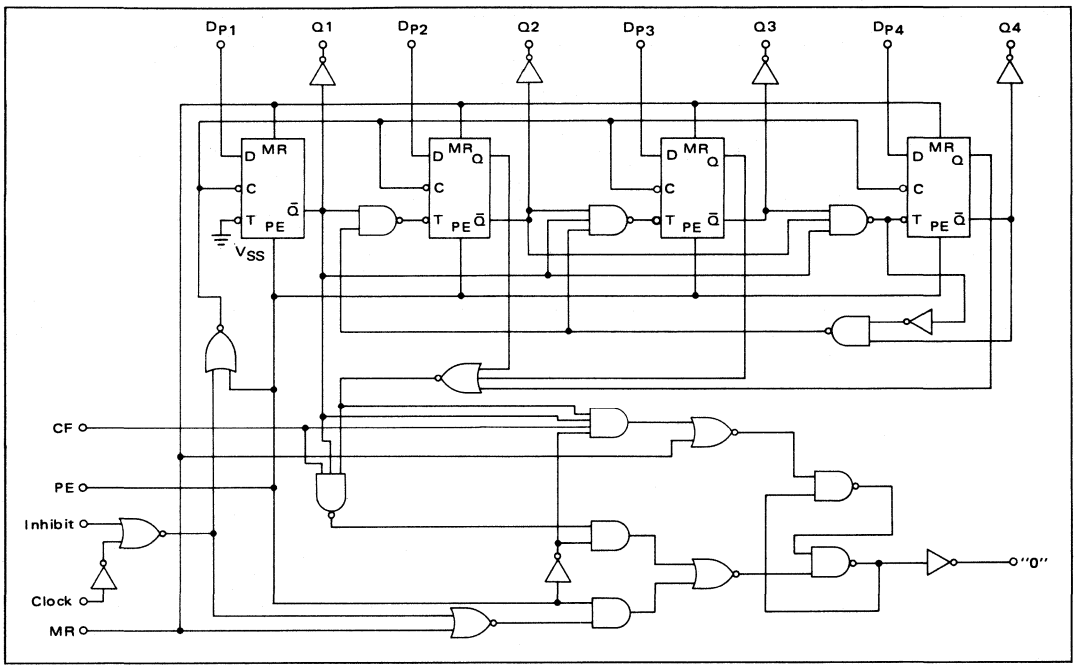
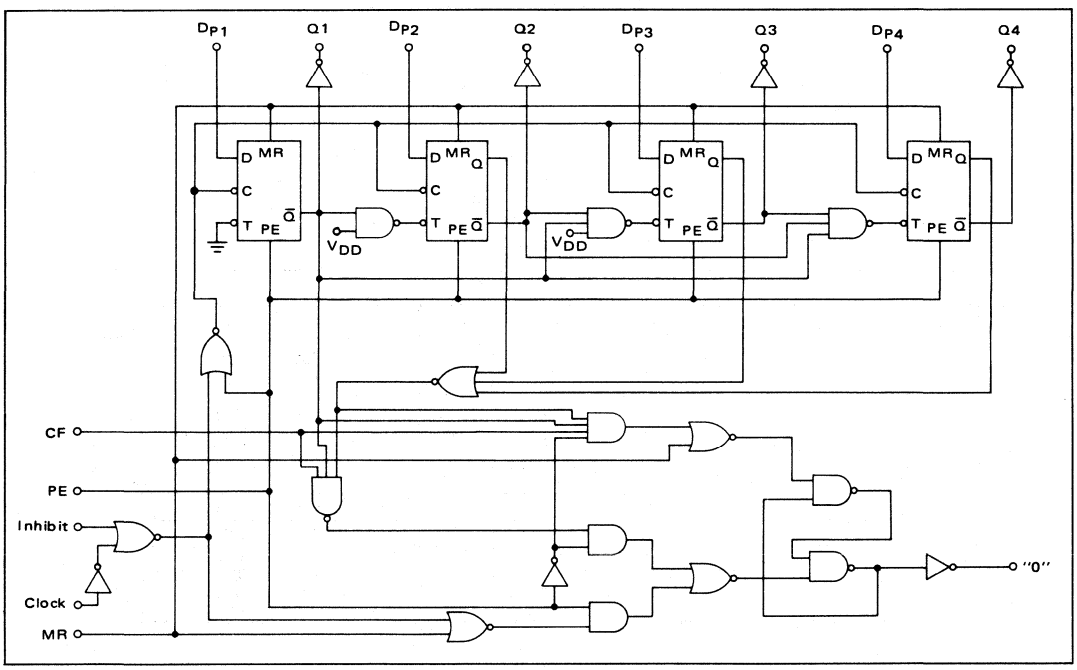


FIGURE 8 – MC14526 LOGIC DIAGRAM (Binary Divide-by-N Counter)



7

APPLICATIONS INFORMATION

As a cascadable down counter, these devices feature asynchronous preset and master reset capability. Figure 9 shows a three-stage presettable down counter whose Q outputs respond synchronously to negative transitions on the clock inhibit inputs.

The three-stage frequency divider of Figure 10 will provide an output pulse approximately equal to the clock pulse width, for N input pulses where N is any BCD input from 1-999 for the MC14522, or any binary input from 1-4095 for the MC14526. The master reset input allows synchronous initiation of a divide-by-N cycle. A pulse counting inhibit may be implemented with the inhibit input.

FIGURE 9 – SYNCHRONOUS PROGRAMMABLE DOWN COUNTER

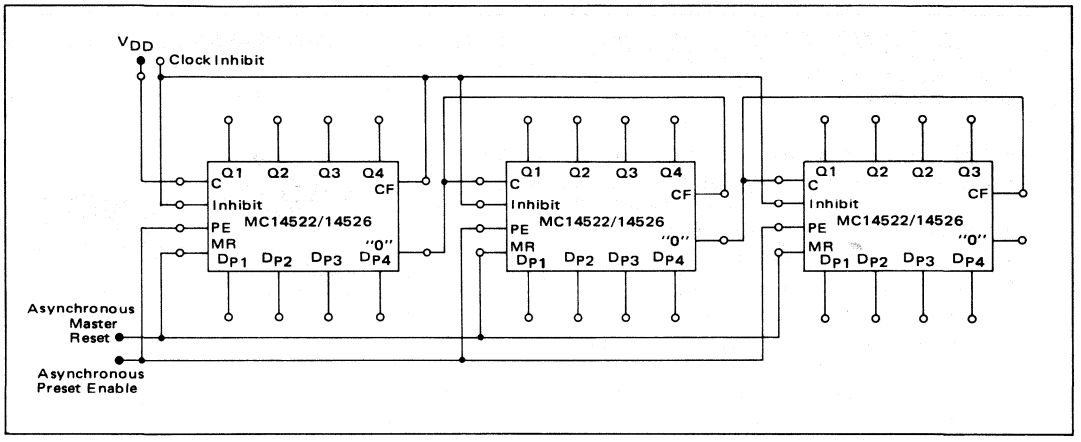
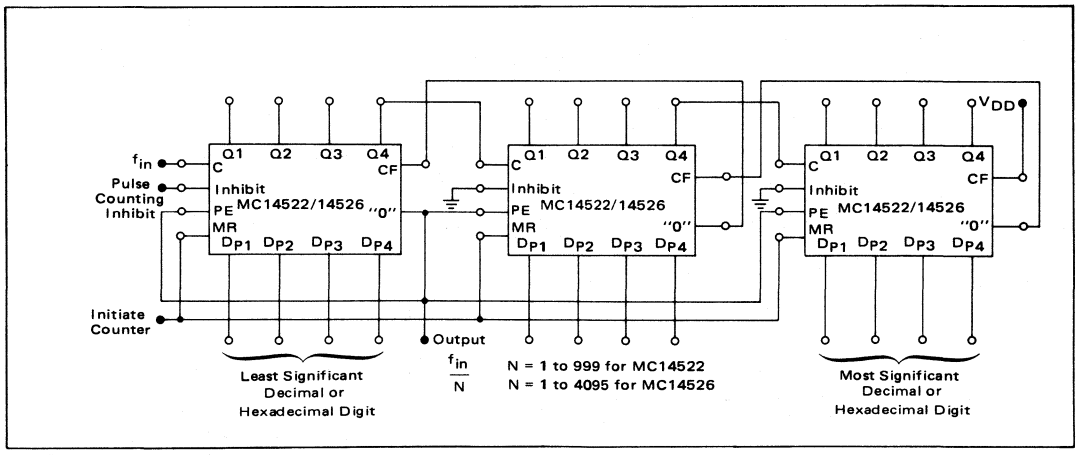


FIGURE 10 – 3-STAGE PROGRAMMABLE FREQUENCY DIVIDER



MC14527AL
MC14527CL
MC14527CP

BCD RATE MULTIPLIER

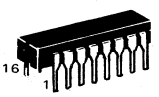
The MC14527 BCD rate multiplier (DRM) provides an output pulse rate based upon the BCD input number. For example, if 6 is the BCD input number, there will be six output pulses for every ten input pulses. This part may be used to add, subtract, divide, raise to power, and solve algebraic and differential equations, and can be used to generate trigonometric functions and natural logarithms. Typical applications include digital filters, motor speed control and frequency synthesizers.

- Quiescent Power Dissipation = 0.25 μW/package typical @ 5.0 Vdc
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14527AL)
  = 3.0 Vdc to 16 Vdc (MC14527CL/CP)
- Low Input Capacitance – 5.0 pF typical
- Internally Synchronous for High Speed
- Output Clocked on the Negative Going Edge of Clock
- Strobe for Inhibiting or Enabling Outputs
- Enable and Cascade Inputs for Cascade Operation of Two or More DRMs
- "9" Output for the Parallel Enable Configuration and DRMs in Cascade
- Complementary Outputs
- Clear and Set to Nine Inputs

McMOS

(LOW-POWER COMPLEMENTARY MOS)

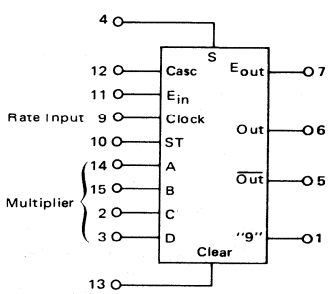
BCD RATE MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14527AL MC14527CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	MC14527AL MC14527CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS									OUTPUT LOGIC LEVEL NUMBER OF PULSES			
D	C	B	A	No. of Clock Pulses	E_{in}	STROBE	CASCADE	CLEAR	SET	OUT	OUT	E_{out}	"9"
0	0	0	0	10	0	0	0	0	0	0	1	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	1	0	0	10	0	0	0	0	0	3	3	1	1
0	1	0	1	10	0	0	0	0	0	4	4	1	1
0	1	1	0	10	0	0	0	0	0	5	5	1	1
0	1	1	1	10	0	0	0	0	0	6	6	1	1
1	0	0	0	10	0	0	0	0	0	7	7	1	1
1	0	0	1	10	0	0	0	0	0	8	8	1	1
1	0	1	0	10	0	0	0	0	0	9	9	1	1
1	0	1	1	10	0	0	0	0	0	8	8	1	1
1	1	0	0	10	0	0	0	0	0	9	9	1	1
1	1	0	1	10	0	0	0	0	0	8	8	1	1
1	1	1	0	10	0	0	0	0	0	9	9	1	1
1	1	1	1	10	0	0	0	0	0	–	–	–	–
X	X	X	X	10	0	1	0	0	0	0	1	1	1
X	X	X	X	10	0	0	1	0	0	1	0	1	1
1	X	X	X	10	0	0	0	1	0	10	10	1	0
0	X	X	X	10	0	0	0	1	0	0	1	1	0
X	X	X	X	10	0	0	0	0	1	0	1	0	1

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14527AL -55°C Min	MC14527AL -55°C Max	MC14527AL +25°C Min	MC14527AL +25°C Typ	MC14527AL +25°C Max	MC14527AL +125°C Min	MC14527AL +125°C Max	MC14527CL/CP -40°C Min	MC14527CL/CP -40°C Max	MC14527CL/CP +25°C Min	MC14527CL/CP +25°C Typ	MC14527CL/CP +25°C Max	MC14527CL/CP +85°C Min	MC14527CL/CP +85°C Max	Unit
Output Level "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}																Vdc
($V_{out} \leq 3.0$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 4.5$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.5	-1.3	–	-0.35	–	-0.23	–	-0.2	-1.3	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-0.9	–	-0.35	–	-0.23	–	-0.2	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}																mAdc
(V_{OL} = 0.5 Vdc)			5.0	0.5	–	0.4	0.6	–	0.28	–	0.23	–	0.2	0.6	–	0.16	–	
(V_{OL} = 1.5 Vdc)			10	1.1	–	0.9	1.6	–	0.65	–	0.6	–	0.5	1.6	–	0.4	–	
			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	1	P_Q	5.0	–	0.025	–	0.00025	–	0.025	1.5	–	0.25	–	0.00025	0.25	–	3.5	–
(C_L = 15 pF)			10	–	0.10	–	0.001	–	0.10	6.0	–	1.0	–	0.001	1.0	–	14	–
			15	–	–	–	0.0025	–	–	–	–	–	–	0.0025	–	–	–	–
Total Power Dissipation **† (Dynamic Plus Quiescent) (C_L = 15 pF)	1	P_D	5.0	P_D = (2.5 mW/MHz) f + 0.00025 mW														mW
			10	P_D = (10.5 mW/MHz) f + 0.001 mW														
			15	P_D = (25 mW/MHz) f + 0.0025 mW														
Output Rise and Fall Time** (C_L = 15 pF)	2	t_r, t_f																ns
t_r, t_f = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r, t_f = (1.2 ns/pF) C_L + 12 ns			10	–	–	–	30	75	–	–	–	–	–	30	110	–	–	
t_r, t_f = (1.0 ns/pF) C_L + 10 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Clock to Out Propagation Delay Time** (C_L = 15 pF)	2	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.4 ns/pF) C_L + 129 ns			5.0	–	–	–	150	300	–	–	–	–	–	150	400	–	–	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 62.5 ns			10	–	–	–	70	150	–	–	–	–	–	70	200	–	–	
t_{PLH}, t_{PHL} = (0.4 ns/pF) C_L + 42 ns			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Clock to $\overline{Out}$ Propagation Delay Time (C_L = 15 pF)	2	t_{PLH}, t_{PHL}	5.0	–	–	–	70	160	–	–	–	–	–	70	280	–	–	ns
			10	–	–	–	35	80	–	–	–	–	–	35	100	–	–	
			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	

(Continued on next page)

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external Load Capacitance (C_L) refer to corresponding formula:

$$P_T(C_L) = P_D + 1.2 \times 10^{-3} (C_L - 15\,pF) V_{DD}^2 f$$

Where: P_T, P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14527AL							MC14527CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Clock to E_{out} Propagation Delay Time (C_L = 15 pF)	2	t_{PLH},t_{PHL}	5.0	–	–	–	240	500	–	–	–	–	–	240	900	–	–	ns
			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Clock to "9" Propagation Delay Time (C_L = 15 pF)	2	t_{PLH},t_{PHL}	5.0	–	–	–	350	600	–	–	–	–	–	350	1000	–	–	ns
			10	–	–	–	125	250	–	–	–	–	–	125	400	–	–	
			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	2	PW_C	5.0	–	–	–	250	340	–	–	–	–	–	250	500	–	–	ns
			10	–	–	–	110	170	–	–	–	–	–	110	200	–	–	
			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Maximum Clock Frequency (C_L = 15 pF)	2	PRF	5.0	–	–	1.5	2.0	–	–	–	–	–	1.0	2.0	–	–	–	MHz
			10	–	–	3.0	4.5	–	–	–	–	–	2.5	4.5	–	–	–	
			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Set or Clear to Out Propagation Delay Time (C_L = 15 pF)	2	t_{PHL}	5.0	–	–	–	350	700	–	–	–	–	–	350	1000	–	–	ns
			10	–	–	–	150	300	–	–	–	–	–	150	400	–	–	
			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Set Removal Time	2	t_{rem}	5.0	–	–	–	-20	0	–	–	–	–	–	-20	0	–	–	ns
			10	–	–	–	-10	0	–	–	–	–	–	-10	0	–	–	
Enable In Setup Time (C_L = 15 pF)	2	t_{setup}	5.0	–	–	–	175	350	–	–	–	–	–	175	400	–	–	ns
			10	–	–	–	60	120	–	–	–	–	–	60	150	–	–	
			15	–	–	–	45	–	–	–	–	–	–	45	–	–	–	
Minimum Set or Clear Pulse Width (C_L = 15 pF)	2	PW_S, PW_{Clear}	5.0	–	–	–	80	180	–	–	–	–	–	80	240	–	–	ns
			10	–	–	–	35	70	–	–	–	–	–	35	100	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Maximum Clock Rise and Fall Time (C_L = 15 pF)	2	t_r,t_f	5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	μs
			10	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
Cascade to Out Propagation Delay Time (C_L = 15 pF)	2	t_{PLH}	5.0	–	–	–	70	140	–	–	–	–	–	70	280	–	–	ns
			10	–	–	–	30	60	–	–	–	–	–	30	100	–	–	
			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Strobe to Out Propagation Delay Time (C_L = 15 pF)	2	t_{PLH}	5.0	–	–	–	175	350	–	–	–	–	–	175	700	–	–	ns
			10	–	–	–	75	150	–	–	–	–	–	75	250	–	–	
			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

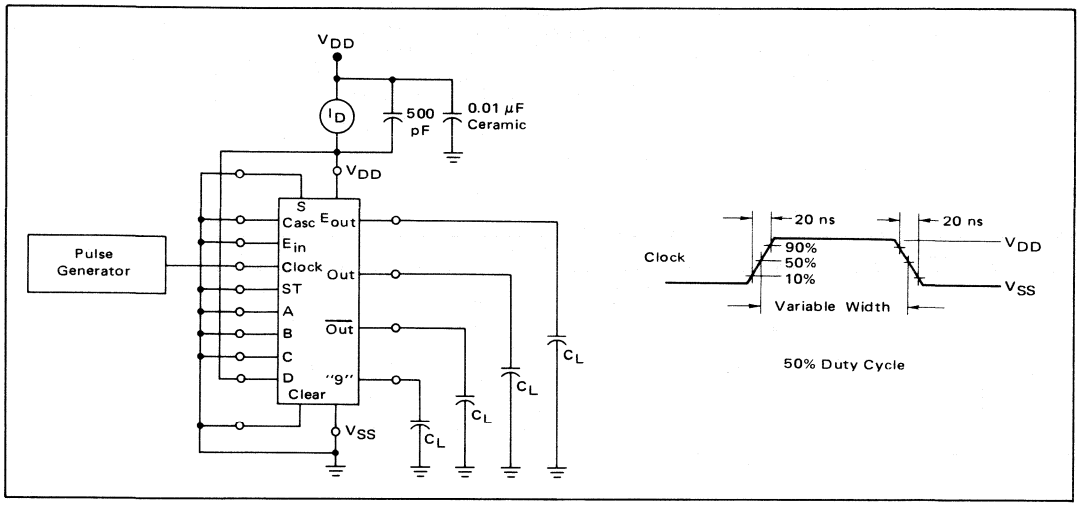
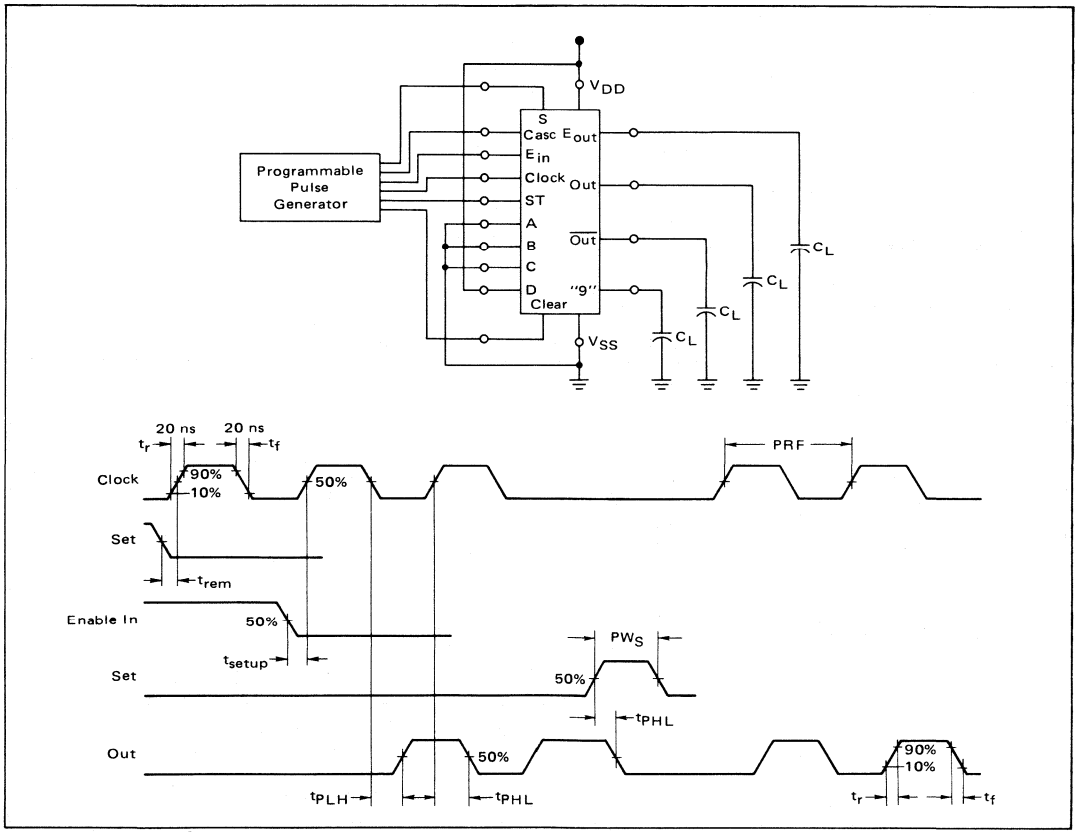


FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM

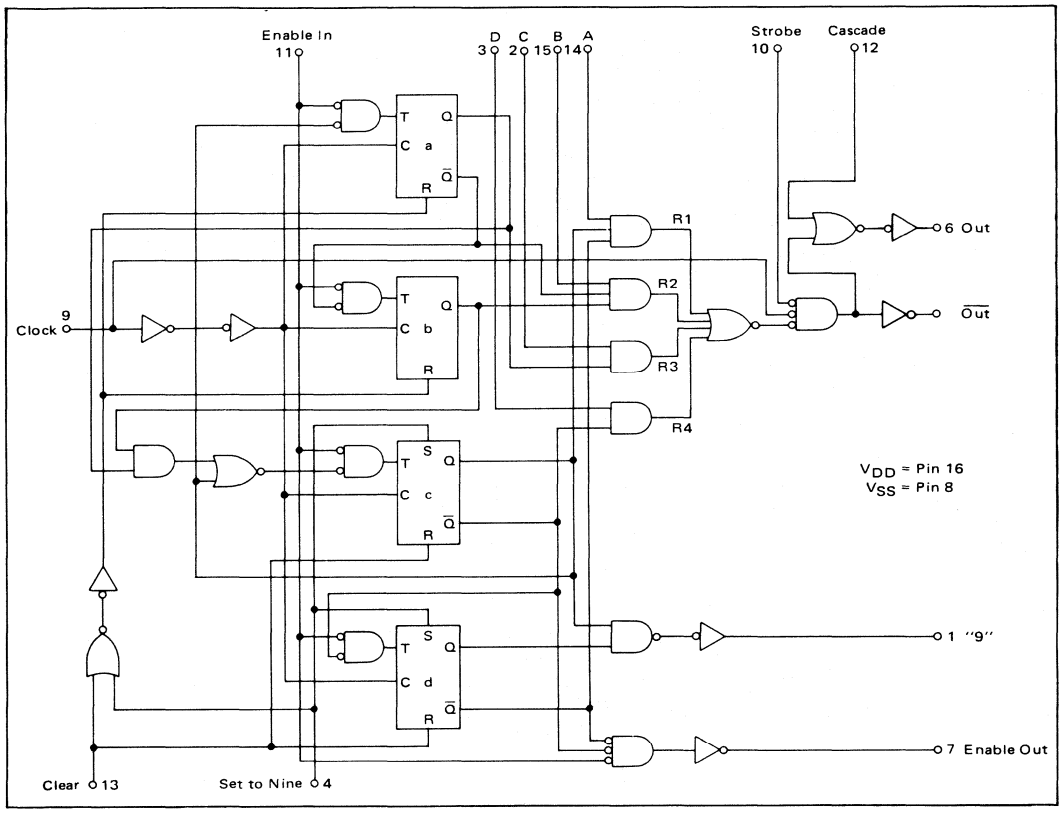


FIGURE 3 – TWO MC14527s IN CASCADE WITH PRESET NO. OF 94

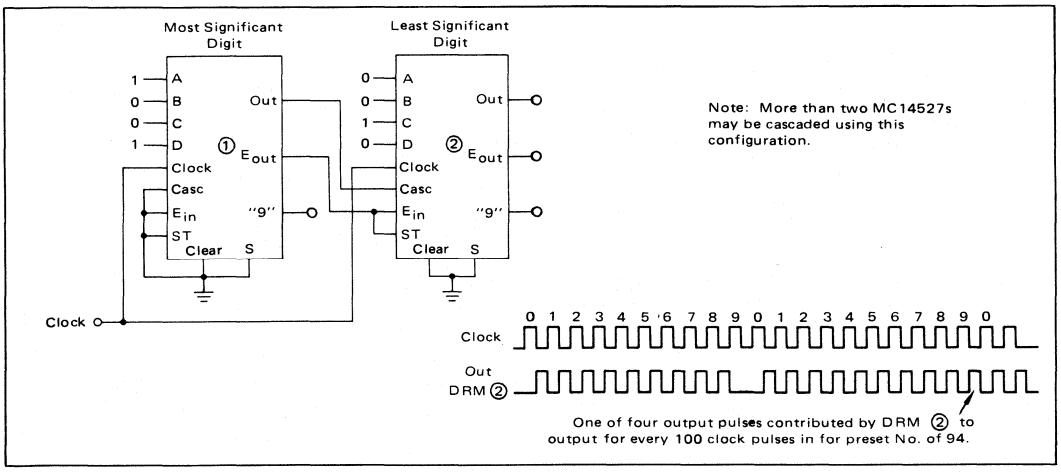
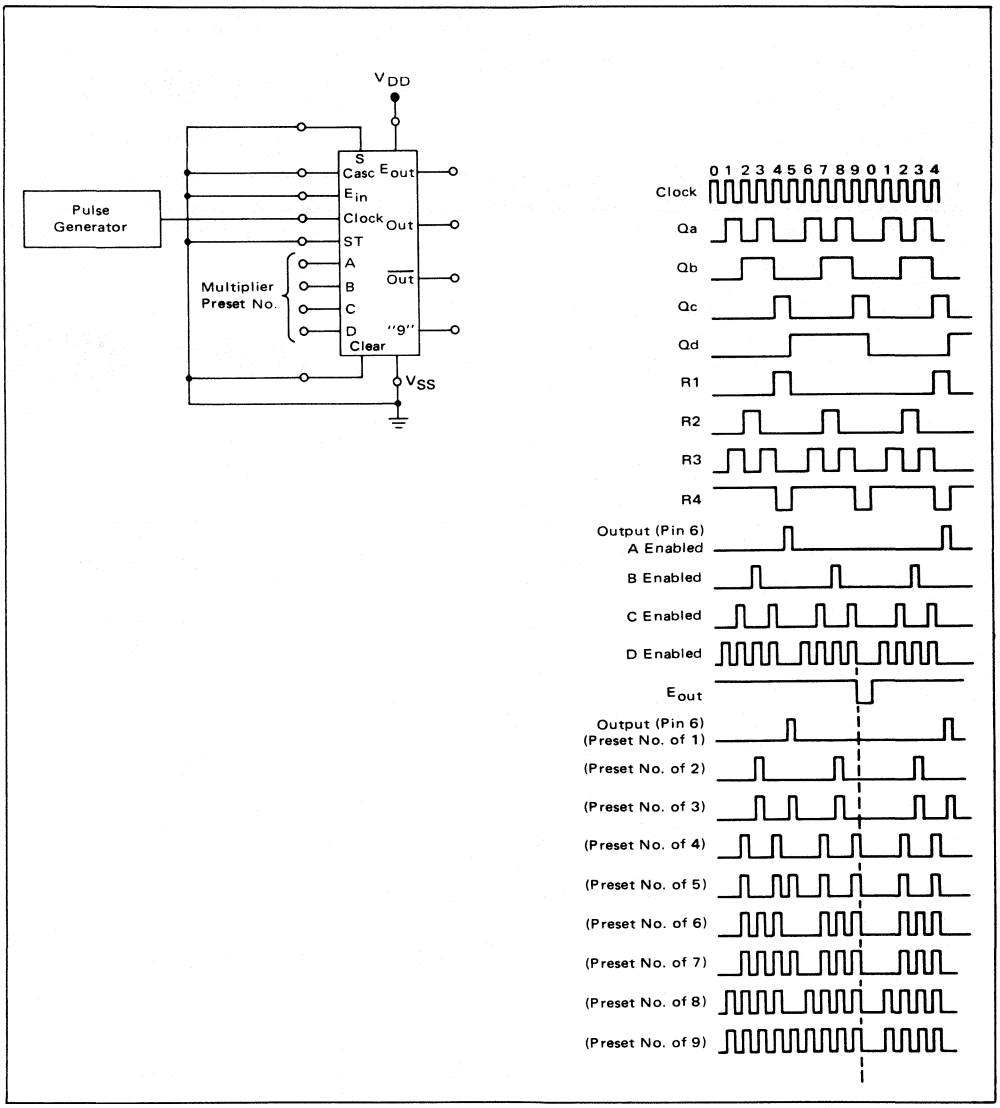


FIGURE 4 – TEST CIRCUIT AND TIMING DIAGRAM



MC14528AL
MC14528CL
MC14528CP

MONOSTABLE MULTIVIBRATOR

DUAL MONOSTABLE MULTIVIBRATOR

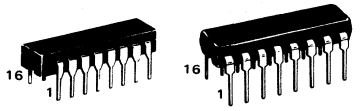
The MC14528 provides the function of a dual, retriggerable, resettable, monostable multivibrator. This device may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Low Quiescent Power Dissipation – 25 nW @ 5.0 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



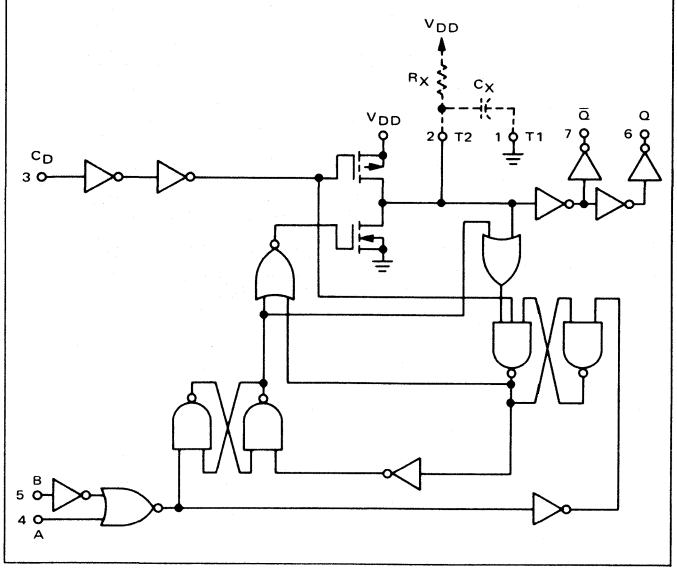
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

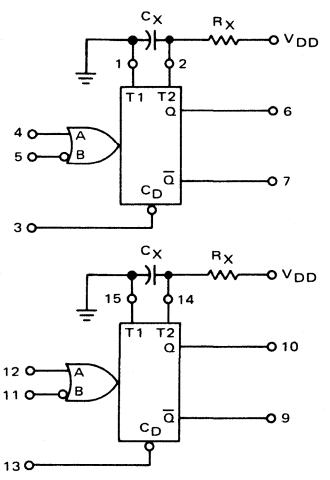
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	– MC14528AL – MC14528CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	– MC14528AL – MC14528CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

LOGIC DIAGRAM
(1/2 of Device Shown)



BLOCK DIAGRAM



R_X and C_X are external components.

V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	MC14528AL -55°C Min	MC14528AL -55°C Max	MC14528AL +25°C Min	MC14528AL +25°C Typ	MC14528AL +25°C Max	MC14528AL +125°C Min	MC14528AL +125°C Max	MC14528CL/CP -40°C Min	MC14528CL/CP -40°C Max	MC14528CL/CP +25°C Min	MC14528CL/CP +25°C Typ	MC14528CL/CP +25°C Max	MC14528CL/CP +85°C Min	MC14528CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	–	–	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			–	–	10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
"1" Level			–	–	5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			–	–	10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
Noise Immunity*																				
(V_{out} ≥3.5 Vdc)	–	V_{NL}	–	–	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} ≥7.0 Vdc)			–	–	10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≥10.5 Vdc)			–	–	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≤1.5 Vdc)		V_{NH}	–	–	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)			–	–	10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≤4.5 Vdc)			–	–	15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																				
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	–	–	5.0	-0.62	–	-0.5	-2.5	–	-0.35	–	-0.23	–	-0.2	-2.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			–	–	10	-0.62	–	-0.5	-1.1	–	-0.35	–	-0.23	–	-0.2	-1.1	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			–	–	15	–	–	–	-4.6	–	–	–	–	–	–	-4.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	–	–	5.0	0.5	–	0.4	1.6	–	0.28	–	0.23	–	0.2	1.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			–	–	10	1.1	–	0.9	3.4	–	0.65	–	0.6	–	0.5	3.4	–	0.4	–	
(V_{OL} = 1.5 Vdc)			–	–	15	–	–	–	14	–	–	–	–	–	–	14	–	–	–	
Input Current	–	I_{in}	–	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	3,6	P_D	–	–	5.0	–	5.0	–	0.025	5.0	–	300	–	50	–	0.025	50	–	700	μW
			–	–	10	–	20	–	0.05	20	–	1200	–	200	–	0.05	200	–	2800	
			–	–	15	–	–	–	0.25	–	–	–	–	–	–	0.25	–	–	–	
Output Rise and Fall Time**																				
(C_L = 15 pF)																				
t_r, t_f = (1.3 ns/pF) C_L + 12 ns	4,5	t_r, t_f	15	5.0	5.0	–	–	–	35	175	–	–	–	–	–	35	200	–	–	ns
t_r, t_f = (0.64 ns/pF) C_L + 6.0 ns			↓	↓	10	–	–	–	25	75	–	–	–	–	–	25	110	–	–	
t_r, t_f = (0.48 ns/pF) C_L + 6.0 ns			↓	↓	15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Output Rise and Fall Time	4,5	t_r, t_f	1000	10	5.0	–	–	–	270	–	–	–	–	–	–	270	–	–	–	ns
(C_L = 15 pF)			↓	↓	10	–	–	–	240	–	–	–	–	–	–	240	–	–	–	
			↓	↓	15	–	–	–	220	–	–	–	–	–	–	220	–	–	–	
A or B to Q or $\bar{Q}$ Propagation Delay** (C_L = 15 pF)																				
t_{PLH}, t_{PHL} = (0.75 ns/pF) C_L + 163 ns	4,5	t_{PLH}, t_{PHL}	15	5.0	5.0	–	–	–	195	400	–	–	–	–	–	195	600	–	–	ns
t_{PLH}, t_{PHL} = (0.39 ns/pF) C_L + 163 ns			↓	↓	10	–	–	–	80	175	–	–	–	–	–	80	240	–	–	
t_{PLH}, t_{PHL} = (0.21 ns/pF) C_L + 42 ns			↓	↓	15	–	–	–	55	–	–	–	–	–	–	55	–	–	–	
Propagation Delay Time	4,5	t_{PLH}, t_{PHL}	1000	10	5.0	–	–	–	475	–	–	–	–	–	–	475	–	–	–	ns
(C_L = 15 pF)			↓	↓	10	–	–	–	230	–	–	–	–	–	–	230	–	–	–	
			↓	↓	15	–	–	–	150	–	–	–	–	–	–	150	–	–	–	
Minimum Input Pulse Width																				
(C_L = 15 pF) (A or B)	4,5	PW_{in}	15	5.0	5.0	–	–	–	70	150	–	–	–	–	–	70	240	–	–	ns
			↓	↓	10	–	–	–	30	75	–	–	–	–	–	30	120	–	–	
			↓	↓	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
			1000	10	5.0	–	–	–	70	–	–	–	–	–	–	70	–	–	–	ns
			↓	↓	10	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
			↓	↓	15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Q or $\bar{Q}$ Output Pulse Width																				
(C_L = 15 pF)	4,5,	PW_{out}																		
For C_X < 1000 pF use graph for appropriate V_{DD} level. For C_X > 1000 pF use formula.	7,8,9		15	5.0	5.0	–	–	–	420	–	–	–	–	–	–	420	–	–	–	ns
			↓	↓	10	–	–	–	260	–	–	–	–	–	–	260	–	–	–	
			↓	↓	15	–	–	–	225	–	–	–	–	–	–	225	–	–	–	
			1000	10	5.0	–	–	–	10	–	–	–	–	–	–	10	–	–	–	μs
			↓	↓	10	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
			↓	↓	15	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
Reset Propagation Delay																				
(C_L = 15 pF)	4,5	t_{PLH}, t_{PHL}	15	5.0	5.0	–	–	–	160	300	–	–	–	–	–	160	450	–	–	ns
(C_D to Q or $\bar{Q}$)			↓	↓	10	–	–	–	60	150	–	–	–	–	–	60	225	–	–	
			↓	↓	15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
			1000	10	5.0	–	–	–	550	–	–	–	–	–	–	550	–	–	–	ns
			↓	↓	10	–	–	–	300	–	–	–	–	–	–	300	–	–	–	
			↓	↓	15	–	–	–	250	–	–	–	–	–	–	250	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change, from an ideal "1" or "0" input level, that the circuit will withstand before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

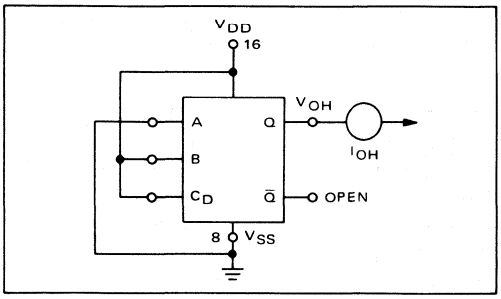


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

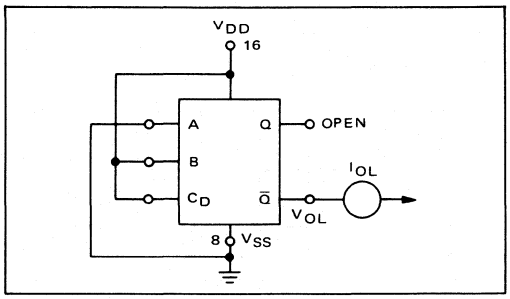


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS

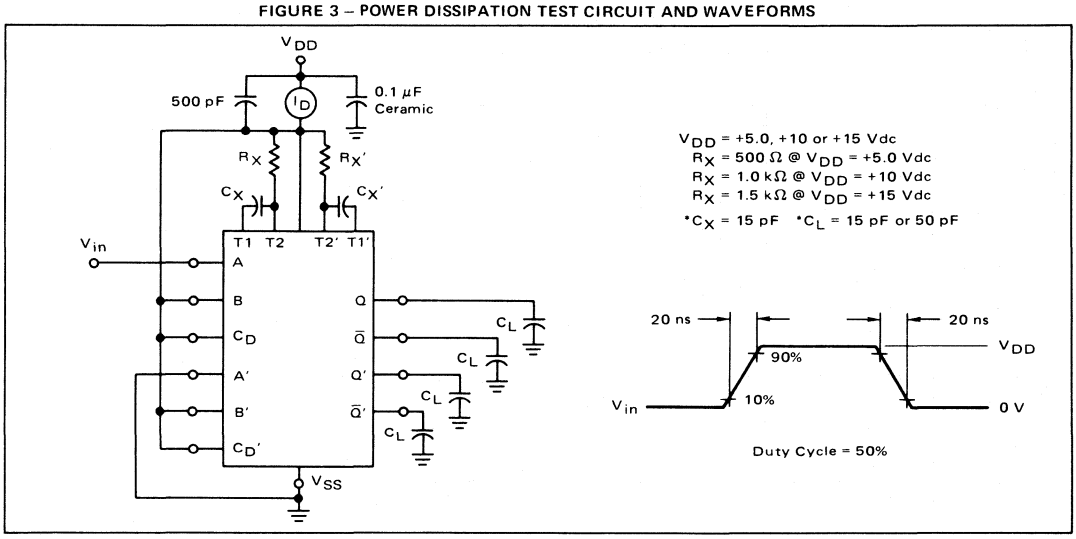
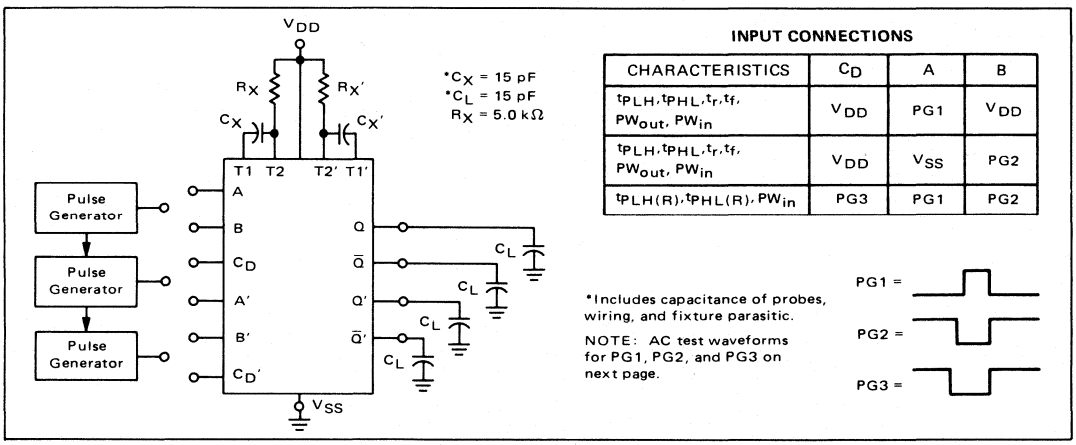


FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	C_D	A	B
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	PG1	V_{DD}
$t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}$	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}, t_{PHL(R)}, PW_{in}$	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

PG1 =

PG2 =

PG3 =

7

FIGURE 5 – AC TEST WAVEFORMS

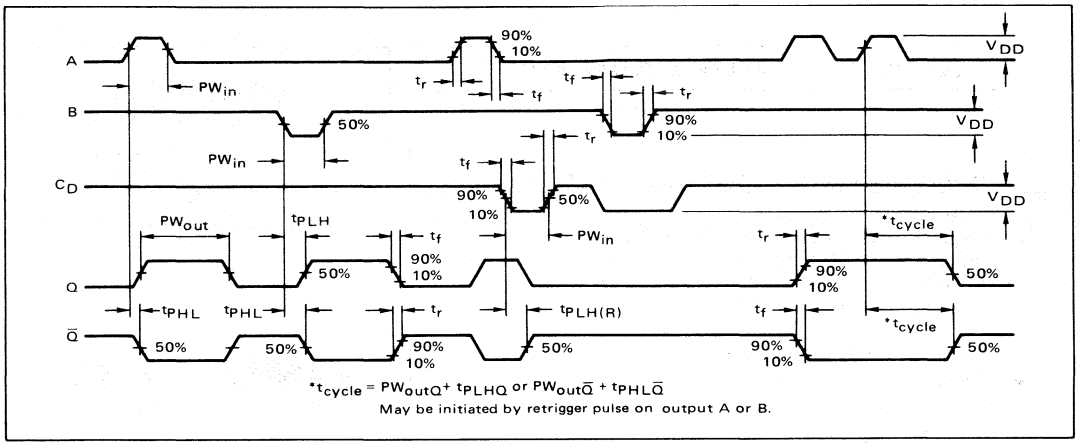


FIGURE 6 – POWER DISSIPATION CHARACTERISTICS

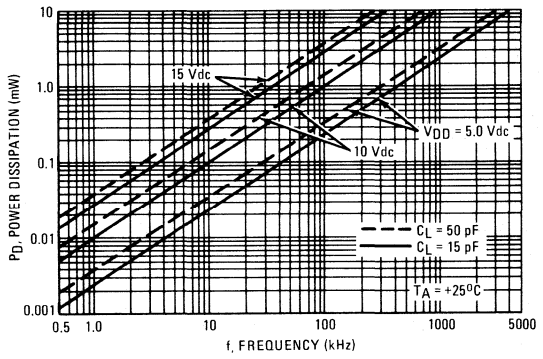


FIGURE 7 – C_X versus PULSE WIDTH @ V_{DD} = 5.0 V

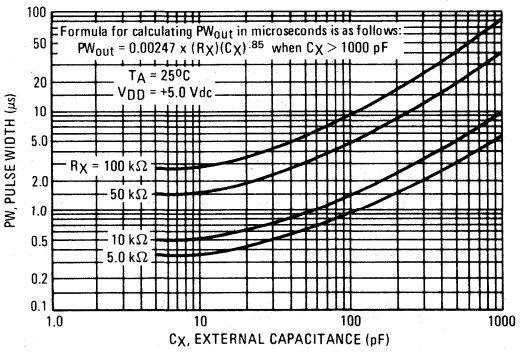


FIGURE 8 – C_X versus PULSE WIDTH @ V_{DD} = 10 V

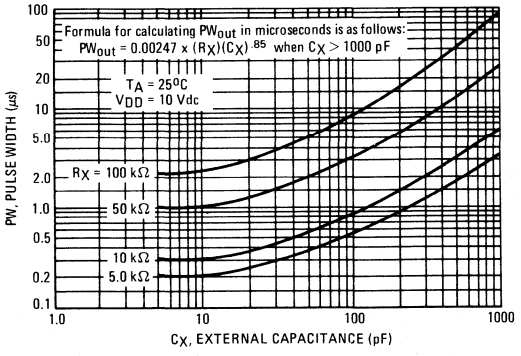
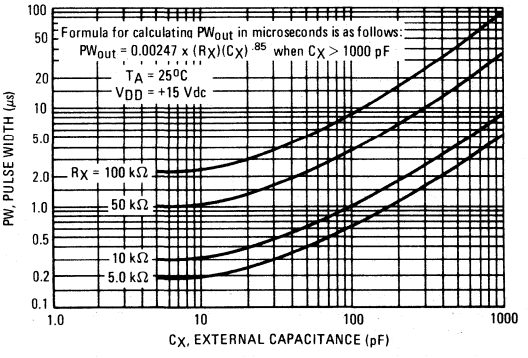


FIGURE 9 – C_X versus PULSE WIDTH @ V_{DD} = 15 V



7

MC14529AL
MC14529CL
MC14529CP

DATA SELECTOR

Advance Information

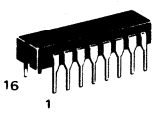
DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529 analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. It is constructed with complementary MOS (CMOS) enhancement mode devices in a single monolithic structure. Applications include various one-of-four or one-of-eight data selector functions.

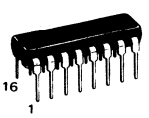
- Low Quiescent Power Dissipation
- 10-MHz Operation (typical)
- 3-State Outputs
- Linear "On" Resistance
- "On" Resistance 140 ohms typical @ 15 V

McMOS
(LOW-POWER COMPLEMENTARY MOS)

DUAL 4-CHANNEL ANALOG DATA SELECTOR OR 8-CHANNEL ANALOG DATA SELECTOR



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

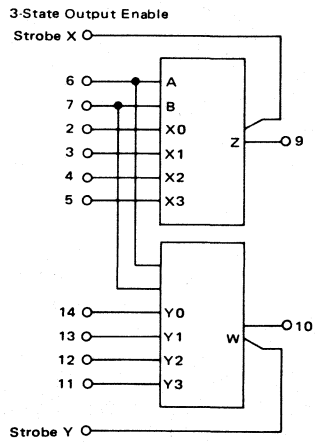
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	MC14529AL MC14529CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range —	MC14529AL MC14529CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	ϕ	ϕ	High Impedance		

ϕ = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.
See Mechanical Data Section for package dimensions.

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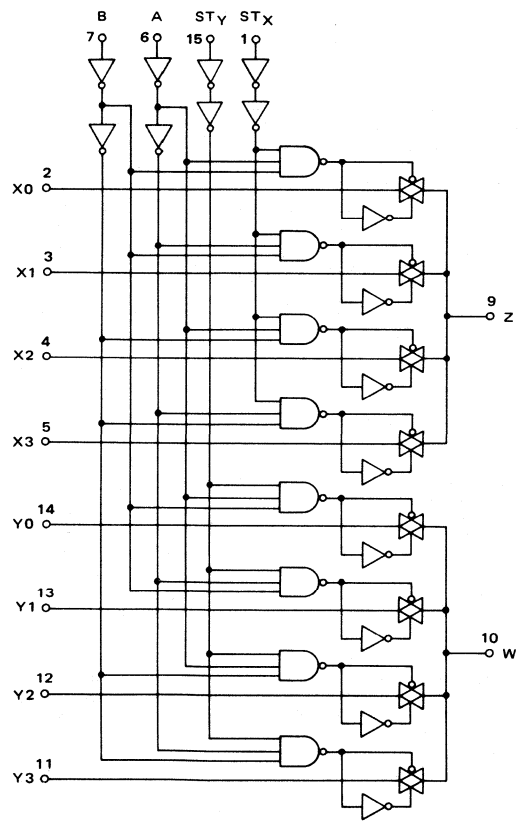
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{SS} Vdc	V_{DD} Vdc	MC14529AL +25°C Min	MC14529AL +25°C Typ	MC14529AL +25°C Max	MC14529CL/CP +25°C Min	MC14529CL/CP +25°C Typ	MC14529CL/CP +25°C Max	Unit
Quiescent Dissipation	P_D	–	5.0	–	0.1	–	–	0.1	–	μW
		–	10	–	0.25	–	–	0.25	–	
		–	15	–	0.4	–	–	0.4	–	
"ON" Resistance ($V_C = V_{DD}$, $R_L = 10\ k\Omega$)	R_{ON}									ohms
(V_{in} = +5.0 Vdc)		-5.0	5.0	–	220	–	–	220	–	
(V_{in} = -5.0 Vdc)				–	220	–	–	220	–	
(V_{in} = ±0.25 Vdc)				–	340	–	–	340	–	
(V_{in} = +7.5 Vdc)		-7.5	7.5	–	160	–	–	160	–	
(V_{in} = -7.5 Vdc)				–	160	–	–	160	–	
(V_{in} = ±0.25 Vdc)				–	260	–	–	260	–	
(V_{in} = +10 Vdc)		0	10	–	180	–	–	180	–	
(V_{in} = +0.25 Vdc)				–	260	–	–	260	–	
(V_{in} = +5.6 Vdc)				–	260	–	–	260	–	
(V_{in} = +15 Vdc)		0	15	–	140	–	–	140	–	
(V_{in} = +0.25 Vdc)				–	140	–	–	140	–	
(V_{in} = +9.3 Vdc)				–	180	–	–	180	–	
△"ON" Resistance Between any 2 of 4 circuits in a common package	$\triangle R_{ON}$									ohms
($V_C = V_{DD}$, V_{in} = ±5.0 Vdc)		-5.0	5.0	–	15	–	–	15	–	
($V_C = V_{DD}$, V_{in} = ±7.5 Vdc)		-7.5	7.5	–	10	–	–	10	–	

LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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MC14530AL
MC14530CL
MC14530CP

MAJORITY LOGIC GATE

DUAL 5-INPUT MAJORITY LOGIC GATE

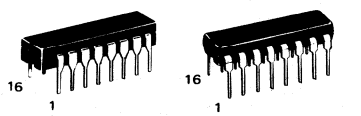
The MC14530 dual five-input majority logic gate is constructed with P-channel and N-channel enhancement mode devices in a single monolithic structure. Combinational and sequential logic expressions are easily implemented with the majority logic gate, often resulting in fewer components than obtainable with the more basic gates. This device can also provide numerous logic functions by using the W and some of the logic (A thru E) inputs as control inputs.

- Single Supply Operation – Positive or Negative
- Quiescent Power Dissipation = 50 nW/package typical
- Input Impedance = 10^{12} ohms typical
- High Fanout – > 50
- Diode Protection on Inputs
- Noise Immunity = 45% of V_{DD} typical

McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL 5-INPUT MAJORITY LOGIC GATE



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

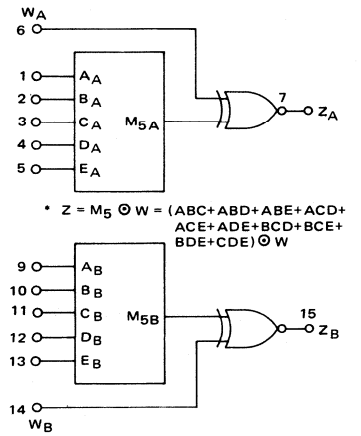
Rating	Symbol	Value	Unit
DC Supply Voltage MC14530AL MC14530CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14530AL MC14530CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LOGIC TABLE

INPUTS	OUTPUTS		
Inputs A B C D E	M_5	W	Z
For all combinations of inputs where three or more inputs are logical "0".	0	0	1
	0	1	0
For all combinations of inputs where three or more inputs are logical "1".	1	0	0
	1	1	1

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must be tied to an appropriate logic level (e.g., V_{SS} or V_{DD}).

BLOCK DIAGRAM



* $Z = M_5 \odot W = (ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE) \odot W$

*M_5 is a logical "1" if any three or more inputs are logical "1".

$\odot \equiv$ Exclusive NOR $\equiv \overline{\text{Exclusive OR}}$

TRUTH TABLE

M_5	W	Z
0	0	1
0	1	0
1	0	0
1	1	1

V_{DD} = Pin 16
V_{SS} = Pin 8

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14530AL -55°C Min	MC14530AL -55°C Max	MC14530AL +25°C Min	MC14530AL +25°C Typ	MC14530AL +25°C Max	MC14530AL +125°C Min	MC14530AL +125°C Max	MC14530CL/CP -40°C Min	MC14530CL/CP -40°C Max	MC14530CL/CP +25°C Min	MC14530CL/CP +25°C Typ	MC14530CL/CP +25°C Max	MC14530CL/CP +85°C Min	MC14530CL/CP +85°C Max	Unit
Output Voltage "0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
(V_{out} ≥3.5 Vdc)		V_{NL}	5.0	1.25	–	1.25	2.25	–	1.15	–	1.25	–	1.25	2.25	–	1.15	–	Vdc
(V_{out} ≥7.0 Vdc)			10	2.5	–	2.5	4.50	–	2.4	–	2.5	–	2.5	4.50	–	2.4	–	
(V_{out} ≥10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≤1.5 Vdc)		V_{NH}	5.0	1.15	–	1.25	2.25	–	1.25	–	1.15	–	1.25	2.25	–	1.25	–	Vdc
(V_{out} ≤3.0 Vdc)			10	2.4	–	2.5	4.50	–	2.5	–	2.4	–	2.5	4.50	–	2.5	–	
(V_{out} ≤4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source		I_{OH}	5.0	-0.62	–	-0.50	-1.5	–	-0.35	–	-0.24	–	-0.20	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.0	–	-0.35	–	-0.24	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.50	–	0.40	0.65	–	0.28	–	0.24	–	0.20	0.65	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	1.6	–	0.62	–	0.60	–	0.50	1.6	–	0.41	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capactiance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	1,2	P_D																μW
			5.0	–	–	–	0.05	0.25	–	–	–	–	–	0.05	2.5	–	–	
			10	–	–	–	0.1	1.0	–	–	–	–	–	0.1	10	–	–	
			15	–	–	–	0.3	–	–	–	–	–	–	0.3	–	–	–	
Output Rise and Fall Time**		t_r, t_f																ns
(C_L = 15 pF)																		
t_r, t_f = (2.5 ns/pF) C_L + 57 ns			5.0	–	–	–	95	175	–	–	–	–	–	95	200	–	–	
t_r, t_f = (1.13 ns/pF) C_L + 28 ns			10	–	–	–	45	75	–	–	–	–	–	45	110	–	–	
t_r, t_f = (0.88 ns/pF) C_L + 16.8 ns			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Turn-On Delay Time**		t_{PHL}																ns
(C_L = 15 pF)																		
A,C,W at V_{DD}, B,E at Gnd																		
D = Pulse Generator																		
t_{PHL} = (1.6 ns/pF) C_L + 375 ns			5.0	–	–	–	400	800	–	–	–	–	–	400	1200	–	–	
t_{PHL} = (0.5 ns/pF) C_L + 172 ns			10	–	–	–	180	360	–	–	–	–	–	180	540	–	–	
t_{PHL} = (0.36 ns/pF) C_L + 105 ns			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Turn-Off Delay Time**		t_{PLH}																ns
(C_L = 15 pF)																		
A,C,W at V_{DD}, B,E at Gnd																		
D = Pulse Generator																		
t_{PLH} = (1.5 ns/pF) C_L + 298 ns			5.0	–	–	–	320	640	–	–	–	–	–	320	960	–	–	
t_{PLH} = (0.5 ns/pF) C_L + 123 ns			10	–	–	–	130	260	–	–	–	–	–	130	390	–	–	
t_{PLH} = (0.4 ns/pF) C_L + 84 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Turn-On Delay Time**		t_{PHL}																ns
(C_L = 15 pF)																		
A,B,C,D,E = Pulse Generator																		
W at V_{DD}																		
t_{PHL} = (1.4 ns/pF) C_L + 229 ns			5.0	–	–	–	250	500	–	–	–	–	–	250	750	–	–	
t_{PHL} = (0.54 ns/pF) C_L + 102 ns			10	–	–	–	110	220	–	–	–	–	–	110	330	–	–	
t_{PHL} = (0.36 ns/pF) C_L + 85 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Turn-Off Delay Time**		t_{PLH}																ns
(C_L = 15 pF)																		
A,B,C,D,E = Pulse Generator																		
W at V_{DD}																		
t_{PLH} = (1.4 ns/pF) C_L + 179 ns			5.0	–	–	–	200	400	–	–	–	–	–	200	600	–	–	
t_{PLH} = (0.5 ns/pF) C_L + 83 ns			10	–	–	–	90	180	–	–	–	–	–	90	270	–	–	
t_{PLH} = (0.4 ns/pF) C_L + 59 ns			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Turn-On, Turn-Off Delay Time**		t_{PHL}, t_{PLH}																ns
(C_L = 15 pF)																		
A,B,C,D,E at Gnd																		
W = Pulse Generator																		
t_{PHL},t_{PLH} = (1.3 ns/pF) C_L + 155 ns			5.0	–	–	–	175	350	–	–	–	–	–	175	525	–	–	
t_{PHL},t_{PLH} = (0.56 ns/pF) C_L + 67 ns			10	–	–	–	75	150	–	–	–	–	–	75	225	–	–	
t_{PHL},t_{PLH} = (0.36 ns/pF) C_L + 50 ns			15	–	–	–	55	–	–	–	–	–	–	55	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change. Standard Family Noise Margin spec is met for any one input variable tested at a time.

**The formula given is for the typical characteristics only.

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

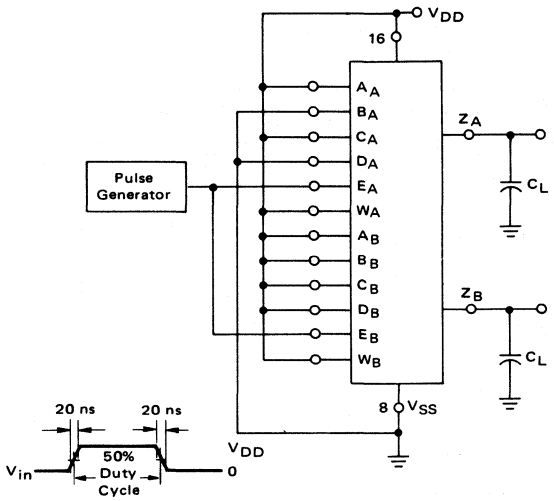
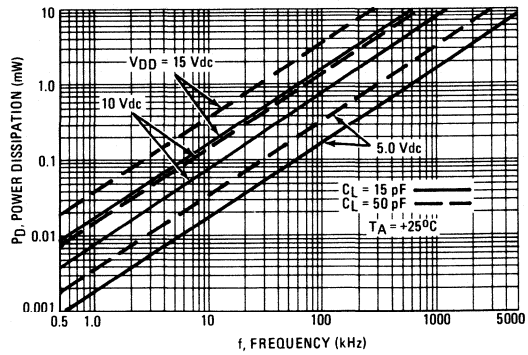
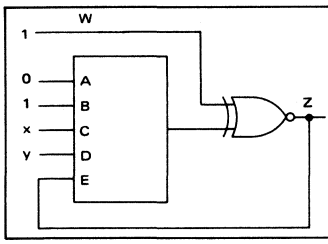


FIGURE 2 – POWER DISSIPATION CHARACTERISTICS



SEQUENTIAL LOGIC APPLICATIONS

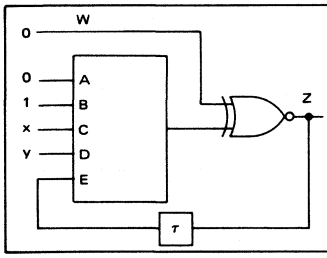
COINCIDENT FLIP-FLOP



x	y	Q_{n+1}
0	0	0
0	1	Q
1	0	Q
1	1	1

A flip-flop that will change only when both inputs agree.

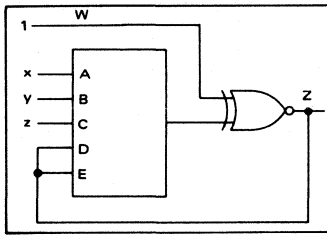
ASTABLE MULTIVIBRATOR



x	y	Q_{n+1}
0	0	1
0	1	2τ
1	0	2τ
1	1	0

A flip-flop with three output conditions, where the third state is in oscillation between "1" and "0". The period of oscillation is twice the delay of the gate and the feedback element.

COINCIDENT FLIP-FLOP

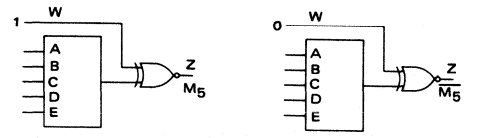


x	y	z	Q_{n+1}
0	0	0	0
0	0	1	Q_n
0	1	0	Q_n
0	1	1	Q_n
1	0	0	Q_n
1	0	1	Q_n
1	1	0	Q_n
1	1	1	1

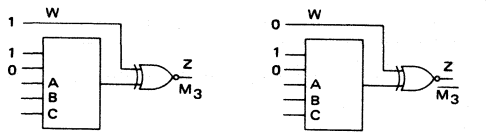
The flip-flop changes state only when all "1's" or all "0's" are entered. This configuration may be extended by cascading M_5 gates to cover n-inputs where all inputs must be "1's" or "0's" before the output will change. As an example, this configuration is useful for controlling an n-stage up/down counter that is to cycle from a minimum to maximum count and back again without flipping over (from all "1's" to all "0's".)

7

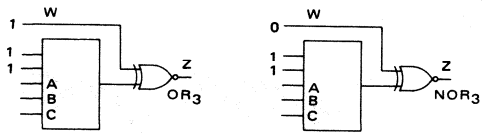
BASIC COMBINATIONAL FUNCTIONS



5-Input Majority Gates

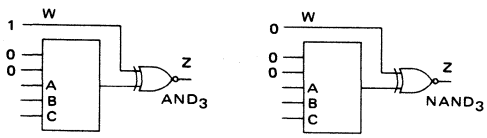


3-Input Majority Gates



3-Input OR Gate

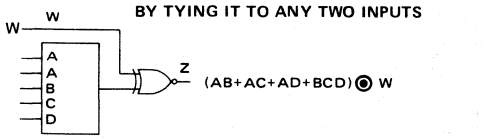
3-Input NOR Gate



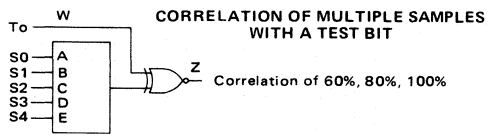
3-Input AND Gate

3-Input NAND Gate

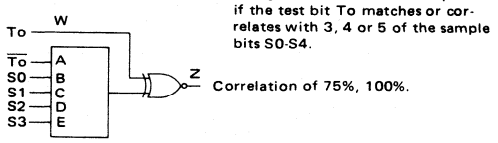
DOUBLING THE WEIGHT OF INPUT VARIABLE A BY TYING IT TO ANY TWO INPUTS

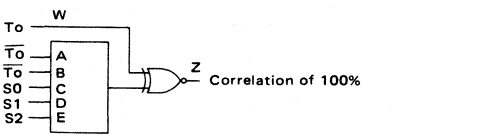


CORRELATION OF MULTIPLE SAMPLES WITH A TEST BIT



The gate will have a "1" output if the test bit To matches or correlates with 3, 4 or 5 of the sample bits S0-S4.



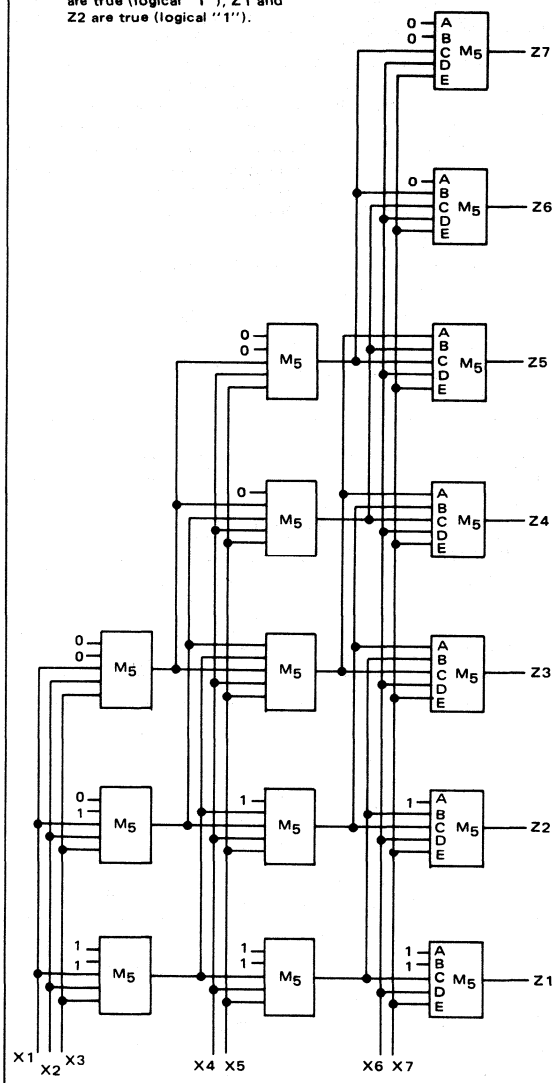


5-INPUT MAJORITY LOGIC GATE APPLICATIONS

Each package labeled M_5 is a single majority logic gate using five inputs, A thru E, and one output Z.

1. Majority Logic Gate Array yielding the symetric function of 1 thru 7 variables true, out of 7 input variables (X1 . . . X7)

(e.g., if any two-input variables are true (logical "1"), Z1 and Z2 are true (logical "1").



MC14531AL
MC14531CL
MC14531CP

12-BIT PARITY TREE

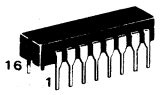
The MC14531 12-bit parity tree is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of 12 data-bit inputs (D0 thru D11), an even or odd parity selection input (W) and an output (Q). The parity selection input can be considered as an additional bit. Words of less than 13 bits can generate an even or odd parity output if the remaining inputs are selected to contain an even or odd number of ones, respectively. Words of greater than 12-bits can be accommodated by cascading other MC14531 devices by using the W input. Applications include checking or including a redundant (parity) bit to a word for error detection/correction systems, controller for remote digital sensors or switches (digital event detection/correction), or as a multiple input summer without carries.

- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Buffered Outputs Compatible With HTL and Low Power TTL
- Quiescent Power Dissipation – 25 nW typical
- Variable Word Length
- Static Operation from dc to 5.0 MHz typical

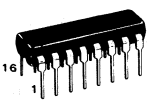
McMOS

(LOW-POWER COMPLEMENTARY MOS)

12-BIT PARITY TREE



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage —MC14531AL —MC14531CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range —MC14531AL —MC14531CL/CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

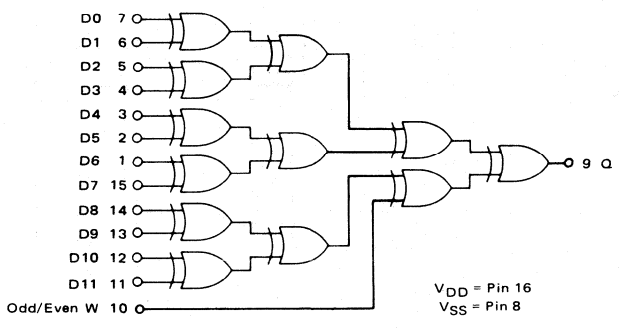
TRUTH TABLE

INPUTS								OUTPUT
W	D11	D10	– –	D2	D1	D0	DECIMAL (OCTAL) EQUIVALENT	Q*
0	0	0	– –	0	0	0	0 (0)	0
0	0	0	– –	0	0	1	1 (1)	1
0	0	0	– –	0	1	0	2 (2)	1
0	0	0	– –	0	1	1	3 (3)	0
0	0	0	– –	1	0	0	4 (4)	1
0	0	0	– –	1	0	1	5 (5)	0
0	0	0	– –	1	1	0	6 (6)	0
0	0	0	– –	1	1	1	7 (7)	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	– –	0	0	0	8184 (17770)	0
1	1	1	– –	0	0	1	8185 (17771)	1
1	1	1	– –	0	1	0	8186 (17772)	1
1	1	1	– –	0	1	1	8187 (17773)	0
1	1	1	– –	1	0	0	8188 (17774)	1
1	1	1	– –	1	0	1	8189 (17775)	0
1	1	1	– –	1	1	0	8190 (17776)	0
1	1	1	– –	1	1	1	8191 (17777)	1

*0 = Even Parity
1 = Odd Parity

Note: May redefine to suit application by manipulating W and/or other available D's.

LOGIC DIAGRAM



Q = D0 ⊕ D1 ⊕ D2 ⊕ . . . . ⊕ D11 ⊕ W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14531AL -55°C Min	MC14531AL -55°C Max	MC14531AL +25°C Min	MC14531AL +25°C Typ	MC14531AL +25°C Max	MC14531AL +125°C Min	MC14531AL +125°C Max	MC14531CL/CP -40°C Min	MC14531CL/CP -40°C Max	MC14531CL/CP +25°C Min	MC14531CL/CP +25°C Typ	MC14531CL/CP +25°C Max	MC14531CL/CP +85°C Min	MC14531CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.5	-1.8	–	-0.35	–	-0.23	–	-0.2	-1.8	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.9	–	–	–	–	–	–	-3.9	–	–	–	
(V_{OL} = 0.4 Vdc) Sink		I_{OL}	5.0	0.5	–	0.4	0.78	–	0.28	–	0.23	–	0.2	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.0	–	0.65	–	0.6	–	0.5	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (0.8 mW/MHz) f + 0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (3.3 mW/MHz) f + 0.00010 mW			10	–	0.10	–	0.00010	0.10	–	6.0	–	1.0	–	0.00010	1.0	–	14	
P_D = (7.5 mW/MHz) f + 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.78 ns/pF) C_L + 23 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.59 ns/pF) C_L + 16 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time (D's)**	2	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (0.95 ns/pF) C_L + 335 ns			5.0	–	–	–	350	880	–	–	–	–	–	350	1320	–	–	
t_{PLH} = (0.50 ns/pF) C_L + 130 ns			10	–	–	–	140	350	–	–	–	–	–	140	525	–	–	
t_{PLH} = (0.35 ns/pF) C_L + 95 ns			15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Turn-On Delay Time (D's)**	2	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (0.6 ns/pF) C_L + 430 ns			5.0	–	–	–	440	880	–	–	–	–	–	440	1320	–	–	
t_{PHL} = (0.5 ns/pF) C_L + 165 ns			10	–	–	–	175	350	–	–	–	–	–	175	525	–	–	
t_{PHL} = (0.25 ns/pF) C_L + 115 ns			10	–	–	–	120	–	–	–	–	–	–	120	–	–	–	
Turn-Off Delay Time (W)**																		ns
(C_L = 15 pF)	2	t_{PLH}																
t_{PLH} = (0.9 ns/pF) C_L + 195 ns			5.0	–	–	–	210	500	–	–	–	–	–	210	750	–	–	
t_{PLH} = (0.6 ns/pF) C_L + 75 ns			10	–	–	–	85	200	–	–	–	–	–	85	300	–	–	
t_{PLH} = (0.35 ns/pF) C_L + 55 ns			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Turn-On Delay Time (W)**																		ns
(C_L = 15 pF)	2	t_{PHL}																
t_{PHL} = (0.6 ns/pF) C_L + 240 ns			5.0	–	–	–	250	500	–	–	–	–	–	250	750	–	–	
t_{PHL} = (0.4 ns/pF) C_L + 95 ns			10	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
t_{PHL} = (0.25 ns/pF) C_L + 65 ns			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORM

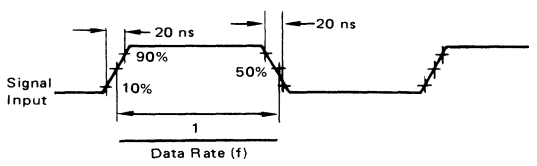
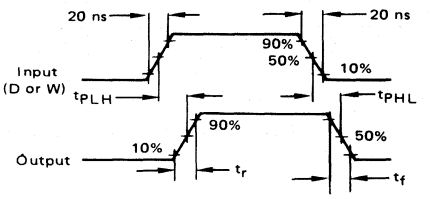


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



MC14532AL
MC14532CL
MC14532CP

PRIORITY ENCODER

Advance Information

8-BIT PRIORITY ENCODER

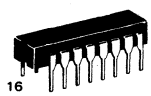
The MC14532AL/CL/CP is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

- Quiescent Power Dissipation = 0.025 μW/package typical @ 5.0 Vdc
- Noise immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical

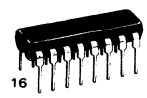
McMOS

(LOW-POWER COMPLEMENTARY MOS)

8-BIT PRIORITY ENCODER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltage referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14532AL MC14532CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14532AL —MC14532CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

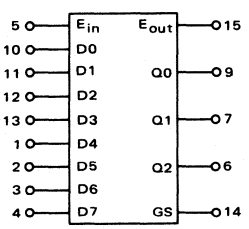
INPUT									OUTPUT				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care

This is advance information and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

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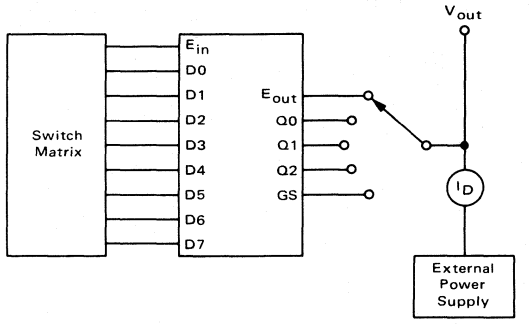
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	MC14532AL -55°C Min	MC14532AL -55°C Max	MC14532AL +25°C Min	MC14532AL +25°C Typ	MC14532AL +25°C Max	MC14532AL +125°C Min	MC14532AL +125°C Max	MC14532CL/CP -40°C Min	MC14532CL/CP -40°C Max	MC14532CL/CP +25°C Min	MC14532CL/CP +25°C Typ	MC14532CL/CP +25°C Max	MC14532CL/CP +85°C Min	MC14532CL/CP +85°C Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0.0	0.01	–	0.05	–	0.01	–	0.0	0.01	–	0.05	Vdc
		10	–	0.01	–	0.0	0.01	–	0.05	–	0.01	–	0.0	0.01	–	0.05	
		15	–	–	–	0.0	–	–	–	–	–	–	0.0	–	–	–	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
		10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
		15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																	
($V_{out} \geq 3.5$ Vdc)	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																	
(V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	I_{in}	–	–	–	–	–	10	–	–	–	–	–	–	10	–	–	pAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	pF
Quiescent Dissipation	P_D																mW
(C_L = 15 pF, f_o = 0)																	
P_D = (4.3 mW/MHz) f_o + 0.000025 mW		5.0	–	0.0025	–	0.000025	0.0025	–	0.15	–	0.025	–	0.000025	0.025	–	0.35	
P_D = (19 mW/MHz) f_o + 0.00005 mW		10	–	0.01	–	0.00005	0.01	–	0.6	–	0.10	–	0.00005	0.10	–	1.4	
P_D = (46.5 mW/MHz) f_o + 0.00035 mW		15	–	–	–	0.00035	–	–	–	–	–	–	0.00035	–	–	–	
Output Rise and Fall Time**	t_r, t_f																ns
(C_L = 15 pF)																	
t_r, t_f = (4.5 ns/pF) C_L + 32.5 ns		5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r, t_f = (1.0 ns/pF) C_L + 20 ns		10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r, t_f = (0.4 ns/pF) C_L + 14 ns		15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	
Propagation Delay Time**	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) E_{in} to E_{out}																	
t_{PHL}, t_{PLH} = (2.8 ns/pF) C_L + 108 ns		5.0	–	–	–	150	225	–	–	–	–	–	150	375	–	–	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 71 ns		10	–	–	–	80	120	–	–	–	–	–	80	200	–	–	
t_{PHL}, t_{PLH} = (0.25 ns/pF) C_L + 56 ns		15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Propagation Delay Time**	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) E_{in} to GS																	
t_{PHL}, t_{PLH} = (2.8 ns/pF) C_L + 78 ns		5.0	–	–	–	120	180	–	–	–	–	–	120	300	–	–	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 51 ns		10	–	–	–	60	90	–	–	–	–	–	60	150	–	–	
t_{PHL}, t_{PLH} = (0.25 ns/pF) C_L + 41 ns		15	–	–	–	45	–	–	–	–	–	–	45	–	–	–	
Propagation Delay Time**	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) E_{in} to Q_n																	
t_{PHL}, t_{PLH} = (2.8 ns/pF) C_L + 183 ns		5.0	–	–	–	225	340	–	–	–	–	–	225	550	–	–	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 101 ns		10	–	–	–	110	165	–	–	–	–	–	110	275	–	–	
t_{PHL}, t_{PLH} = (0.25 ns/pF) C_L + 76 ns		15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Propagation Delay Time**	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) D_n to Q_n																	
t_{PHL}, t_{PLH} (2.8 ns/pF) C_L + 208 ns		5.0	–	–	–	250	375	–	–	–	–	–	250	620	–	–	
t_{PHL}, t_{PLH} (0.6 ns/pF) C_L + 111 ns		10	–	–	–	120	180	–	–	–	–	–	140	300	–	–	
t_{PHL}, t_{PLH} (0.25 ns/pF) C_L + 86 ns		15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	
Propagation Delay Time**	t_{PHL}, t_{PLH}																ns
(C_L = 15 pF) D_n to GS																	
t_{PHL}, t_{PLH} = (2.8 ns/pF) C_L + 183 ns		5.0	–	–	–	225	340	–	–	–	–	–	225	550	–	–	
t_{PHL}, t_{PLH} = (0.6 ns/pF) C_L + 91 ns		10	–	–	–	100	150	–	–	–	–	–	100	250	–	–	
t_{PHL}, t_{PLH} = (0.25 ns/pF) C_L + 66 ns		15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

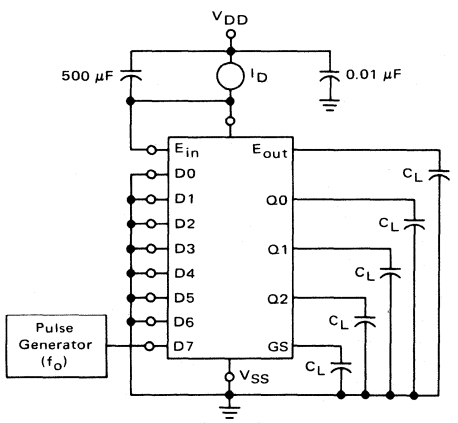
FIGURE 1 – TYPICAL SINK AND SOURCE CURRENT CHARACTERISTICS



Output Under Test	$V_{GS} = V_{DD}$, $V_{DS} = V_{out}$ Sink Current									$V_{GS} = -V_{DD}$, $V_{DS} = V_{out}-V_{DD}$ Source Current								
	D0	D1	D2	D3	D4	D5	D6	D7	E_{in}	D0	D1	D2	D3	D4	D5	D6	D7	E_{in}
E_{out}	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0	1
Q0	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1
Q1	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1
Q2	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1
GS	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	1	1

X = Don't Care

FIGURE 2 – TYPICAL POWER DISSIPATION TEST CIRCUIT



$P_D(C_L) = P_D + 5 \times 10^{-3} [C_L - 15] f_o V_{DD}^2$

Where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f_o in MHz.

LOGIC EQUATIONS

$E_{out} = E_{in} \bullet \overline{D0} \bullet \overline{D1} \bullet \overline{D2} \bullet \overline{D3} \bullet \overline{D4} \bullet \overline{D5} \bullet \overline{D6} \bullet \overline{D7}$

$Q0 = E_{in} \bullet (D1 \bullet \overline{D2} \bullet \overline{D4} \bullet \overline{D6} + D3 \bullet \overline{D4} \bullet \overline{D6} + D5 \bullet \overline{D6} + D7)$

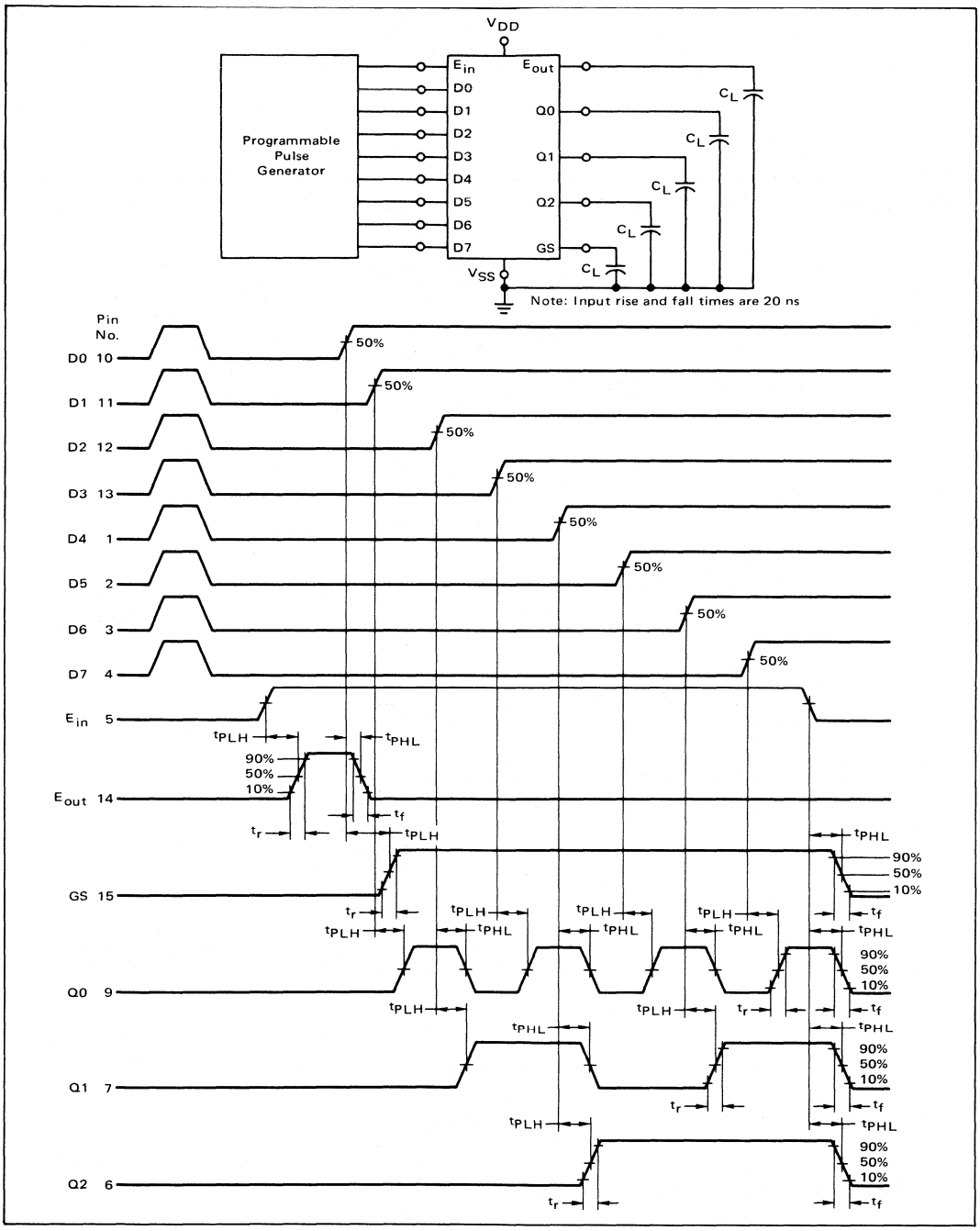
$Q1 = E_{in} \bullet (D2 \bullet \overline{D4} \bullet \overline{D5} + D3 \bullet \overline{D4} \bullet \overline{D5} + D6 + D7)$

$Q_2 = E_{in} \bullet (D4 + D5 + D6 + D7)$

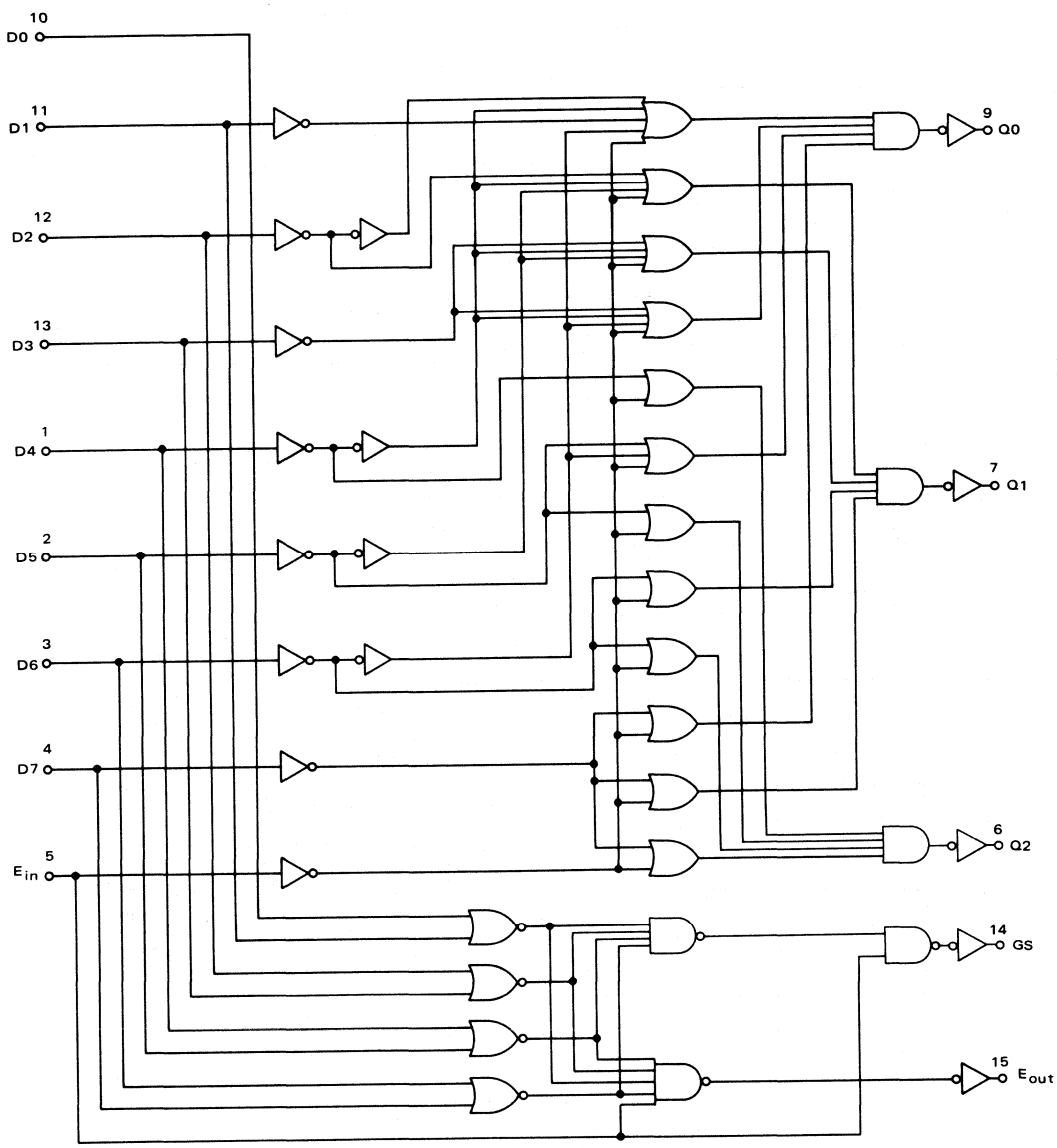
$GS = E_{in} \bullet (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$

7

FIGURE 3 – AC TEST CIRCUIT AND WAVEFORMS



LOGIC DIAGRAM
(Positive Logic)



APPLICATIONS INFORMATION

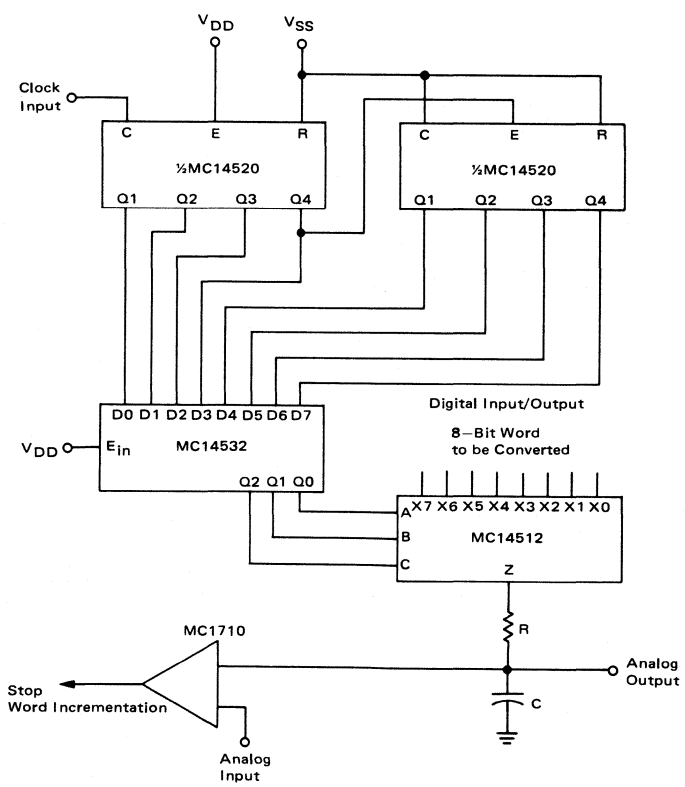
DIGITAL TO ANALOG CONVERSION

The digital eight-bit word to be converted is applied to the inputs of the MC14512 with the most significant bit at X7 and the least significant bit at X0. A clock input of up to 2.5 MHz (at V_{DD} = 10 V) is applied to the MC14520. A compromise between I_{bias} for the MC1710 and ΔR between N and P-channel outputs gives a value of R of 33 k ohms. In order to filter out the switching frequencies, RC should be about 1.0 ms (if R = 33 k ohms, C ≈ 0.03 μF). The analog 3.0 dB bandwidth would then be dc to 1.0 kHz.

ANALOG TO DIGITAL CONVERSION

An analog signal is applied to the analog input of the MC1710. A digital eight-bit word known to represent a digitized level less than the analog input is applied to the MC14512 as in the D to A conversion. The word is incremented at rates sufficient to allow steady state to be reached between incrementations (i.e. 3.0 ms). The output of the MC1710 will change when the digital input represents the first digitized level above the analog input. This word is the digital representation of the analog word.

DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTER



MC14539AL
MC14539CL
MC14539CP

DATA SELECTOR/MULTIPLEXER

Advance Information

DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER

The MC14539 data selector/multiplexer is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. The circuit consists of two sections of four inputs each. One input from each section is selected by the address inputs A and B. A "high" on the Strobe input will cause the output to remain "low".

This device finds primary application in signal multiplexing functions. It permits multiplexing from N-lines to l-line, and can also perform parallel-to-serial conversion. The Strobe input allows cascading of n-lines to n-lines.

- Quiescent Power Dissipation = 30 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- High Fanout – > 50
- Input Impedance = 10^{12} ohms typical

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	–MC14539AL –MC14539CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	–MC14539AL –MC14539CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLE

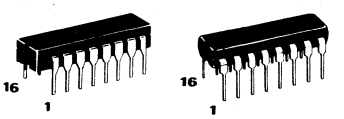
ADDRESS INPUTS		DATA INPUTS					
		X3	X2	X1	X0		OUTPUTS
B	A	Y3	Y2	Y1	Y0	ST,ST'	Z, W
X	X	X	X	X	X	1	0
0	0	X	X	X	0	0	0
0	0	X	X	X	1	0	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	0	1
1	0	X	0	X	X	0	0
1	0	X	1	X	X	0	1
1	1	0	X	X	X	0	0
1	1	1	X	X	X	0	1

X = Don't Care

McMOS

(LOW-POWER COMPLEMENTARY MOS)

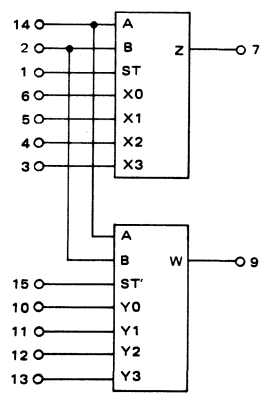
DUAL 4-CHANNEL DATA SELECTOR/MULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14539AL -55°C Min	MC14539AL -55°C Max	MC14539AL +25°C Min	MC14539AL +25°C Typ	MC14539AL +25°C Max	MC14539AL +125°C Min	MC14539AL +125°C Max	MC14539CL/CP -40°C Min	MC14539CL/CP -40°C Max	MC14539CL/CP +25°C Min	MC14539CL/CP +25°C Typ	MC14539CL/CP +25°C Max	MC14539CL/CP +85°C Min	MC14539CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)	–	V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.5	-1.7	–	-0.35	–	-0.23	–	-0.2	-1.7	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62		-0.5	-0.95	–	-0.35	–	-0.23	–	-0.2	-0.15	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.6	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.5	–	0.4	0.9	–	0.28	–	0.23	–	0.2	0.9	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	2.3	–	0.65	–	0.6	–	0.5	2.3	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	9.0	–	–	–	–	–	–	9.0	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)	–	C_{in}	–	–	–	–	5	–	–	–	–	–	–	5	–	–	–	pF
Quiescent Dissipation**†	1	P_D																mW
(C_L = 15 pF, f = 0 MHz)																		
P_D = (2.5 mW/MHz) f + 0.0003 mW			5.0	–	–	–	0.00003	0.025	–	–	–	–	–	0.00003	0.25	–	–	
P_D = (10 mW/MHz) f + 0.00010 mW			10	–	–	–	0.00010	0.1	–	–	–	–	–	0.00010	1.0	–	–	
P_D = (27 mW/MHz) f + 0.00025 mW			15	–	–	–	0.00025	–	–	–	–	–	–	0.00025	–	–	–	
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 35 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_r = (1.5 ns/pF) C_L + 17 ns			10	–	–	–	40	75	–	–	–	–	–	40	110	–	–	
t_r = (1.0 ns/pF) C_L + 15 ns			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 57 ns			5.0	–	–	–	80	175	–	–	–	–	–	80	200	–	–	
t_f = (0.7 ns/pF) C_L + 30 ns			10	–	–	–	40	75	–	–	–	–	–	40	110	–	–	
t_f = (0.5 ns/pF) C_L + 23 ns			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Turn-On Delay Time**	2	t_{PHL}																ns
X, Y, Input to Output																		
(C_L = 15 pF)																		
t_{PHL} = (1.6 ns/pF) C_L + 156 ns			5.0	–	–	–	180	360	–	–	–	–	–	180	540	–	–	
t_{PHL} = (0.6 ns/pF) C_L + 66 ns			10	–	–	–	75	150	–	–	–	–	–	75	225	–	–	
t_{PHL} = (0.45 ns/pF) C_L + 53 ns			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Turn-Off Delay Time**	2	t_{PLH}																ns
X, Y Input to Output																		
(C_L = 15 pF)																		
t_{PLH} = (1.6 ns/pF) C_L + 126 ns			5.0	–	–	–	150	300	–	–	–	–	–	150	450	–	–	
t_{PLH} = (0.6 ns/pF) C_L + 56 ns			10	–	–	–	65	130	–	–	–	–	–	65	195	–	–	
t_{PLH} = (0.45 ns/pF) C_L + 43 ns			15	–	–	–	50	–	–	–	–	–	–	50	–	–	–	
Turn-On Delay Time**	2	t_{PHL}																ns
A Input to Output																		
(C_L = 15 pF)																		
t_{PHL} = (1.5 ns/pF) C_L + 192 ns			5.0	–	–	–	215	430	–	–	–	–	–	215	645	–	–	
t_{PHL} = (0.6 ns/pF) C_L + 86 ns			10	–	–	–	95	190	–	–	–	–	–	95	285	–	–	
t_{PHL} = (0.45 ns/pF) C_L + 63 ns			15	–	–	–	70	–	–	–	–	–	–	70	–	–	–	
Turn-Off Delay Time**	2	t_{PLH}																ns
A Input to Output																		
(C_L = 15 pF)																		
t_{PLH} = (1.5 ns/pF) C_L + 147 ns			5.0	–	–	–	170	340	–	–	–	–	–	170	510	–	–	
t_{PLH} = (0.6 ns/pF) C_L + 71 ns			10	–	–	–	80	160	–	–	–	–	–	80	240	–	–	
t_{PLH} = (0.45 ns/pF) C_L + 58 ns			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Turn-On Delay Time**	2	t_{PHL}																ns
ST Input to Output																		
(C_L = 15 pF)																		
t_{PHL} = (1.5 ns/pF) C_L + 68 ns			5.0	–	–	–	90	180	–	–	–	–	–	90	270	–	–	
t_{PHL} = (0.7 ns/pF) C_L + 35 ns			10	–	–	–	45	90	–	–	–	–	–	45	135	–	–	
t_{PHL} = (0.5 ns/pF) C_L + 32 ns			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Turn-Off Delay Time**	2	t_{PLH}																ns
t_{PLH} = (1.5 ns/pF) C_L + 68 ns			5.0	–	–	–	90	180	–	–	–	–	–	90	270	–	–	
t_{PLH} = (0.7 ns/pF) C_L + 35 ns			10	–	–	–	45	90	–	–	–	–	–	45	135	–	–	
t_{PLH} = (0.5 ns/pF) C_L + 32 ns			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refer to corresponding formula:

$$P_D(C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}{}^2 f$$

FIGURE 1 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

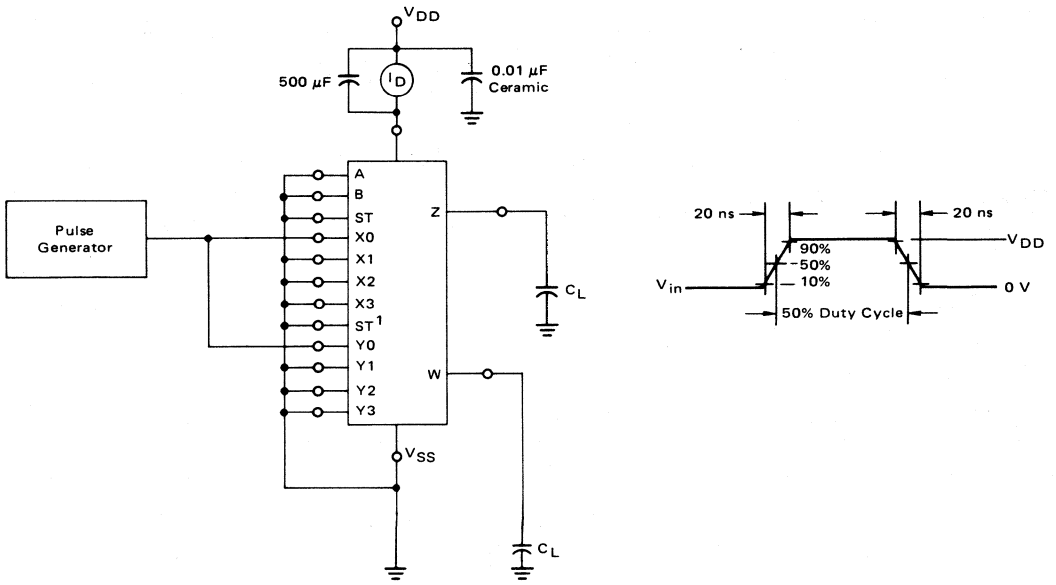
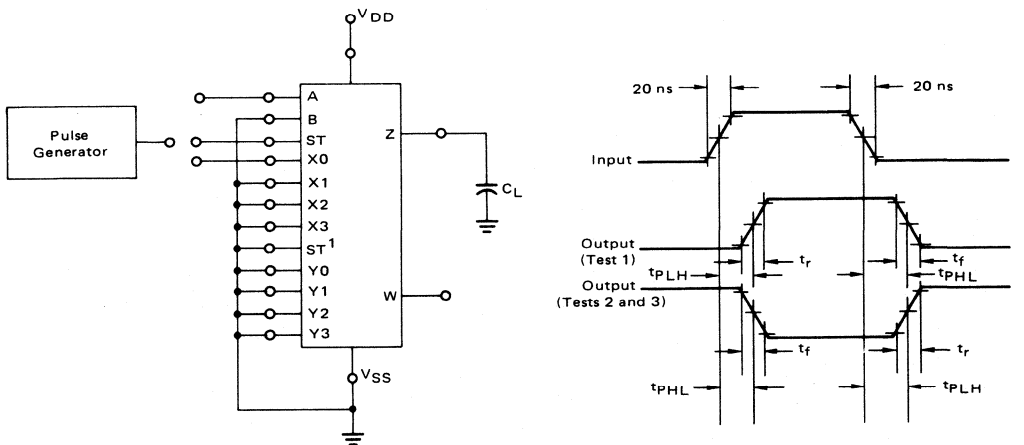


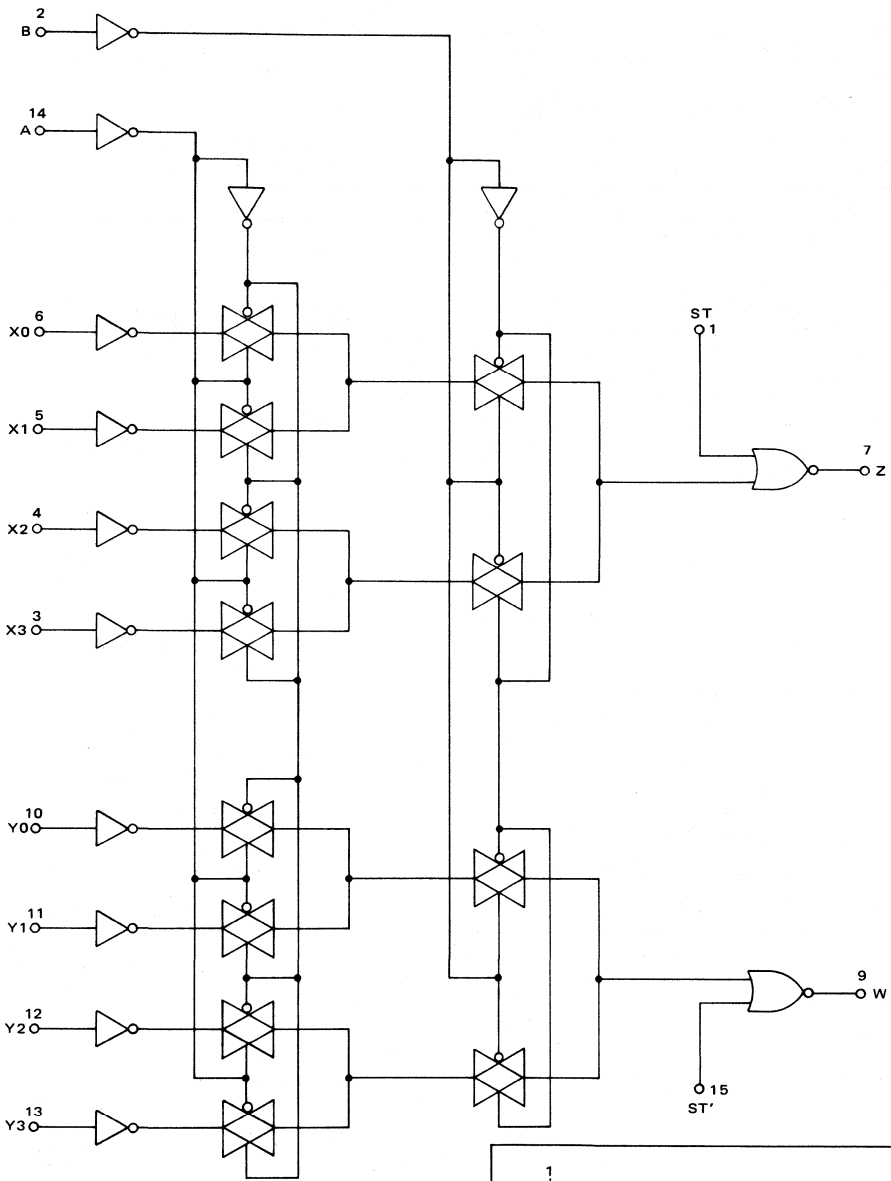
FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS

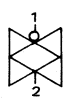


Input Connections for t_r, t_f, t_{PLH}, T_{PHL}

TEST	STROBE	A	X0
1	Gnd	Gnd	P. G
2	P. G.	Gnd	V_{DD}
3	Gnd	P. G.	V_{DD}

LOGIC DIAGRAM





Transmission Gate

Input to Output is:

a) A bidirectional low impedance when control input 1 is a logic "0" and control input 2 is logic "1".

b) An open circuit is when control input 1 is a logic "1" and control input 2 is a logic "0".

MC14543AL
MC14543CL
MC14543CP

LATCH/DECODER/DRIVER

Advance Information

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS

The MC14543 BCD-to-seven segment latch/decoder/driver is designed for use with liquid crystal readouts, and is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD -to-seven segment decoder and driver. The device has the capability to invert the logic levels of the output combinations. The phase (Ph) blanking (BI), and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display. The outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

Applications include instrument (e.g., counter, DVM etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Logic Circuit Quiescent Power Dissipation = 25nW/package typical
- Latch Storage of Code
- Blanking Input
- Readout Blanking on All Illegal Input Combinations
- Direct LED (Common Anode or Cathode) Driving Capability
- Pin-for-Pin Replacement for CD4056A (with Pin 7 Tied to V_{SS}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage –MC14543AL MC14543CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin, All Data Inputs	I	10	mAdc
Operating Temperature Range MC14543AL MC14543CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Drive Current (Source or Sink) per Output	I_{OHmax} I_{OLmax}	10	mAdc
Maximum Continuous Output Power* (Source or Sink) per Output	P_{OHmax} P_{OLmax}	70	mW

*$P_{OHmax} = I_{OH}(V_{OH} - V_{DD})$ and $P_{OLmax} = I_{OL}(V_{OL} - V_{SS})$

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended than V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

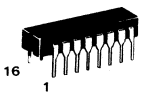
This is advance information and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

McMOS

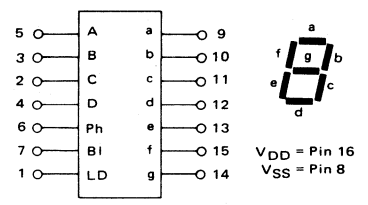
(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT LATCH/DECODER/DRIVER for LIQUID CRYSTALS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



TRUTH TABLE

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X				**				**
†	†	1			†		Inverse of Output Combinations Above							Display as above

X = Don't care
† = Above Combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code applied during the 1 to 0 transition of LD.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD}	MC14543AL							MC14543CL/CP							Unit
				-55°C		-25°C			+125°C		-40°C		+25°C			+85°C		
			Vdc	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
($V_{out} \geq 3.5$ Vdc)	–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.50	-1.9	–	-0.35	–	-0.23	–	-0.20	-1.9	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-1.0	–	-0.35	–	-0.23	–	-0.20	-1.0	–	-0.16	–	
(V_{OH} = 0.5 Vdc)			10	–	–	–	-9.7	–	–	–	–	–	–	-9.7	–	–	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.9	–	–	–	–	–	–	-3.9	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 9.5 Vdc)			10	–	–	–	11.4	–	–	–	–	–	–	11.4	–	–	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance	–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation**†	–	P_D																mW
(C_L = 15 pF, f = 0 MHz)	3																	
P_D = (4.8 mW/MHz) f + 0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (19 mW/MHz) f + 0.00010 mW			10	–	0.10	–	0.00010	0.10	–	6.0	–	1.0	–	0.00010	1.0	–	14	
P_D = (43 mW/MHz) f + 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	4a	t_r																ns
(CL = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	4a	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pG) C_L + 17ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time**	4a	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (1.65 ns/pF) C_L + 525 ns			5.0	–	–	–	550	1100	–	–	–	–	–	550	1650	–	–	
t_{PLH} = (0.65 ns/pF) C_L + 210 ns			10	–	–	–	220	440	–	–	–	–	–	220	660	–	–	
t_{PLH} = (0.49 ns/pF) C_L + 158 ns			15	–	–	–	165	–	–	–	–	–	–	165	–	–	–	
Turn-On delay Time**	4a	t_{PHL}																ns
(C_L = 15pF)																		
t_{PHL} = (1.65 ns/pF) C_L + 450 ns			5.0	–	–	–	475	1100	–	–	–	–	–	475	1650	–	–	
t_{PHL} = (0.65 ns/pF) C_L + 180 ns			10	–	–	–	190	440	–	–	–	–	–	190	660	–	–	
t_{PHL} = (0.49 ns/pF) C_L + 138 ns			15	–	–	–	145	–	–	–	–	–	–	145	–	–	–	
Minimum Setup Time	4b	t_{setup}																ns
			5.0	–	–	–	40	80	–	–	–	–	–	40	120	–	–	
			10	–	–	–	15	30	–	–	–	–	–	15	45	–	–	
			15	–	–	–	10	–	–	–	–	–	–	10	–	–	–	
Minimum Hold Time	4b	t_{hold}																ns
			5.0	–	–	–	-40	0	–	–	–	–	–	-40	80	–	–	
			10	–	–	–	-15	0	–	–	–	–	–	-15	30	–	–	
			15	–	–	–	-10	–	–	–	–	–	–	-10	–	–	–	
Minimum Latch Disable Pulse Width (Strobing Data)	4c	PW_{LD}																ns
			5.0	–	–	–	125	250	–	–	–	–	–	125	375	–	–	
			10	–	–	–	50	100	–	–	–	–	–	50	150	–	–	
			15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances refer to corresponding formula:

$$P_D(C_L) = P_D + \frac{7}{2} \times 10^{-3}(C_L - 15pF)\ V_{DD}{}^2 f$$

with P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz

FIGURE 1 – TYPICAL OUTPUT SOURCE CHARACTERISTICS

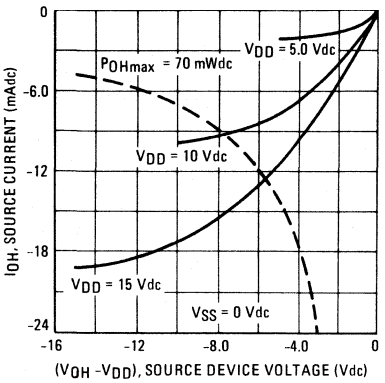
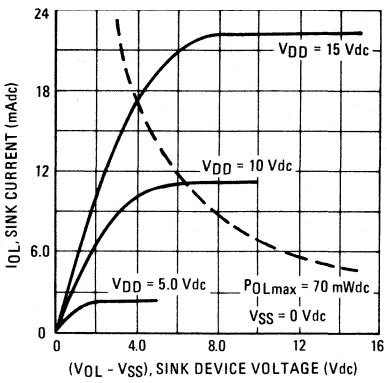
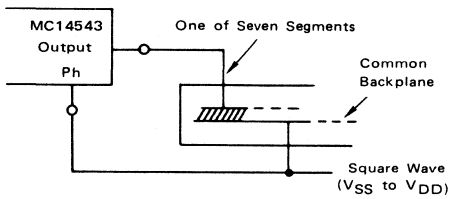


FIGURE 2 – TYPICAL OUTPUT SINK CHARACTERISTICS

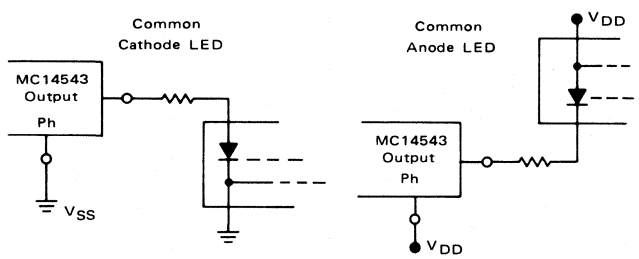


CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIQUID CRYSTAL (LC) READOUT

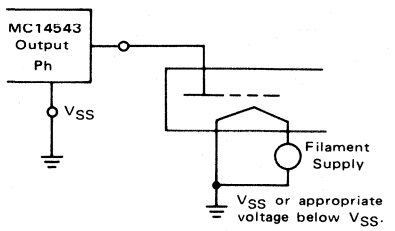


LIGHT EMITTING DIODE (LED) READOUT

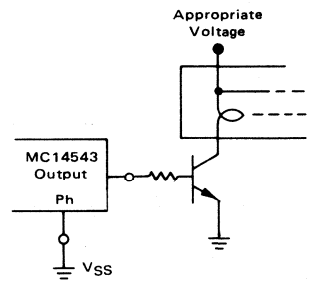


Note: Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{out} \geq 10$ mA).

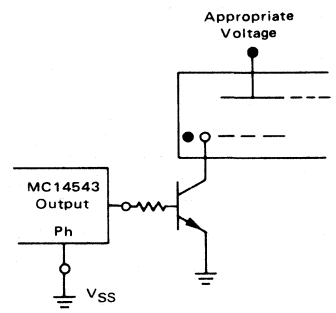
FLUORESCENT READOUT



INCANDESCENT READOUT



GAS DISCHARGE READOUT



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LOGIC DIAGRAM

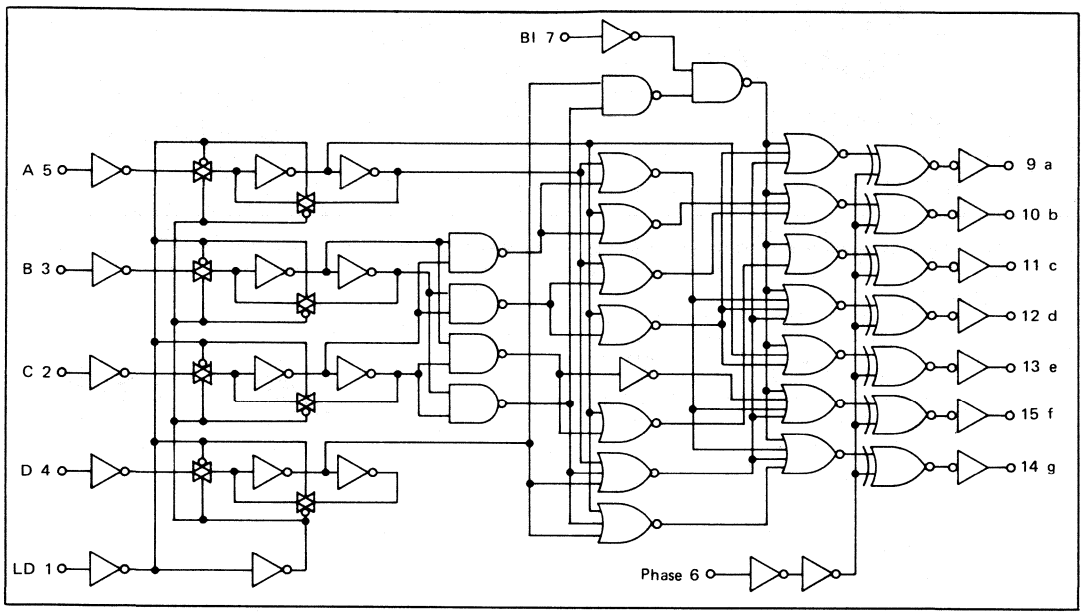


FIGURE 3 – DYNAMIC POWER DISIPATION SIGNAL WAVEFORMS

Inputs BI and Ph low, and Inputs D and LD high.
f in respect to a system clock.

All outputs connected to respective C_L loads.

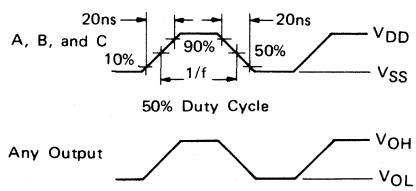
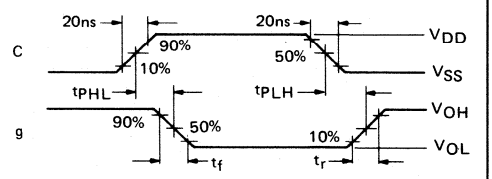
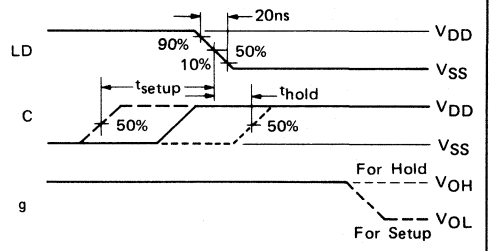


FIGURE 4 – DYNAMIC SIGNAL WAVEFORMS

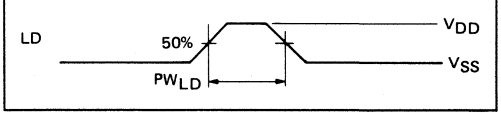
(a) Inputs D, Ph, and BI low, and Inputs A, B, and LD high.



(b) Inputs D, Ph, and BI low, and Inputs A and B high.



(c) Data DCBA strobed into latches



7

MC14549AL
MC14549CL
MC14549CP
MC14559AL
MC14559CL
MC14559CP

SUCCESSIVE APPROXIMATION REGISTERS

Advance Information

SUCCESSIVE APPROXIMATION REGISTERS

The MC14549 and MC14559 successive approximation registers are 8-bit registers providing all the digital control and storage necessary for successive approximation analog-to-digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549 is required in the cascaded mode when greater than 8 bits are desired. The Feed Forward (FF) of the MC14559 is used for register shortening where End-of-Conversion (EOC) is required after less than eight cycles.

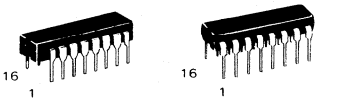
Applications for the MC14549 and MC14559 include finding square roots, division, ring counters, serial-to-parallel conversion, and analog-to-digital conversion.

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8-Bit D/A Converter
- All Control Inputs Positive-Edge Triggered

McMOS

(LOW-POWER COMPLIMENTARY MOS)

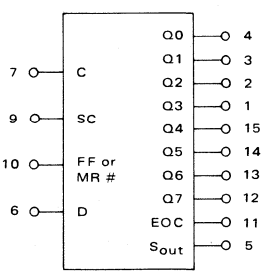
SUCCESSIVE APPROXIMATION REGISTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

#For MC14549 Pin 10 is MR input
For MC14559 Pin 10 is FF input

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating		Symbol	Value	Unit
DC Supply Voltage	AL Version CL,CP Version	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	AL Version CL,CP Version	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

TRUTH TABLES

MC14549

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	⌐¬	None
X	X	1	X	⌐¬	Reset
1	0	0	0	⌐¬	Start Conversion
1	X	0	1	⌐¬	Start Conversion
1	1	0	0	⌐¬	Continue Conversion
0	X	0	X	⌐¬	Continue Previous Operation

MC14559

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	⌐¬	None
1	0	0	⌐¬	Start Conversion
X	1	0	⌐¬	Continue Conversion
0	0	0	⌐¬	Continue Conversion
0	X	1	⌐¬	Retain Conversion Result
1	X	1	⌐¬	Start Conversion

X = Don't Care
t-1 = Stage at Previous Clock ⌐¬

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	MC14549AL/MC14559AL							MC14549CL,CP/MC14559CL,CP							Unit
			-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
		15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
	V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)		5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
	I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	1.0	–	0.80	1.56	–	0.56	–	0.46	–	0.40	1.56	–	0.32	–	
(V_{OL} = 0.5 Vdc) (Q Outputs)		10	2.2	–	1.80	4.0	–	1.30	–	1.20	–	1.0	4.0	–	0.80	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	15.6	–	–	–	–	–	–	15.6	–	–	–	
	I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc) (All other Outputs)		10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation (C_L = 15 pF, f = 0 Hz)	P_Q																mW
		5.0	–	0.5	–	0.10	0.5	–	300	–	0.5	–	0.10	0.5	–	7.0	
		10	–	2.0	–	0.50	2.0	–	120	–	2.0	–	0.50	2.0	–	28	
		15	–	–	–	2.0	–	–	–	–	–	–	2.0	–	–	–	
Dynamic Power Dissipation (C_L = 15 pF) (Typical)	P_D																mW
		5.0	P_D = (3.0 mW/MHz) f + 0.1 mW														
		10	P_D = (12 mW/MHz) f + 0.5 mW														
		15	P_D = (27 mW/MHz) f + 2.0 mW														
Output Rise Time** (C_L = 15 pF)	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns		5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns		10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns		15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time** (C_L = 15 pF)	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns		5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns		10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns		15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	

(Continued on next page)

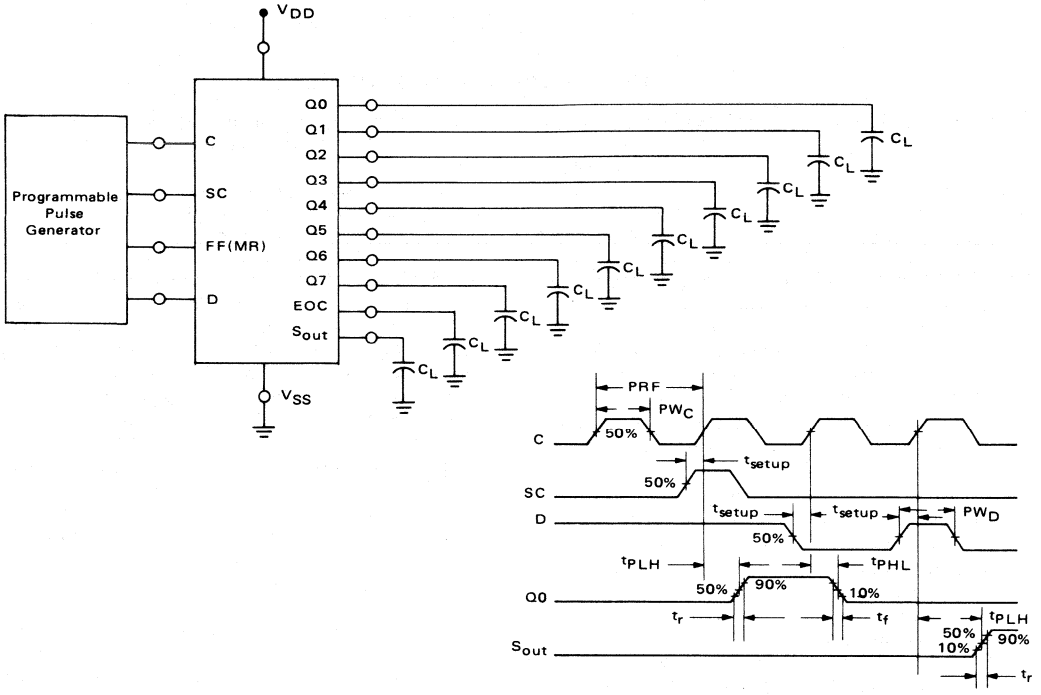
ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	V_{DD} Vdc	MC14549AL/MC14559AL							MC14549CL,CP/MC14559CL,CP							Unit
			-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Clock Turn-Off, Turn-On Delay Time** (C_L = 15 pF) To Q Output	t_{PLH}, t_{PHL}																ns
t_{PLH},t_{PHL} = (1.8 ns/pF) C_L + 423 ns		5.0	–	–	–	450	700	–	–	–	–	–	450	1100	–	–	
t_{PLH},t_{PHL} = (0.8 ns/pF) C_L + 168 ns		10	–	–	–	180	250	–	–	–	–	–	180	450	–	–	
t_{PLH},t_{PHL} = (0.6 ns/pF) C_L + 126 ns		15	–	–	–	135	–	–	–	–	–	–	135	–	–	–	
Clock Turn-Off, Turn-On Delay Time** (C_L = 15 pF) (To Serial Out)	t_{PLH}, t_{PHL}																ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 424 ns		5.0	–	–	–	450	700	–	–	–	–	–	450	1100	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 169 ns		10	–	–	–	180	250	–	–	–	–	–	180	450	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 127 ns		15	–	–	–	135	–	–	–	–	–	–	135	–	–	–	
Clock Turn-Off, Turn-On Delay Time** (C_L = 15 pF) (To EOC)	t_{PLH}, t_{PHL}																ns
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 224 ns		5.0	–	–	–	250	350	–	–	–	–	–	250	750	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 89 ns		10	–	–	–	100	150	–	–	–	–	–	100	300	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 72 ns		15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
SC,D, and MR Setup Time (C_L = 15 pF)	t_{setup}																ns
		5.0	–	–	–	125	175	–	–	–	–	–	125	300	–	–	
		10	–	–	–	50	75	–	–	–	–	–	50	150	–	–	
		15	–	–	–	40	–	–	–	–	–	–	40	–	–	–	
Minimum Clock Pulse Width (C_L = 15 pF)	PW_C																ns
		5.0	–	–	–	350	500	–	–	–	–	–	350	600	–	–	
		10	–	–	–	135	200	–	–	–	–	–	135	300	–	–	
		15	–	–	–	100	–	–	–	–	–	–	100	–	–	–	
Minimum Pulse Width (C_L = 15 pF) (D,SC,FF or MR)	PW																ns
		5.0	–	–	–	250	375	–	–	–	–	–	250	750	–	–	
		10	–	–	–	100	150	–	–	–	–	–	100	300	–	–	
		15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	
Maximum Clock Rise and Fall Time	t_r,t_f																μs
		5.0	–	–	–	–	15	–	–	–	–	–	–	15	–	–	
		10	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	
Maximum Clock Pulse Frequency (C_L = 15 pF)	PRF																MHz
		5.0	–	–	1.0	1.5	–	–	–	–	–	0.8	1.5	–	–	–	
		10	–	–	2.0	3.0	–	–	–	–	–	1.5	3.0	–	–	–	
		15	–	–	–	4.0	–	–	–	–	–	–	4.0	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

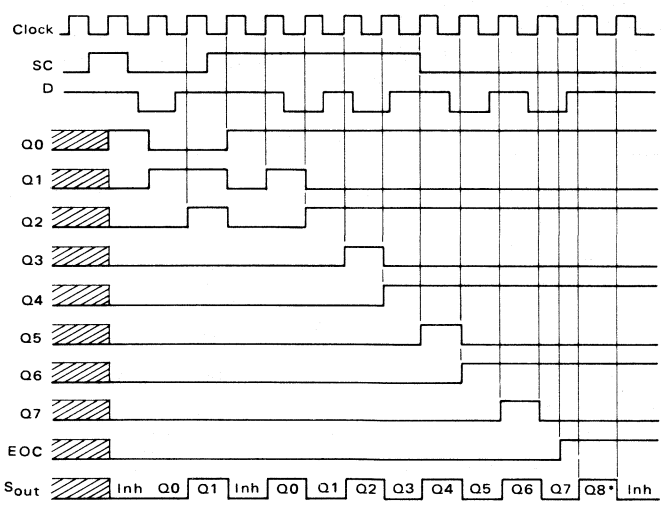
**The formula given is for the typical characteristics only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



Note: Pin 10 = V_{SS}

TIMING DIAGRAM



– Don't care condition

Inh – Indicates Serial Out is inhibited low.

* – Q8 is ninth-bit of serial information available from 8-bit register.

Note: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549 and MC14559 can be operated in either the "free run" or "strobed operation" mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549 but either 1 or 0 for MC14559) no stable state exists under continual clocked operation. The MC14559 will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock – A positive-going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert – A conversion sequence is initiated on the positive-going transition of the SC input on succeeding clock cycles.

D = Data In – Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive-going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed equality of serial and parallel data.

MR = Master Reset (MC14549 only) – Resets all output to 0 on positive-going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559 only) – Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6-bit conversion, tie Q6 to FF; the part will respond as shown in the timing diagram less two bit times. Note that Q6 and Q7 will still operate and must be disregarded.

For 8-bit operation, FF is tied to V_{SS}.

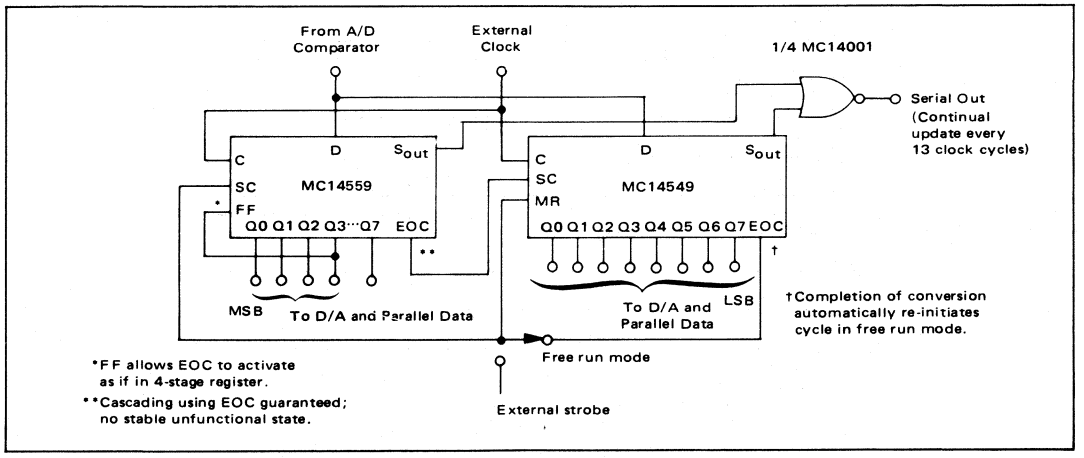
For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559 is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559 allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559 to the MC14549. The Serial Out (S_{out}) inhibit structure of the MC14559 remains inactive one cycle after EOC goes high, while S_{out} of the MC14549 remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs – After a conversion is initiated the Q's on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert – This output goes high on the negative-going transition of the clock following FF = 1 (for the MC14559) or the conditional reset of Q7. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out – Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.

FIGURE 1 – 12-BIT CONVERSION SCHEME



MC14554AL
MC14554CL
MC14554CP

BINARY MULTIPLIER

Advance Information

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER

The MC14554 2 x 2-bit parallel binary multiplier is constructed with complementary MOS (CMOS) enhancement mode devices. The multiplier can perform the multiplication of two binary numbers and simultaneously add two other binary numbers to the product. The MC14554 has two multiplicand inputs (X0 and X1), two multiplier inputs (Y0 and Y1), five cascading or adding inputs (K0, K1, M0, M1, and M2), and five sum and carry outputs (S0, S1, S2, C1 [S3], and C0). The basic multiplier can be expanded into a straight-forward m-bit by n-bit parallel multiplier without additional logic elements.

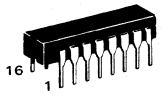
Application areas include arithmetic processing (multiplying/adding, obtaining square roots, polynomial evaluation, obtaining reciprocals, and dividing), Fast Fourier Transform processing, digital filtering, communications (convolution and correlation), and process and machine controls.

- Diode Protection on All Inputs
- Buffered Outputs Compatible with HTL and Low Power TTL
- Low Quiescent Power Dissipation — 25 nW typical
- Straightforward m-Bit By n-Bit Expansion
- No Additional Logic Elements Needed for Expansion
- Multiplies and Adds Simultaneously
- Positive Logic Design

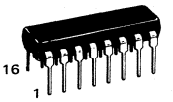
McMOS

(LOW-POWER COMPLEMENTARY MOS)

2-BIT BY 2-BIT PARALLEL BINARY MULTIPLIER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

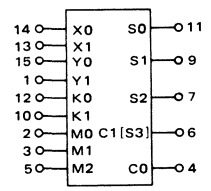
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14554AL — MC14554CL/CP	V_{DD}	+18 to −0.5 +16 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to −0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14554AL — MC14554CL/CP	T_A	 −55 to +125 −40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

EQUATIONS

S = (X x Y) + K + M
Where:
x Means Arithmetic Times.
+ Means Arithmetic Plus.
S = S3 S2 S1 S0, X = X1X0, Y = Y1Y0,
K = K1 K0, M = M1 M0 (Binary Numbers).
Example:
Given: X = 2(10), Y = 3(11)
K = 1(01), M = 2(10)
Then: S = (2 x 3) + 1 + 2 = 9
S = (10 x 11) + 01 + 10 = 1001
Note: C0 connected to M2 for this size multiplier.
See general expansion diagram for other size multipliers.

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14554AL							MC14554CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*		V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source	–	I_{OH}	5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
																		mAdc
(V_{OL} = 0.4 Vdc) Sink	–	I_{OL}	5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	–	P_Q																mW
			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
			10	–	0.10	–	0.00010	0.10	–	6.0	–	1.0	–	0.00010	1.0	–	14	
			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Total Power Dissipation**† (Dynamic plus Quiescent) (C_L = 15 pF)	1	P_T	5.0	$P_T = (1.9\ mW/MHz)\ f + 0.000025\ mW$														mW
			10	$P_T = (7.5\ mW/MHz)\ f + 0.00010\ mW$														
			15	$P_T = (17\ mW/MHz)\ f + 0.00023\ mW$														

(Continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14554AL							MC14554CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Rise Time** (C_L = 15 pF)	2	t_r																ns
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time ** (C_L = 15 pF)	2	t_f																ns
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time (K0 to C0)** (C_L = 15 pF)	2	t_{PLH}																ns
t_{PLH} = (1.7 ns/pF) C_L + 175 ns			5.0	–	–	–	200	430	–	–	–	–	–	200	645	–	–	
t_{PLH} = (0.67 ns/pF) C_L + 70 ns			10	–	–	–	80	170	–	–	–	–	–	80	255	–	–	
t_{PLH} = (0.50 ns/pF) C_L + 52 ns			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
Turn-On Delay Time (K0 to C0)** (C_L = 15 pF)	2	t_{PHL}																ns
t_{PHL} = (1.7 ns/pF) C_L + 190 ns			5.0	–	–	–	215	430	–	–	–	–	–	215	645	–	–	
t_{PHL} = (0.67 ns/pF) C_L + 75 ns			10	–	–	–	85	170	–	–	–	–	–	85	255	–	–	
t_{PHL} = (0.50 ns/pF) C_L + 57 ns			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Turn-Off Delay Time (M0 to S2)** (C_L = 15 pF)	2	t_{PLH}																ns
t_{PLH} = (1.7 ns/pF) C_L + 525 ns			5.0	–	–	–	550	1250	–	–	–	–	–	550	1875	–	–	
t_{PLH} = (0.67 ns/pF) C_L + 210 ns			10	–	–	–	220	500	–	–	–	–	–	220	750	–	–	
t_{PLH} = (0.50 ns/pF) C_L + 157 ns			15	–	–	–	165	–	–	–	–	–	–	165	–	–	–	
Turn-On Delay Time (M0 to S2)** (C_L = 15 pF)	2	t_{PHL}																ns
t_{PHL} = (1.7 ns/pF) C_L + 600 ns			5.0	–	–	–	625	1250	–	–	–	–	–	625	1875	–	–	
t_{PHL} = (0.67 ns/pF) C_L + 240 ns			10	–	–	–	250	500	–	–	–	–	–	250	750	–	–	
t_{PHL} = (0.50 ns/pF) C_L + 182 ns			15	–	–	–	190	–	–	–	–	–	–	190	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change for an ideal "1" or "0" input level before producing an output state change.
**The formula given is for the typical characteristics only.
†For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$$P_T(C_L) = P_T + \frac{5}{2} \times 10^{-3} (C_L - 15\ pF)\ V_{DD}{}^2 f$$

Where: P_T in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

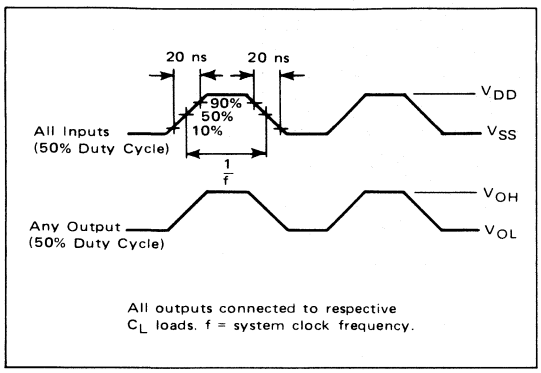
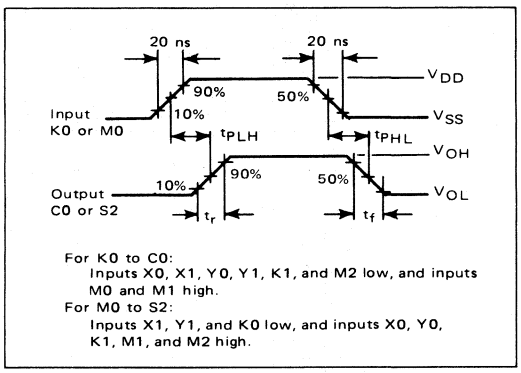
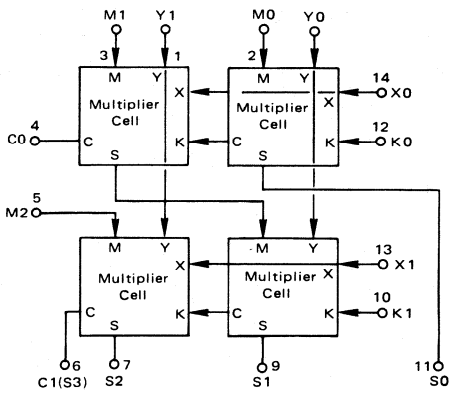
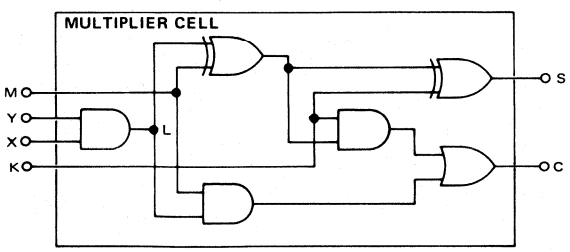


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS



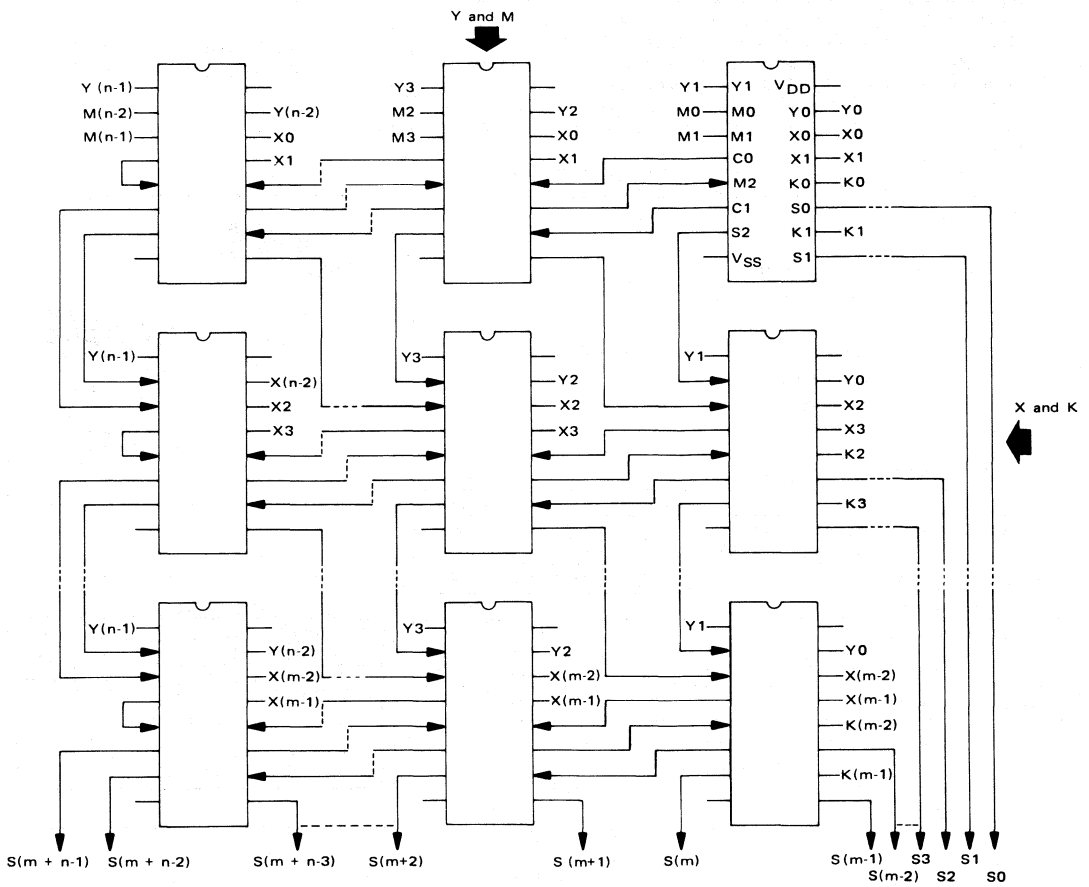
LOGIC DIAGRAM





EXPANSION DIAGRAM

m-Bit by n-Bit Parallel Binary Multiplier (Top View)



S = (X x Y) + K + M Where: x means Arithmetic Times.
+ means Arithmetic Plus.

S = S(m + n-1) S(m + n-2) - - - S2 S1 S0
X = X(m-1) X (m-2) - - - X2 X1 X0, Y = Y(n-1) Y(n-2) - - - Y2 Y1 Y0
K = K(m-1) K(m-2) - - - K2 K1 K0 and M = M(n-1) M(n-2) - - - M2 M1 M0
(Binary Numbers).

Number of output binary digits = m + n
Number of packages = mxn/4 (For m or n or both odd select next highest even number.)

MC14555AL
MC14555CL
MC14555CP
MC14556AL
MC14556CL
MC14556CP

DECODER/DEMULTIPLEXER

Advance Information

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER

The MC14555 and MC14556 are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input ($\overline{E}$), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555 (active high outputs) has the selected output go to the "high" state, and the MC14556 (active low outputs) has the selected output go to the "low" state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555 or MC14556 devices.

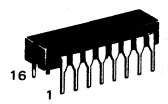
Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} Typical
- High Fanout – > 50
- Buffered Outputs Compatible With HTL and Low-Power TTL
- Active High or Active Low Outputs
- Low Quiescent Power Dissipation – 25 nW Typical
- Expandable

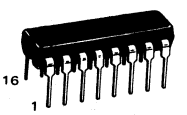
McMOS

(LOW-POWER COMPLEMENTARY MOS)

DUAL BINARY TO 1-OF-4 DECODER/DEMULTIPLEXER



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

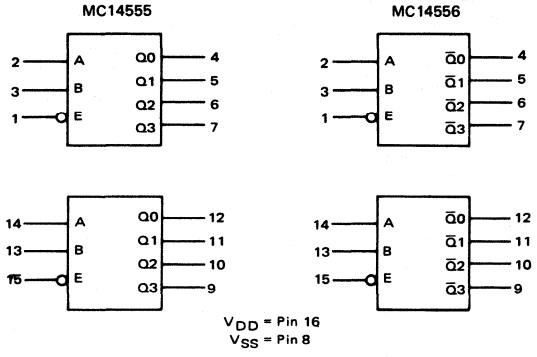
Rating	Symbol	Value	Unit
DC Supply Voltage – MC14555AL/556AL – MC14555CL,CP/556CL,CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range– MC14555AL/556AL MC14555CL,CP/556CL,CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS			OUTPUTS MC14555				OUTPUTS MC14556			
ENABLE	SELECT									
$\overline{E}$	B	A	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} or V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

7

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14555AL, MC14556AL −55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC14555CL/CP, MC14556CL/CP −40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level	–		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.95	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
($V_{out} \geq 3.5$ Vdc)			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
($V_{out} \leq 1.5$ Vdc)			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current		I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source			5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
		I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink			5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10^{-5}	–	–	–	pAdc
Input Capacitance, V_{in} = 0 Vdc	–	C_{in}	–	–	–	–	5	–	–	–	–	–	–	5	–	–	–	pF
Quiescent Dissipation **†	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (2.5 mW/MHz) f + 0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (10 mW/MHz) f + 0.00010 mW			10	–	0.10	–	0.00010	0.10	–	6.0	–	1.0	–	0.00010	1.0	–	1.4	
P_D = (23 mW/MHz) f + 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	2,3	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2,3	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
	MC14555AL										MC14555CL/CP							
Turn-Off, Turn-On Delay Time**	2	t_{PLH}, t_{PHL}																ns
(C_L = 15 pF)																		
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 174 ns			5.0	–	–	–	200	400	–	–	–	–	–	200	600	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 69 ns			10	–	–	–	80	160	–	–	–	–	–	80	240	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 52 ns			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	
	MC14556AL										MC14556CL/CP							
Turn-Off, Turn-On Delay Time	3	t_{PLH}, t_{PHL}																ns
(C_L = 15 pF)																		
t_{PLH},t_{PHL} = (1.75 ns/pF) C_L + 199 ns			5.0	–	–	–	225	450	–	–	–	–	–	225	675	–	–	
t_{PLH},t_{PHL} = (0.70 ns/pF) C_L + 79 ns			10	–	–	–	90	180	–	–	–	–	–	90	270	–	–	
t_{PLH},t_{PHL} = (0.53 ns/pF) C_L + 60 ns			15	–	–	–	68	–	–	–	–	–	–	68	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external Load Capacitance (C_L) refer to corresponding formula:

$P_D (C_L) = P_D + 2 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$

where: P_D in mW, C_L in pF, V_{DD} in Vdc, and f in MHz.

LOGIC DIAGRAM
(1/2 of Dual)

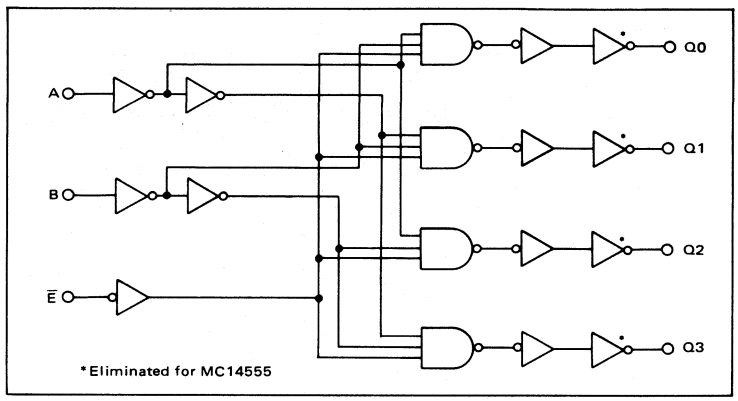


FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS

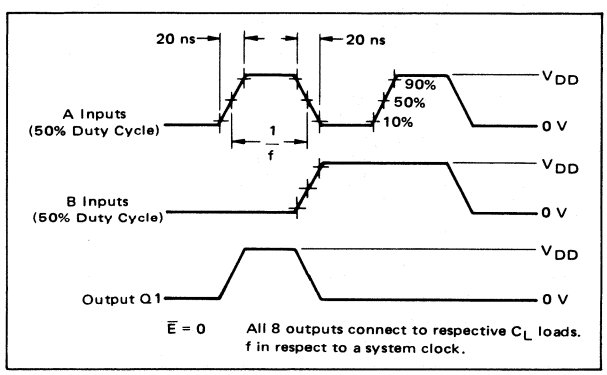


FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS
(MC14555)

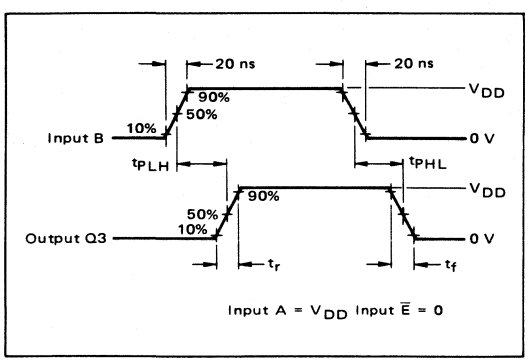
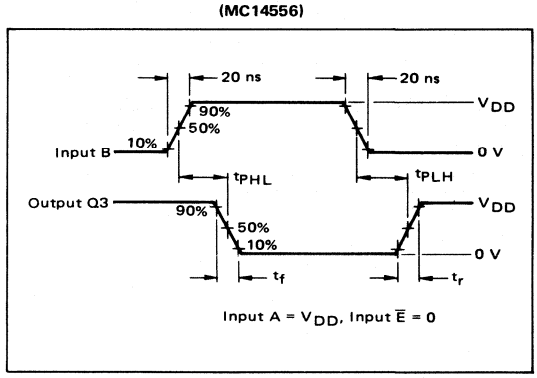


FIGURE 3 – DYNAMIC SIGNAL WAVEFORMS
(MC14556)



7

MC14570AL
MC14570CL
MC14570CP

QUAD 2-INPUT "OR" GATE

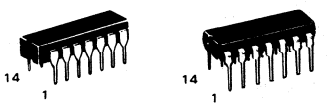
The MC14570 quad 2-input OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 6.0 nW/package typical @ V_{DD} = 5.0 V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14570AL)
  = 3.0 Vdc to 16 Vdc (MC14570CL/CP)
- Single Supply Operation – Positive or Negative
- High Fanout > 50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

McMOS

(LOW-POWER COMPLEMENTARY MOS)

QUAD 2-INPUT "OR" GATE



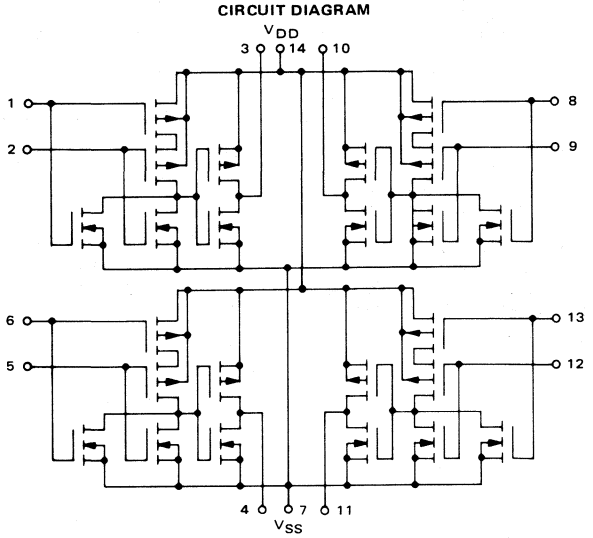
L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

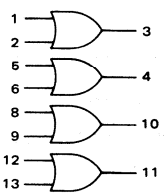
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage – MC14570AL – MC14570CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – MC14570AL – MC14570CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

CIRCUIT DIAGRAM



LOGIC DIAGRAM



3 = 1 + 2

V_{DD} = Pin 14
V_{SS} = Pin 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	MC14570AL -55°C Min	MC14570AL -55°C Max	MC14570AL +25°C Min	MC14570AL +25°C Typ	MC14570AL +25°C Max	MC14570AL +125°C Min	MC14570AL +125°C Max	MC14570CL/CP -40°C Min	MC14570CL/CP -40°C Max	MC14570CL/CP +25°C Min	MC14570CL/CP +25°C Typ	MC14570CL/CP +25°C Max	MC14570CL/CP +85°C Min	MC14570CL/CP +85°C Max	Unit
Output Voltage "0" Level	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
		10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
		15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level		5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
		10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
		15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	V_{NL}																Vdc
($V_{out} \leq 1.5$ Vdc)		5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \leq 3.0$ Vdc)		10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
($V_{out} \leq 4.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
	V_{NH}																Vdc
($V_{out} \geq 3.5$ Vdc)		5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
($V_{out} \geq 7.0$ Vdc)		10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
($V_{out} \geq 10.5$ Vdc)		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	I_{OH}																mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
(V_{OH} = 9.5 Vdc)		10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)		15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
	I_{OL}																mAdc
(V_{OL} = 0.4 Vdc) Sink		5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
(V_{OL} = 0.5 Vdc)		10	1.1	–	0.90	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
(V_{OL} = 1.5 Vdc)		15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	I_{in}	–	–	–	–	–	10	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0 Vdc)	C_{in}	–	–	–	–	–	5.0	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation Per Package (C_L = 15 pF, f = 0 Hz)	P_Q																mW
		5.0	–	0.00025	–	0.000006	0.00025	–	0.015	–	0.0025	–	0.000006	0.0025	–	0.075	
		10	–	0.001	–	0.000028	0.001	–	0.06	–	0.01	–	0.000028	0.01	–	0.3	
		15	–	–	–	0.0001	–	–	–	–	–	–	0.0001	–	–	–	
Power Dissipation**† Dynamic Per Gate Plus Quiescent (C_L = 15 pF)	P_D																mW
		5.0	P_D = 0.7 mW/MHz + 0.000006 mW														
		10	P_D = 2.8 mW/MHz + 0.000028 mW														
		15	P_D = 5.0 mW/MHz + 0.00023 mW														
Output Rise Time** (C_L = 15 pF)	t_r																ns
t_r = (4.4 ns/pF) C_L + 23 ns		5.0	–	–	–	90	175	–	–	–	–	–	90	200	–	–	
t_r = (2.1 ns/pF) C_L + 11 ns		10	–	–	–	42	75	–	–	–	–	–	42	110	–	–	
t_r = (1.53 ns/pF) C_L + 7.0 ns		15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Output Fall Time** (C_L = 15 pF)	t_f																ns
t_f = (2.4 ns/pF) C_L + 34 ns		5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (1.1 ns/pF) C_L + 14 ns		10	–	–	–	30	75	–	–	–	–	–	30	110	–	–	
t_f = (0.8 ns/pF) C_L + 10 ns		15	–	–	–	22	–	–	–	–	–	–	22	–	–	–	
Turn-Off Delay Time** (C_L = 15 pF)	t_{PLH}																ns
t_{PLH} = (2.1 ns/pF) C_L + 69 ns		5.0	–	–	–	100	200	–	–	–	–	–	100	300	–	–	
t_{PLH} = (0.9 ns/pF) C_L + 32 ns		10	–	–	–	45	90	–	–	–	–	–	45	135	–	–	
t_{PLH} = (0.67 ns/pF) C_L + 20 ns		15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Turn-On Delay Time** (C_L = 15 pF)	t_{PHL}																ns
t_{PHL} = (1.6 ns/pF) C_L + 86 ns		5.0	–	–	–	110	220	–	–	–	–	–	110	330	–	–	
t_{PHL} = (0.65 ns/pF) C_L + 35 ns		10	–	–	–	45	90	–	–	–	–	–	45	135	–	–	
t_{PHL} = (0.42 ns/pF) C_L + 24 ns		15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output stage change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitance (C_L) refer to corresponding formula:

$P_T(C_L) = P_D + 1 \times 10^{-3} (C_L - 15\text{ pF}) V_{DD}^2 f$

Where: P_T in mW (Per Gate), C_L in pF, V_{DD} in Vdc, and f in MHz.

7

FIGURE 1 – CURRENT AND VOLTAGE TRANSFER CHARACTERISTICS TEST CIRCUIT

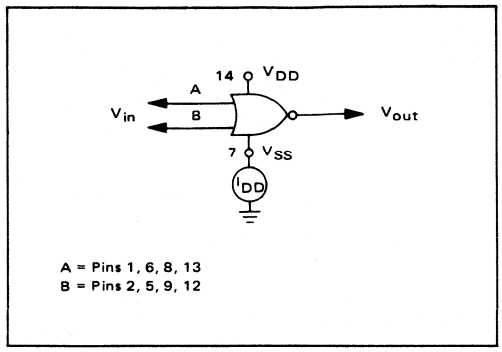


FIGURE 2 – TYPICAL VOLTAGE AND CURRENT TRANSFER CHARACTERISTICS

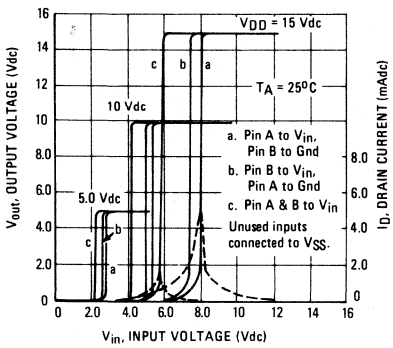


FIGURE 3 – TYPICAL VOLTAGE TRANSFER CHARACTERISTICS versus TEMPERATURE

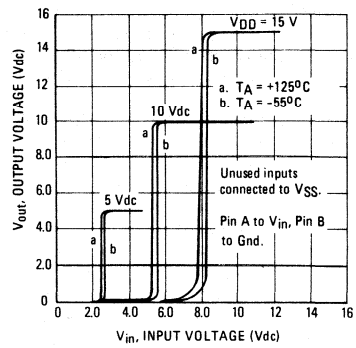


FIGURE 4 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

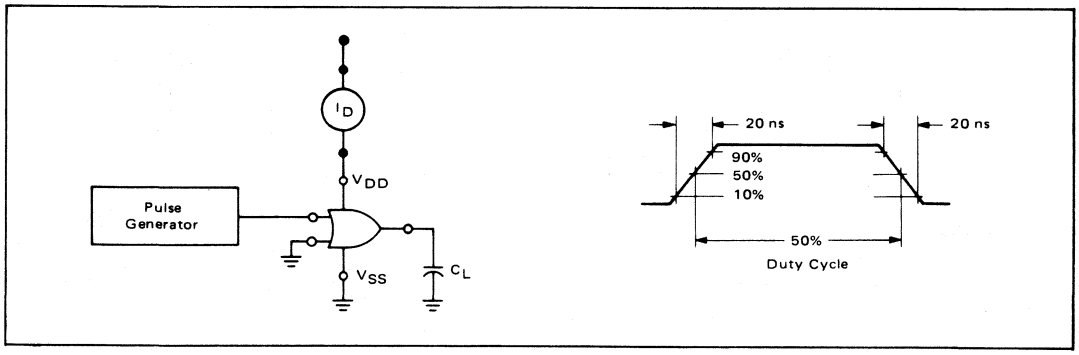
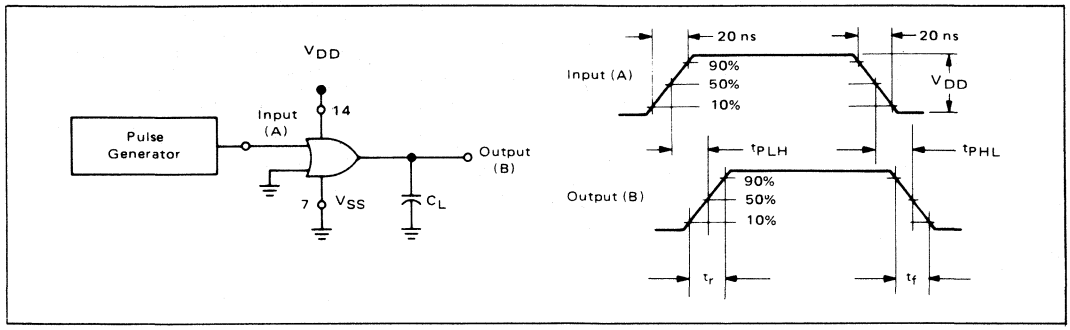


FIGURE 5 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



7

MC14581AL
MC14581CL

4-BIT ARITHMETIC LOGIC UNIT

The MC14581 is a CMOS 4-bit ALU logic unit capable of providing 16 functions of two Boolean variables and 16 binary arithmetic operations on two 4-bit words. The level of the mode control input determines whether the output function is logic or arithmetic. The desired logic function is selected by applying the appropriate binary word to the select inputs (S0 thru S3) with the mode control input high, while the desired arithmetic operation is selected by applying a low voltage to the mode control input, the required level to carry in, and the appropriate word to the select inputs. The word inputs and function outputs can be operated with either active high or active low data.

Carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs are provided to allow a full look-ahead carry scheme for fast simultaneous carry generation for the four bits in the package. Fast arithmetic operations on long words are obtainable by using the MC14582 as a second order look-ahead block. An inverted ripple carry input (C_n) and a ripple carry output (C_{n+4}) are included for ripple through operation.

When the device is in the subtract mode (LHHL), comparison of two 4-bit words present at the $\overline{A}$ and $\overline{B}$ inputs is provided using the A = B output. It assumes a high-level state when indicating equality. Also, when the ALU is in the subtract mode the C_{n+4} output can be used to indicate relative magnitude as shown in this table:

Data Level	C_n	C_{n+4}	Magnitude
Active High	H	H	$A \leq B$
	L	H	$A < B$
	H	L	$A > B$
	L	L	$A \geq B$
Active Low	L	L	$A \leq B$
	H	L	$A < B$
	L	H	$A > B$
	H	H	$A \geq B$

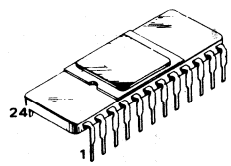
FEATURES:

- Functional Flexibility
- Low Quiescent Power Dissipation
- High Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Low Input Capacitance — 5.0 pF typical
- All Outputs Buffered

McMOS

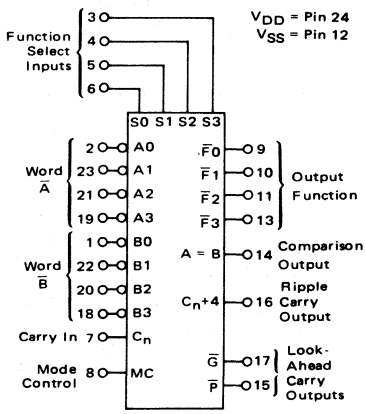
(LOW-POWER COMPLEMENTARY MOS)

4-BIT ARITHMETIC LOGIC UNIT



L SUFFIX
CERAMIC PACKAGE
CASE 684

BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD})

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 12)

Rating		Symbol	Value	Unit
DC Supply Voltage	—MC14581AL —MC14581CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs		V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin		I	10	mAdc
Operating Temperature Range	— MC14581AL — MC14581CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Figure	Symbol	V_{DD} Vdc	MC14581AL -55°C Min	MC14581AL -55°C Max	MC14581AL +25°C Min	MC14581AL +25°C Typ	MC14581AL +25°C Max	MC14581AL +125°C Min	MC14581AL +125°C Max	MC14581CL -40°C Min	MC14581CL -40°C Max	MC14581CL +25°C Min	MC14581CL +25°C Typ	MC14581CL +25°C Max	MC14581CL +85°C Min	MC14581CL +85°C Max	Unit
Output Voltage	"0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
				10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
				15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
(V_{in} = V_{DD} V_{SS})	"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
				10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
				15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																			
(V_{out} ≥3.5 Vdc)		–	V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} ≥7.0 Vdc)				10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≥10.5 Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≤1.5 Vdc)			V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)				10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≤4.5 Vdc)				15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																			mAdc
(V_{OH} = 2.5 Vdc)	Source	1	I_{OH}	5.0	-0.62	–	-0.50	-1.3	–	-0.35	–	-0.23	–	-0.20	-1.3	–	-0.16	–	
(V_{OH} = 9.5 Vdc)				10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)				15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	2	I_{OL}	5.0	0.50	–	0.40	0.6	–	0.28	–	0.23	–	0.20	0.6	–	0.16	–	
(V_{OL} = 0.5 Vdc)				10	1.1	–	0.90	1.6	–	0.65	–	0.60	–	0.50	1.6	–	0.40	–	
(V_{OL} = 1.5 Vdc)				15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current		–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		–	C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Power Dissipation**		4	P_D																mW
(C_L = 15 pF, f = 0 Hz)																			
P_D = (2.0 mW/MHz) f + 0.00025 mW				5.0	–	0.025	–	0.00025	0.025	–	1.5	–	0.25	–	0.00025	0.25	–	3.5	
P_D = (9.0 mW/MHz) f + 0.001 mW				10	–	0.1	–	0.001	0.1	–	6.0	–	1.0	–	0.001	1.0	–	14	
P_D = (20 mW/MHz) f + 0.004 mW				15	–	–	–	0.004	–	–	–	–	–	–	0.004	–	–	–	
Output Rise and Fall Time**		3	t_r,t_f																ns
(C_L = 15 pF)																			
t_r,t_f = (2.9 ns/pF) C_L + 57 ns				5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r,t_f = (1.5 ns/pF) C_L + 12.5 ns				10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r,t_f = (1.0 ns/pF) C_L + 10 ns				15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	

(Continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14581AL							MC14581CL							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Sum_{in} to Sum_{out} Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 623 ns			5.0	–	–	–	650	1000	–	–	–	–	–	650	2000	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 213 ns			10	–	–	–	225	350	–	–	–	–	–	225	700	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 151 ns			15	–	–	–	160	–	–	–	–	–	–	160	–	–	–	
Sum_{in} to P Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 403 ns			5.0	–	–	–	430	650	–	–	–	–	–	430	1300	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L +-138 ns			10	–	–	–	150	225	–	–	–	–	–	150	450	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 101 ns			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Sum_{in} to G Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 403 ns			5.0	–	–	–	430	650	–	–	–	–	–	430	1300	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 138 ns			10	–	–	–	150	225	–	–	–	–	–	150	450	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 101 ns			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Sum_{in} to C_{n+4} Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 533 ns			5.0	–	–	–	560	1000	–	–	–	–	–	560	1700	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 178 ns			10	–	–	–	190	350	–	–	–	–	–	190	600	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 131 ns			15	–	–	–	140	–	–	–	–	–	–	140	–	–	–	
C_n to Sum_{out} Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 298 ns			5.0	–	–	–	325	450	–	–	–	–	–	325	1000	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 103 ns			10	–	–	–	115	160	–	–	–	–	–	115	350	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 76 ns			15	–	–	–	85	–	–	–	–	–	–	85	–	–	–	
C_n to C_{n+4} Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 223 ns			5.0	–	–	–	250	375	–	–	–	–	–	250	750	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 78 ns			10	–	–	–	90	135	–	–	–	–	–	90	270	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 56 ns			15	–	–	–	65	–	–	–	–	–	–	65	–	–	–	
Sum_{in} to "A = B" Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 873 ns			5.0	–	–	–	900	1500	–	–	–	–	–	900	3000	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 288 ns			10	–	–	–	300	500	–	–	–	–	–	300	1000	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 216 ns			15	–	–	–	225	–	–	–	–	–	–	225	–	–	–	
Sum_{in} to Sum_{out} Delay Time** (Logic Mode) (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PLH}, t_{PHL} = (1.8 ns/pF) C_L + 523 ns			5.0	–	–	–	550	1000	–	–	–	–	–	550	1700	–	–	
t_{PLH}, t_{PHL} = (0.8 ns/pF) C_L + 173 ns			10	–	–	–	185	350	–	–	–	–	–	185	600	–	–	
t_{PLH}, t_{PHL} = (0.6 ns/pF) C_L + 126 ns			15	–	–	–	135	–	–	–	–	–	–	135	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

FIGURE 1 – TYPICAL SOURCE CURRENT TEST CIRCUIT

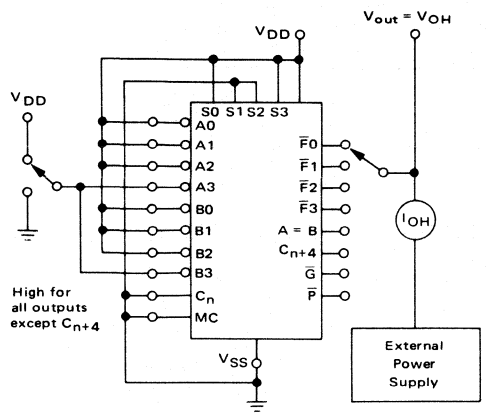


FIGURE 2 – TYPICAL SINK CURRENT TEST CIRCUIT

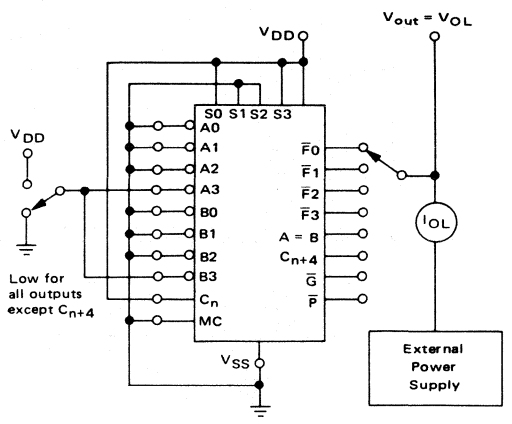


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

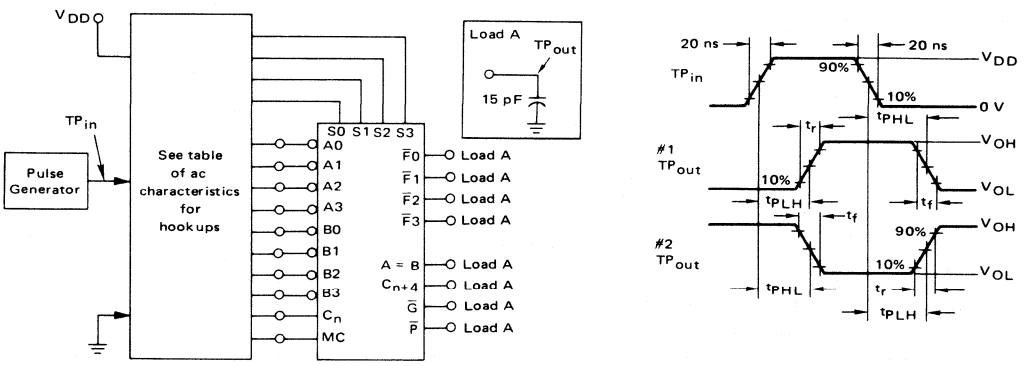


FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM

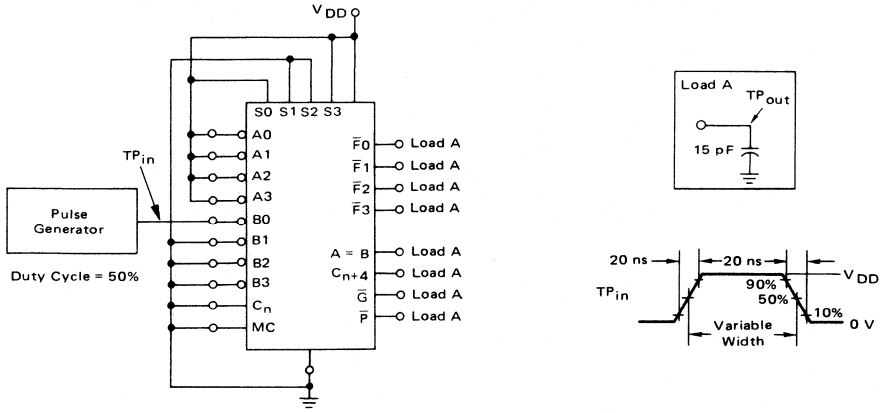
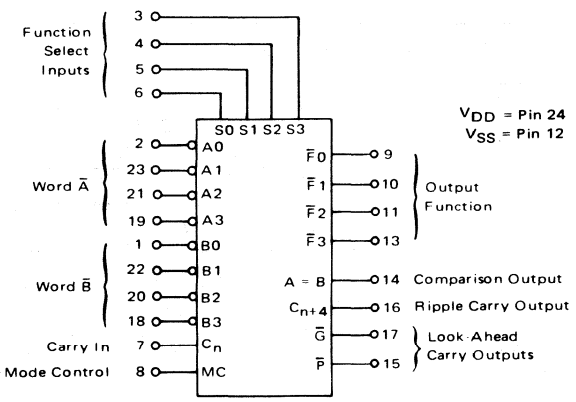


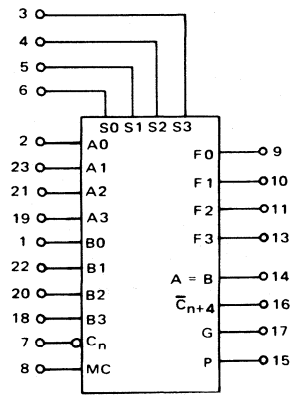
FIGURE 5 – AC TEST SETUP REFERENCE TABLE

TEST	AC PATHS		DC DATA INPUTS		MODE	WAVEFORM
	INPUTS	OUTPUTS	TO V_{SS}	TO V_{DD}		
Sum_{in} to Sum_{out} Delay Time	$\overline{A}0$	Any $\overline{F}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{P}$ Delay Time	$\overline{A}0$	$\overline{P}$	Remaining $\overline{A}$'s C_n	All $\overline{B}$'s	Add	#1
Sum_{in} to $\overline{G}$ Delay Time	$\overline{B}0$	C_{n+y}	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#1
Sum_{in} to C_{n+4} Delay Time	$\overline{B}0$	$\overline{G}$	All $\overline{A}$'s C_n	Remaining $\overline{B}$'s	Add	#2
C_n to Sum_{out} Delay Time	C_n	Any $\overline{F}$	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
C_n to C_{n+4} Delay Time	C_n	C_{n+4}	All $\overline{A}$'s	All $\overline{B}$'s	Add	#1
Sum_{in} to A = B Delay Time	$\overline{A}0$	A = B	All $\overline{B}$'s Remaining $\overline{A}$'s	C_n	Sub	#2
Sum_{in} to Sum_{out} Delay Time (Logic Mode)	All $\overline{B}$'s	Any $\overline{F}$	All A's	M	Exclusive OR	#2

BLOCK DIAGRAM (ACTIVE LOW)



BLOCK DIAGRAM (ACTIVE HIGH)



TRUTH TABLE

FUNCTION SELECT				INPUTS/OUTPUTS ACTIVE LOW		INPUTS/OUTPUTS ACTIVE HIGH	
				LOGIC FUNCTION	ARITHMETIC* FUNCTION	LOGIC FUNCTION	ARITHMETIC* FUNCTION
S3	S2	S1	S0	(MC = H)	(MC = L, C_n = L)	(MC = H)	(MC = L, $\overline{C}_n$ = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A+B
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$\overline{AB}$	$A+\overline{B}$
L	L	H	H	Logic "1"	minus 1	Logic "0"	minus 1
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{A\overline{B}}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus $(A+B)$	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
H	L	H	H	A+B	A+B	AB	AB minus 1
H	H	L	L	Logic "0"	A plus A	Logic "1"	A plus A
H	H	L	H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H	H	H	L	AB	$A\overline{B}$ plus A	A+B	$(A+\overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

*Expressed as two's complement

MC14582AL
MC14582CL
MC14582CP

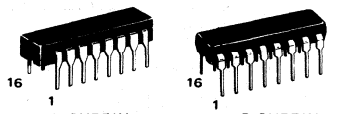
LOOK-AHEAD CARRY BLOCK

The MC14582 is a CMOS look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. The device is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table shown below.

- High Speed Operation – 115 ns typical (from Data-in to Carry-out)
- Expandable to any Number of Bits
- Noise Immunity = 45% of V_{DD} typical
- All Buffered Outputs
- Low Power Dissipation
- Diode Protection on All Inputs

McMOS
(LOW-POWER COMPLEMENTARY MOS)

LOOK-AHEAD CARRY BLOCK



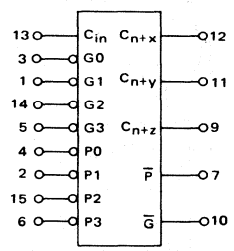
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14582AL — MC14582CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14582AL — MC14582CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

PIN DESIGNATIONS

DESIGNATION	PIN NO's	FUNCTION
$\overline{G0},\overline{G1},\overline{G2},\overline{G3}$	3,1,14,5	Active-Low Carry-Generate Inputs
$\overline{P0},\overline{P1},\overline{P2},\overline{P3}$	4,2,15,6	Active-Low Carry-Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	Carry Outputs
$\overline{G}$	10	Active-Low Group Carry-Generate Output
$\overline{P}$	7	Active-Low Group Carry-Propagate Output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leqslant (V_{in}$ or $V_{out}) \leqslant V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14582AL -55°C Min	MC14582AL -55°C Max	MC14582AL +25°C Min	MC14582AL +25°C Typ	MC14582AL +25°C Max	MC14582AL +125°C Min	MC14582AL +125°C Max	MC14582CL/CP -40°C Min	MC14582CL/CP -40°C Max	MC14582CL/CP +25°C Min	MC14582CL/CP +25°C Typ	MC14582CL/CP +25°C Max	MC14582CL/CP +85°C Min	MC14582CL/CP +85°C Max	Unit
Output Voltage "0" Level (V_{in} = V_{DD}, V_{SS})		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*																		
(V_{out} ≥3.5 Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
(V_{out} ≥7.0 Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
(V_{out} ≥10.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
(V_{out} ≤1.5 Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
(V_{out} ≤3.0 Vdc)			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	3.0	4.50	–	3.0	–	
(V_{out} ≤4.5 Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–		–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.50	-1.3	–	-0.35	–	-0.23	–	-0.20	-1.3	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.0	–	–	–	–	–	–	-3.0	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	2	I_{OL}	5.0	0.50	–	0.40	0.6	–	0.28	–	-0.23	–	0.20	0.6	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.90	1.6	–	0.65	–	0.60	–	0.50	1.6	–	0.40	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation** (C_L = 15 pF, f = 0 Hz)	4	P_D																mW
P_D = (2.5 mW/MHz) f + 0.00005 mW			5.0	–	0.0025	–	0.00005	0.0025	–	0.15	–	0.025	–	0.00005	0.025	–	0.75	
P_D = (11 mW/MHz) f + 0.0001 mW			10	–	0.01	–	0.0001	0.01	–	0.6	–	0.1	–	0.0001	0.1	–	3.0	
P_D = (25 mW/MHz) f + 0.0003 mW			15	–	–	–	0.0003	–	–	–	–	–	–	0.0003	–	–	–	
Output Rise and Fall Time** (C_L = 15 pF)	3	t_r,t_f																ns
t_r,t_f = (2.9 ns/pF) C_L + 57 ns			5.0	–	–	–	100	175	–	–	–	–	–	100	200	–	–	
t_r,t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r,t_f = (1.0 ns/pF) C_L + 10 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-On, Turn-Off Delay Time** (C_L = 15 pF)	3	t_{PLH}, t_{PHL}																ns
t_{PHL},t_{PLH} = (1.8 ns/pF) C_L + 253 ns			5.0	–	–	–	280	375	–	–	–	–	–	280	750	–	–	
t_{PHL},t_{PLH} = (0.8 ns/pF) C_L + 103 ns			10	–	–	–	115	150	–	–	–	–	–	115	300	–	–	
t_{PHL},t_{PLH} = (0.6 ns/pF) C_L + 81 ns			15	–	–	–	90	–	–	–	–	–	–	90	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" to "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

LOGIC EQUATIONS

$C_{n+x} = G0 + P0 \bullet C_n$
$C_{n+y} = G1 + P1 \bullet G0 + P1 \bullet P0 \bullet C_n$
$C_{n+z} = G2 + P2 \bullet G1 + P2 \bullet P1 \bullet G0 + P2 \bullet P1 \bullet P0 \bullet C_n$
$\overline{G} = G3 + P3 \bullet G2 + P3 \bullet P2 \bullet G1 + P3 \bullet P2 \bullet P1 \bullet G0$
$\overline{P} = P3 \bullet P2 \bullet P1 \bullet P0$

FIGURE 1 – SOURCE CURRENT TEST CIRCUIT

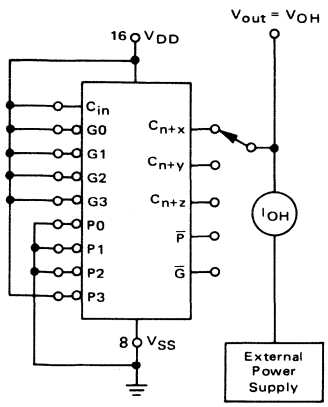


FIGURE 2 – SINK CURRENT TEST CIRCUIT

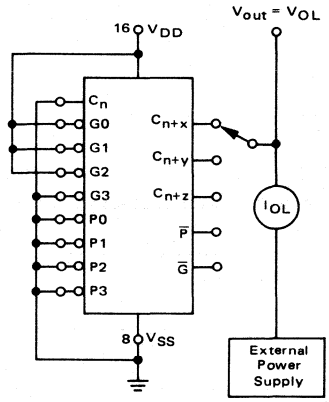
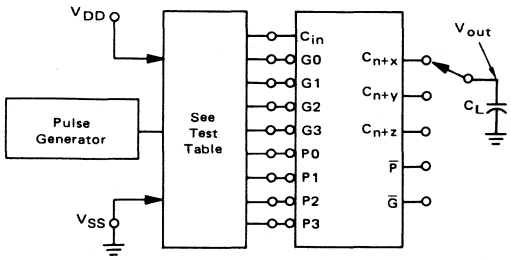


FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST TABLE

AC PATHS		DC DATA	
INPUT	OUTPUT	To V_{SS}	To V_{DD}
$\bar{P}0$	$\bar{P}$	Remaining $\bar{P}$'s, C_n	$\bar{G}$'s
$\bar{G}0$	$\bar{G}$	$\bar{P}$'s, C_n	Remaining $\bar{G}$'s
C_n	C_{n+x}, C_{n+y} C_{n+z}	$\bar{P}$'s	$\bar{G}$'s

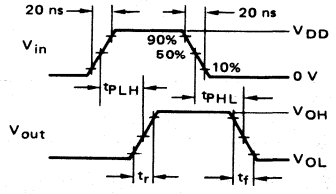
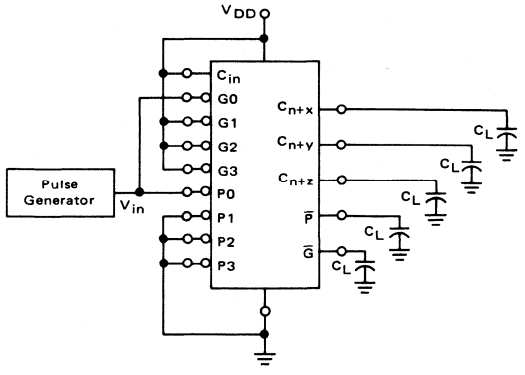
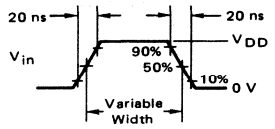


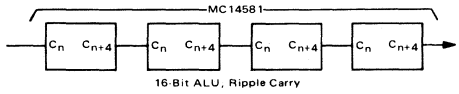
FIGURE 4 – DYNAMIC POWER DISSIPATION TEST CIRCUIT AND WAVEFORM



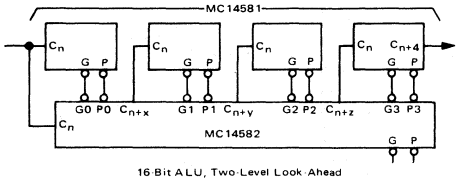


7

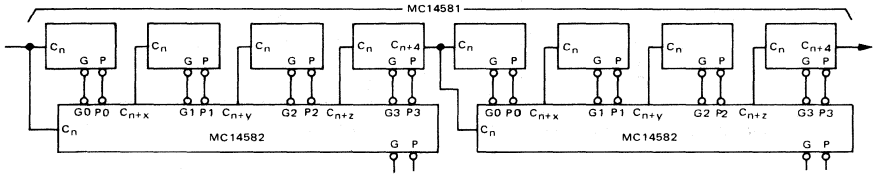
TYPICAL APPLICATIONS



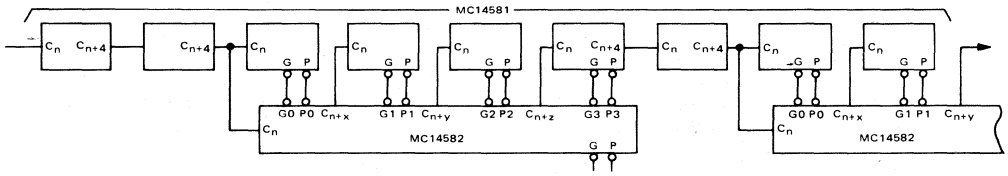
16-Bit ALU, Ripple Carry



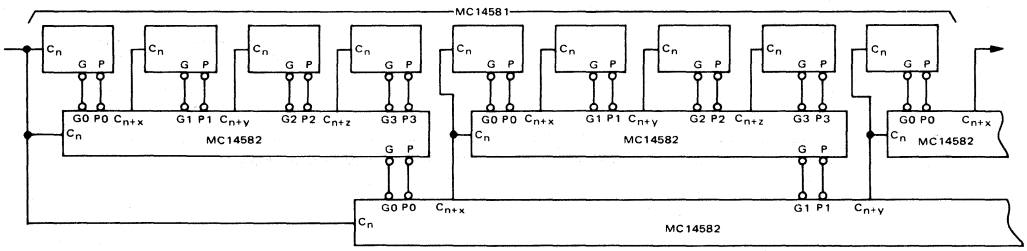
16-Bit ALU, Two-Level Look-Ahead



32-Bit ALU, Two-Level Look-Ahead Over 16-Bit Groups



Combined two-level look-ahead and ripple-carry ALU



64-Bit ALU, Full Carry Look-Ahead in Three Levels.

A and B inputs and F outputs are not shown (MC14581).

MC14583AL
MC14583CL
MC14583CP

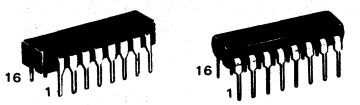
Advance Information

DUAL SCHMITT TRIGGER

The MC14583 is a dual Schmitt trigger constructed with complementary P-channel and N-channel MOS devices on a monolithic silicon substrate. Each Schmitt trigger is functionally independent except for a common 3-state input and an internally-connected Exclusive OR output for use in line receiver applications. Trigger levels are adjustable through the positive, negative, and common terminals with the use of external resistors. Applications include the speed-up of a slow waveform edge in interface receivers, level detectors, etc.

- Quiescent Power Dissipation = 25 nW/package Typical
- Schmitt Trigger Input Noise Immunity = 60% of V_{DD} Typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc (MC14583AL)
  3.0 Vdc to 16 Vdc (MC14583CL/CP)
- Single Supply Operation

McMOS
(LOW-POWER COMPLEMENTARY MOS)
DUAL SCHMITT TRIGGER



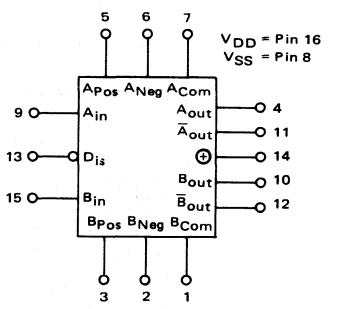
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

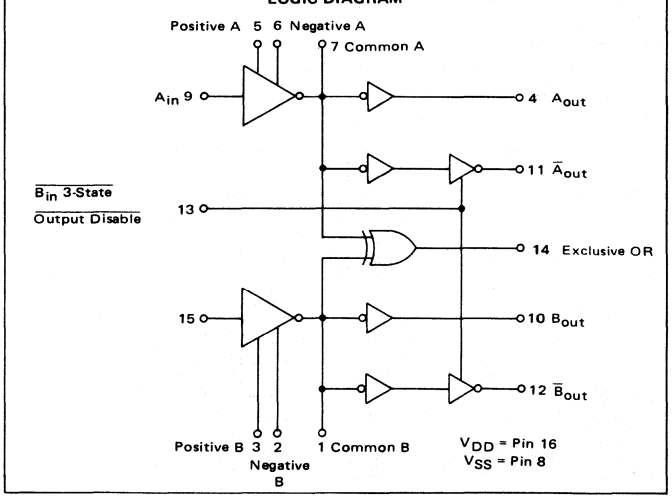
MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage — MC14583AL — MC14583CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MC14583AL — MC14583CL/CP	T_A	 -55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM



LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS				
A	B	$\overline{Dis}$	A_{out}	$\bar{A}_{out}$	B_{out}	$\bar{B}_{out}$	⊕
0	0	0	0	R	0	R	0
0	0	1	0	1	0	1	0
0	1	0	0	R	1	R	1
0	1	1	0	1	1	0	1
1	0	0	1	R	0	R	1
1	0	1	1	0	0	1	1
1	1	0	1	R	1	R	0
1	1	1	1	0	1	0	0

R = High resistance at output

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information on a new introduction and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14583AL							MC14583CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0.00	0.01	–	0.05	–	0.01	–	0.00	0.01	–	0.05	Vdc
			10	–	0.01	–	0.00	0.01	–	0.05	–	0.01	–	0.00	0.01	–	0.05	
			15	–	–	–	0.00	–	–	–	–	–	–	0.00	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.00	–	4.95	–	4.99	–	4.99	5.00	–	4.95	–	
			10	9.99	–	9.99	10.0	–	9.95	–	9.99	–	9.99	10.0	–	9.95	–	
			15	–	–	–	15.0	–	–	–	–	–	–	15.0	–	–	–	
Noise Immunity* (A and B Inputs)																		
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	2.0	–	2.0	3.5	–	1.9	–	2.0	–	2.0	3.5	–	1.9	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	4.0	–	4.0	7.0	–	3.9	–	4.0	–	4.0	7.0	–	3.9	–	
($V_{out} \geq 10.5$ Vdc)	–		15	–	–	–	10.5	–	–	–	–	–	–	10.5	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.9	–	2.0	3.5	–	2.0	–	1.9	–	2.0	3.5	–	2.0	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	3.9	–	4.0	7.0	–	4.0	–	3.9	–	4.0	7.0	–	4.0	–	
($V_{out} \leq 4.5$ Vdc)	–		15	–	–	–	10.5	–	–	–	–	–	–	10.5	–	–	–	
Noise Immunity* (3-State Input)																		
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	Vdc
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	3.0	–	
($V_{out} \geq 10.5$ Vdc)	–		15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	0.9	–	1.0	2.0	–	0.9	–	0.9	–	1.0	2.0	–	1.0	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	0.9	–	1.0	2.0	–	0.9	–	0.9	–	1.0	2.0	–	1.0	–	
($V_{out} \leq 4.5$ Vdc)	–		15	–	–	–	2.0	–	–	–	–	–	–	2.0	–	–	–	
Output Drive Current																		
(V_{OH} = 2.5 Vdc) Source	1	I_{OH}	5.0	-0.62	–	-0.5	-1.5	–	-0.35	–	-0.23	–	-0.2	-1.5	–	-0.16	–	mAdc
(V_{OH} = 9.5 Vdc)			10	-0.62	–	-0.5	-1.0	–	-0.35	–	-0.23	–	-0.2	-1.0	–	-0.16	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-3.5	–	–	–	–	–	–	-3.6	–	–	–	
(V_{OL} = 0.4 Vdc) Sink	1	I_{OL}	5.0	0.5	–	0.4	0.8	–	0.28	–	0.23	–	0.2	0.8	–	0.16	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.1	–	0.9	1.2	–	0.65	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current		I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance (V_{in} = 0)		C_{in}	–	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	pF
Quiescent Dissipation	2	P_D																mW
(C_L = 15 pF, f = 0 MHz)																		
P_D = (2.25 mW/MHz) f + 0.0000025 mW			5.0	–	0.0025	–	0.0000025	0.00025	–	0.015	–	0.0025	–	0.0000025	0.0025	–	0.025	
P_D = (9.0 mW/MHz) f + 0.00001 mW			10	–	0.001	–	0.00001	0.001	–	0.06	–	0.01	–	0.00001	0.01	–	0.14	
P_D = (20.3 mW/MHz) f + 0.0001 mW			15	–	–	–	0.0001	–	–	–	–	–	–	0.0001	–	–	–	
Output Rise and Fall Times**	4	t_r,t_f																ns
(C_L = 15 pF)																		
t_r,t_f = (4.8 ns/pF) C_L + 28 ns			5.0	–	–	–	100	300	–	–	–	–	–	100	350	–	–	
t_r,t_f = (1.5 ns/pF) C_L + 12.5 ns			10	–	–	–	35	100	–	–	–	–	–	35	150	–	–	
t_r,t_f = (0.8 ns/pF) C_L + 8.0 ns			15	–	–	–	20	–	–	–	–	–	–	20	–	–	–	

(Continued on next page)

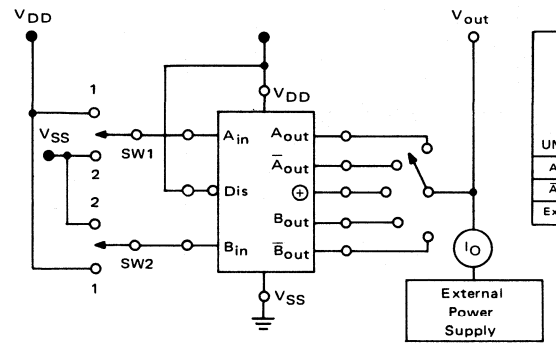
ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14583AL							MC14583CL/CP							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
				Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Turn-On, Turn-Off Delay Times**	4	t_{PHL}, t_{PLH}																ns
A_{in}, B_{in} to A_{out}, B_{out}																		
t_{PHL}, t_{PLH} = (3.0 ns/pF) C_L + 555 ns			5.0	–	–	–	600	900	–	–	–	–	–	600	1500	–	–	
t_{PHL}, t_{PLH} = (0.93 ns/pF) C_L + 186 ns			10	–	–	–	200	300	–	–	–	–	–	200	500	–	–	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 127.5 ns			15	–	–	–	135	–	–	–	–	–	–	135	–	–	–	
Turn-On, Turn-Off Delay Times**	4	t_{PHL}, t_{PLH}																ns
A_{in}, B_{in} to $\bar{A}_{out}$, $\bar{B}_{out}$																		
t_{PHL}, t_{PLH} = (3.0 ns/pF) C_L + 1005 ns			5.0	–	–	–	1050	1600	–	–	–	–	–	1050	2600	–	–	
t_{PHL}, t_{PLH} = (0.93 ns/pF) C_L + 337 ns			10	–	–	–	350	525	–	–	–	–	–	350	750	–	–	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 242.5 ns			15	–	–	–	240	–	–	–	–	–	–	240	–	–	–	
Turn-On, Turn-Off Delay Times**	4	t_{PHL}, t_{PLH}																ns
A_{in}, B_{in} to Exclusive OR																		
t_{PHL}, t_{PLH} = (3.0 ns/pF) C_L + 655 ns			5.0	–	–	–	700	1050	–	–	–	–	–	700	1750	–	–	
t_{PHL}, t_{PLH} = (0.93 ns/pF) C_L + 236 ns			10	–	–	–	250	375	–	–	–	–	–	250	625	–	–	
t_{PHL}, t_{PLH} = (0.5 ns/pF) C_L + 142.5 ns			15	–	–	–	150	–	–	–	–	–	–	150	–	–	–	
3-State Enable Delay	5	t_{on}																ns
			5.0	–	–	–	560	840	–	–	–	–	–	560	1400	–	–	
			10	–	–	–	200	300	–	–	–	–	–	200	500	–	–	
			15	–	–	–	120	–	–	–	–	–	–	120	–	–	–	
3-State Disable Delay	5	t_{off}																ns
			5.0	–	–	–	170	250	–	–	–	–	–	170	425	–	–	
			10	–	–	–	60	90	–	–	–	–	–	60	150	–	–	
			15	–	–	–	35	–	–	–	–	–	–	35	–	–	–	
Positive Threshold Voltage	3	V_P																Vdc
(R1, R2 = 5.0 kΩ)			5.0	–	–	–	3.25	–	–	–	–	–	–	3.25	–	–	–	
			10	–	–	–	5.9	–	–	–	–	–	–	5.9	–	–	–	
			15	–	–	–	8.5	–	–	–	–	–	–	8.5	–	–	–	
Negative Threshold Voltage	3	V_N																Vdc
(R1, R2 = 5.0 kΩ)			5.0	–	–	–	1.75	–	–	–	–	–	–	1.75	–	–	–	
			10	–	–	–	4.1	–	–	–	–	–	–	4.1	–	–	–	
			15	–	–	–	6.5	–	–	–	–	–	–	6.5	–	–	–	
Hysteresis Voltage		V_H																Vdc
(R1, R2 = 5.0 kΩ)			5.0	–	–	1.0	1.5	2.2	–	–	–	–	0.6	1.5	3.7	–	–	
			10	–	–	1.2	1.8	2.7	–	–	–	–	0.72	1.8	4.5	–	–	
			15	–	–	–	2.0	–	–	–	–	–	–	2.0	–	–	–	
Threshold Voltage Variation		ΔV_T																Vdc
A to B (R1, R2 = 5.0 kΩ)			5.0	–	–	–	0.1	–	–	–	–	–	–	0.1	–	–	–	
			10	–	–	–	0.15	–	–	–	–	–	–	0.15	–	–	–	
			15	–	–	–	0.20	–	–	–	–	–	–	0.20	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
When testing the A and B inputs, connect Positive A, Negative A, and Common A together, and also connect Positive B, Negative B, and Common B together.

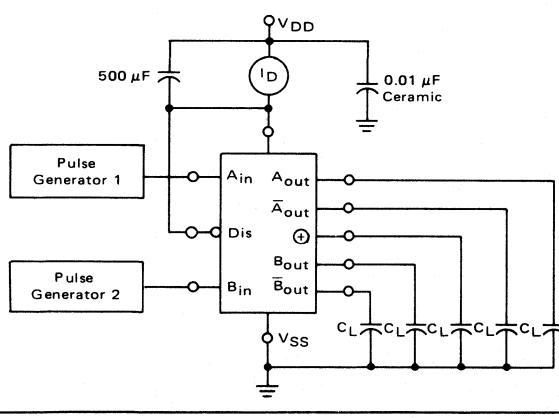
**The formula given is for the typical characteristics only.

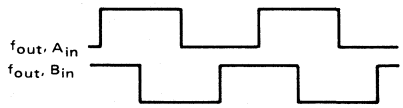
FIGURE 1 – TYPICAL OUTPUT SOURCE AND SINK CHARACTERISTICS TEST CIRCUIT



OUTPUT UNDER TEST	OUTPUT SOURCE CHARACTERISTICS		OUTPUT SINK CHARACTERISTICS	
	TEST VALUE $V_{GS} = -V_{DD}$, $V_{DS} = V_{out} - V_{DD}$		TEST VALUE $V_{GS} = V_{DD}$, $V_{DS} = V_{out}$	
	SWITCH POSITION		SWITCH POSITION	
	SW1	SW2	SW1	SW2
A_{out}, B_{out}	1	1	2	2
$\overline{A}_{out}$, $\overline{B}_{out}$	2	2	1	1
Exclusive OR	1	2	1	1

FIGURE 2 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS



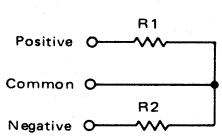


$$P_{D(C_L)} = P_D + (6f_{out} \bullet 10^{-3})(C_L - 15)(V_{DD}^2)$$

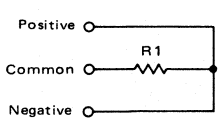
$P_{D(C_L)}$ and P_D are in mW
C_L is in pF
f_{out} is in MHz
V_{DD} is in Volts

FIGURE 3 – TYPICAL THRESHOLD POINTS

A – Feedback scheme for independent threshold adjustment:



B – Feedback scheme for hysteresis adjustment:



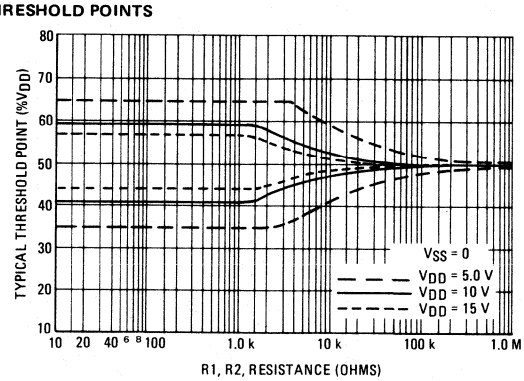


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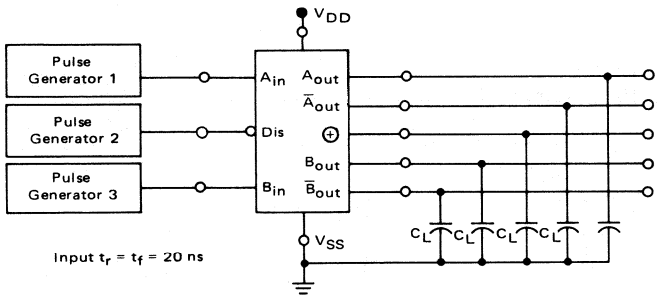
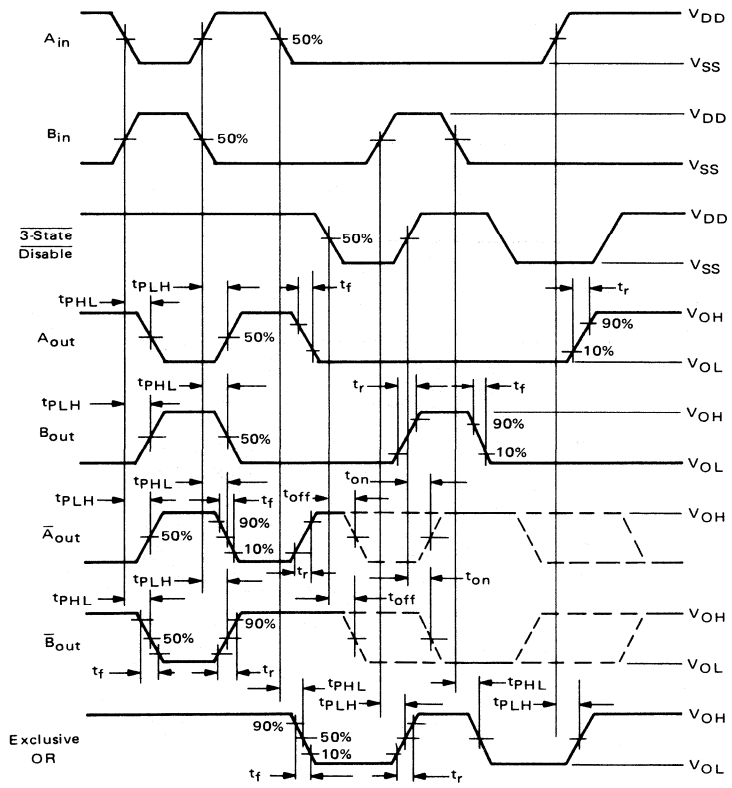
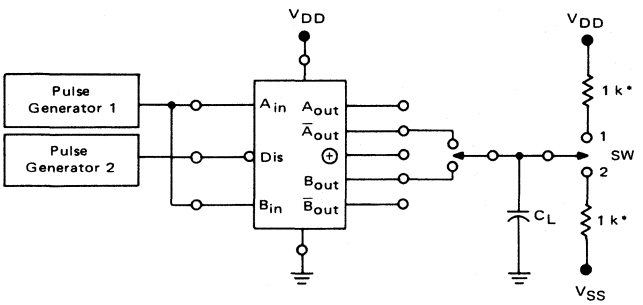
FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





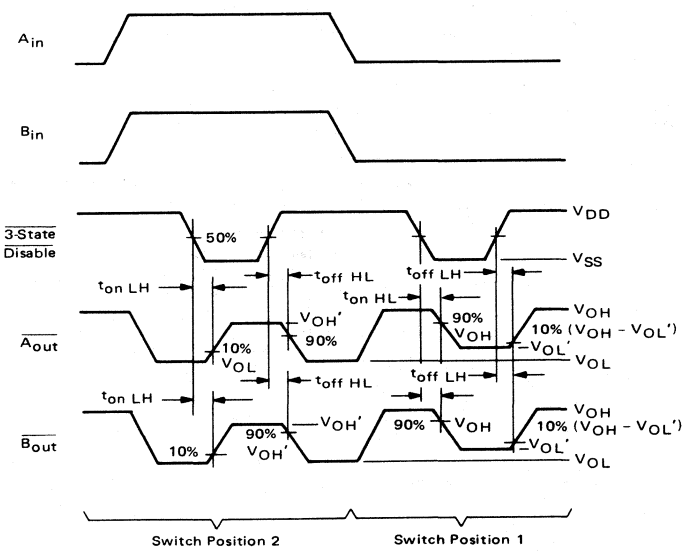
Note: Dashed lines indicate high output resistance.

FIGURE 5 – 3-STATE SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH POSITION
$t_{on\ HL}$	1
$t_{on\ LH}$	2
$t_{off\ HL}$	2
$t_{off\ LH}$	1

*Metal film, ± 1%, 1/4 W or greater
C_L = 15 pF, which includes test circuit capacitance.



V_{OL}' and V_{OH}' refer to the levels present as a result of the 1 k ohm load resistors.

MC14585AL
MC14585CL
MC14585CP

Advance Information

4-BIT MAGNITUDE COMPARATOR

The MC14585 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator, (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

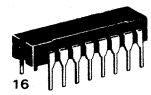
Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout >50
- Buffered Outputs Compatable with HTL and Low Power TTL
- Low Quiescent Power Dissipation – 25 nW typical
- Expandable
- Applicable to Binary or 8421-BCD Code

McMOS

(LOW POWER COMPLEMENTARY MOS)

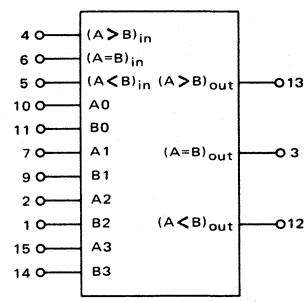
4-BIT MAGNITUDE COMPARATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MC14585AL MC14585CL/CP	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—MC14585AL — MC14585CL/CP	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

This is advance information and specifications are subject to change without notice.

See Mechanical Data Section for package dimensions.

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ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD} Vdc	MC14585AL -55°C Min	MC14585AL -55°C Max	MC14585AL +25°C Min	MC14585AL +25°C Typ	MC14585AL +25°C Max	MC14585AL +125°C Min	MC14585AL +125°C Max	MC14585CL/CP -40°C Min	MC14585CL/CP -40°C Max	MC14585CL/CP +25°C Min	MC14585CL/CP +25°C Typ	MC14585CL/CP +25°C Max	MC14585CL/CP +85°C Min	MC14585CL/CP +85°C Max	Unit
Output Voltage "0" Level	–	V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	Vdc
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–	V_{NL}																Vdc
$V_{out} \geq 3.5$ Vdc			5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
$V_{out} \geq 7.0$ Vdc			10	3.0	–	3.0	4.50	–	2.9	–	3.0	–	3.0	4.50	–	2.9	–	
$V_{out} \geq 10.5$ Vdc			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
		V_{NH}																Vdc
$V_{out} \leq 1.5$ Vdc			5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	
$V_{out} \leq 3.0$ Vdc			10	2.9	–	3.0	4.50	–	3.0	–	2.9	–	5.0	4.50	–	3.0	–	
$V_{out} \leq 4.5$ Vdc			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current	–	I_{OH}																mAdc
V_{OH} = 2.5 Vdc Source			5.0	-0.62	–	-0.50	-1.7	–	-0.35	–	-0.23	–	-0.20	-1.7	–	-0.16	–	
V_{OH} = 9.5 Vdc			10	-0.62	–	-0.50	-0.9	–	-0.35	–	-0.23	–	-0.20	-0.9	–	-0.16	–	
V_{OH} = 13.5 Vdc			15	–	–	–	-3.5	–	–	–	–	–	–	-3.5	–	–	–	
		I_{OL}																mAdc
V_{OL} = 0.4 Vdc Sink			5.0	0.50	–	0.40	0.78	–	0.28	–	0.23	–	0.20	0.78	–	0.16	–	
V_{OL} = 0.5 Vdc			10	1.1	–	0.50	2.0	–	0.65	–	0.60	–	0.50	2.0	–	0.40	–	
V_{OL} = 1.5 Vdc			15	–	–	–	7.8	–	–	–	–	–	–	7.8	–	–	–	
Input Current	–	I_{in}	–	–	–	–	10	–	–	–	–	–	–	10	–	–	–	pAdc
Input Capacitance, V_{in} = 0 Vdc	–	C_{in}	–	–	–	–	5	–	–	–	–	–	–	5	–	–	–	pF
Quiescent Dissipation**†	1	P_D																mW
(C_L = 15 pF, f = 0 Hz)																		
P_D = (2.0 mW/MHz) f + 0.000025 mW			5.0	–	0.025	–	0.000025	0.025	–	1.5	–	0.25	–	0.000025	0.25	–	3.5	
P_D = (8.0 mW/MHz) f + 0.00010 mW			10	–	0.10	–	0.00010	0.10	–	6.0	–	1.0	–	0.00010	1.0	–	14	
P_D = (18 mW/MHz) f + 0.00023 mW			15	–	–	–	0.00023	–	–	–	–	–	–	0.00023	–	–	–	
Output Rise Time**	2	t_r																ns
(C_L = 15 pF)																		
t_r = (3.0 ns/pF) C_L + 25 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_r = (1.5 ns/pF) C_L + 12 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_r = (1.1 ns/pF) C_L + 8.0 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Output Fall Time**	2	t_f																ns
(C_L = 15 pF)																		
t_f = (1.5 ns/pF) C_L + 47 ns			5.0	–	–	–	70	175	–	–	–	–	–	70	200	–	–	
t_f = (0.75 ns/pF) C_L + 24 ns			10	–	–	–	35	75	–	–	–	–	–	35	110	–	–	
t_f = (0.55 ns/pF) C_L + 17 ns			15	–	–	–	25	–	–	–	–	–	–	25	–	–	–	
Turn-Off Delay Time**	2	t_{PLH}																ns
(C_L = 15 pF)																		
t_{PLH} = (1.9 ns/pF) C_L + 347 ns			5.0	–	–	–	375	750	–	–	–	–	–	375	1125	–	–	
t_{PLH} = (0.75 ns/pF) C_L + 139 ns			10	–	–	–	150	300	–	–	–	–	–	150	450	–	–	
t_{PLH} = (0.56 ns/pF) C_L + 102 ns			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Turn-On Delay Time**	2	t_{PHL}																ns
(C_L = 15 pF)																		
t_{PHL} = (1.9 ns/pF) C_L + 247 ns			5.0	–	–	–	275	750	–	–	–	–	–	275	1125	–	–	
t_{PHL} = (0.75 ns/pF) C_L + 99 ns			10	–	–	–	110	300	–	–	–	–	–	110	450	–	–	
t_{PHL} = (0.56 ns/pF) C_L + 72 ns			15	–	–	–	80	–	–	–	–	–	–	80	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.

**The formula given is for the typical characteristics only.

†For dissipation at different external load capacitances (C_L) refer to corresponding formula:

$P_D(C_L) = P_D + 10^{-3}(C_L - 15\text{ pF})\,V_{DD}{}^2 f$

where: P_D in mW, C_L in pF, V_{DD} in V_{DD}, and f in MHz.

All outputs connected to respective C_L loads.

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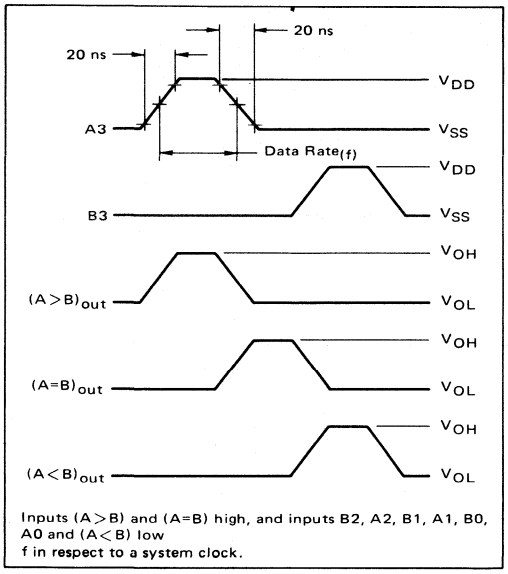
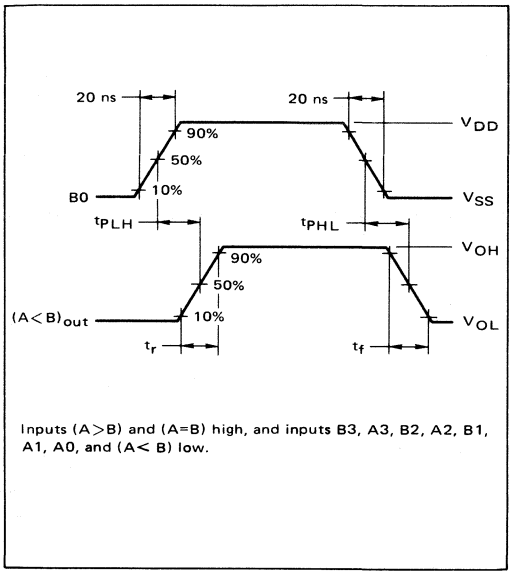
FIGURE 1 – DYNAMIC POWER DISSIPATION SIGNAL WAVEFORMS



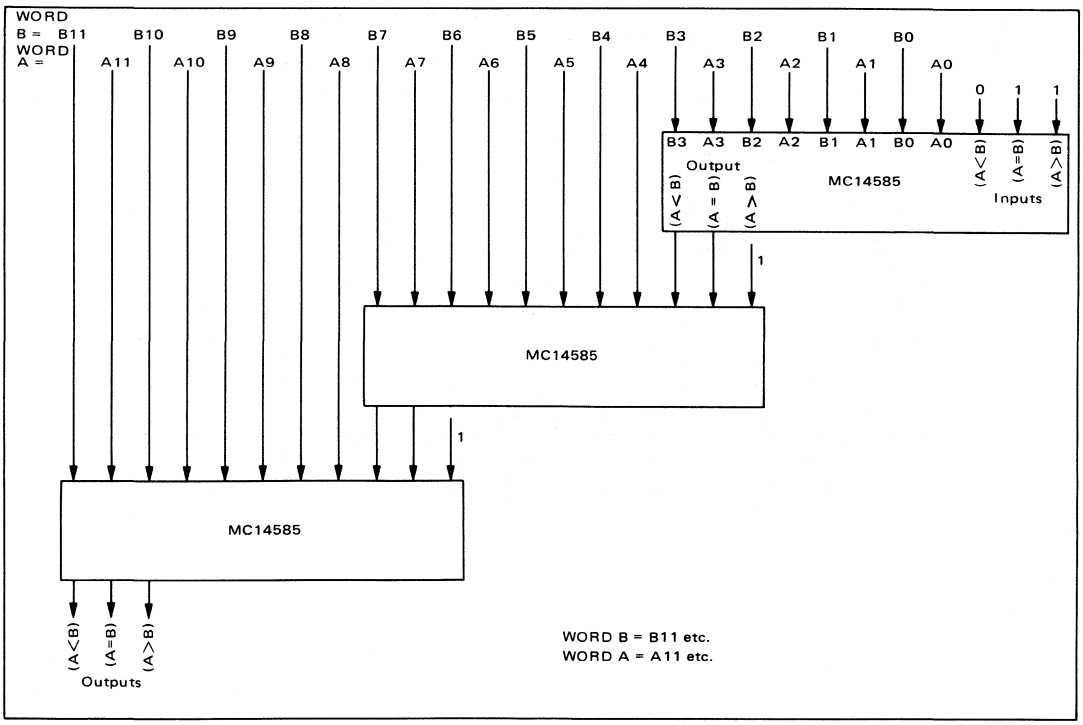
Inputs (A>B) and (A=B) high, and inputs B2, A2, B1, A1, B0, A0 and (A<B) low
f in respect to a system clock.

FIGURE 2 – DYNAMIC SIGNAL WAVEFORMS

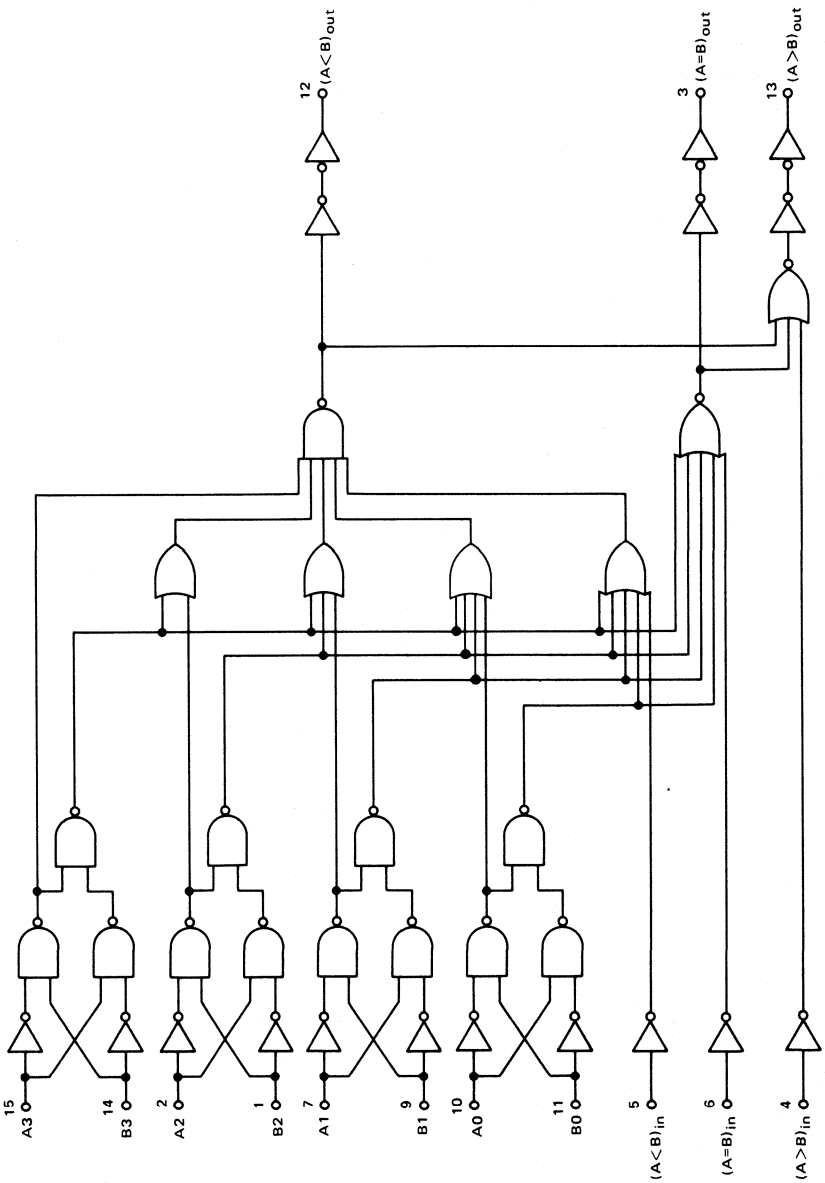


Inputs (A>B) and (A=B) high, and inputs B3, A3, B2, A2, B1, A1, A0, and (A< B) low.

FIGURE 3 – CASCADING COMPARATORS



LOGIC DIAGRAM



MCM14505AL
MCM14505CL

64-BIT RANDOM ACCESS READ-WRITE MEMORY

The MCM14505 64-bit random access read-write memory is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Fully decoded on the chip, this memory is organized as 64 one-bit words (64 X 1). Medium speed operation and micropower supply requirements make this device useful for scratch pad or buffer memory applications where power must be conserved or where battery operation is required.

When used with a battery backup, the MCM14505 can be utilized as an alterable read-only memory, allowing the battery to retain information in the memory when the system is powered down, and allowing the battery to charge when power is applied. The micropower requirements of this memory allow quiescent battery operation for great lengths of time without significant discharging.

- Quiescent Power Dissipation = 0.3 μW/package typical at V_{DD} = 10 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Supply Voltage Range = 3.0Vdc to 18 Vdc (MCM14505AL)
  4.5Vdc to 16 Vdc (MCM14505CL)
- Single Read/Write Control Line
- Wired-OR Output Capability (3-State Output) for Memory Expansion
- Access Time = 180 ns typical at V_{DD} = 10 Vdc
- Write Cycle Time = 275 ns typical at V_{DD} = 10 Vdc
- Fully Buffered Low Capacitance Inputs
- Guaranteed Fanout of One Low-Power TTL Gate at V_{DD} = 5.0 Vdc (MCM14505AL)

MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 7)

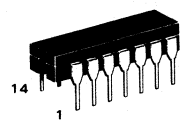
Rating	Symbol	Value	Unit
DC Supply Voltage MCM14505AL / MCM14505CL	V_{DD}	+18 to -0.5 / +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — MCM14505AL / — MCM14505CL	T_A	-55 to +125 / -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

See Mechanical Data Section for package dimensions.

McMOS

(LOW-POWER COMPLEMENTARY MOS)

64-BIT RANDOM ACCESS READ-WRITE MEMORY

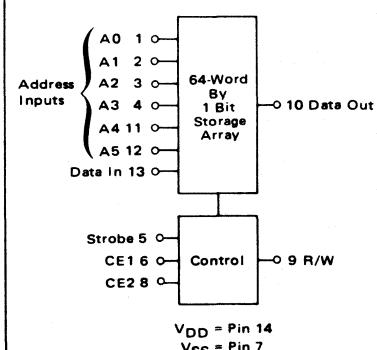


L SUFFIX
CERAMIC PACKAGE
CASE 632

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.i. either V_{SS} or V_{DD})

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

Characteristic	Figure	Symbol	V_{DD}	MCM14505AL							MCM14505CL							Unit
				-55°C		+25°C			+125°C		-40°C		+25°C			+85°C		
			Vdc	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
Output Voltage	–																	Vdc
"0" Level		V_{out}	5.0	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			10	–	0.01	–	0	0.01	–	0.05	–	0.01	–	0	0.01	–	0.05	
			15	–	–	–	0	–	–	–	–	–	–	0	–	–	–	
"1" Level			5.0	4.99	–	4.99	5.0	–	4.95	–	4.99	–	4.99	5.0	–	4.95	–	Vdc
			10	9.99	–	9.99	10	–	9.95	–	9.99	–	9.99	10	–	9.95	–	
			15	–	–	–	15	–	–	–	–	–	–	15	–	–	–	
Noise Immunity*	–																	Vdc
($V_{out} \geq 3.5$ Vdc)		V_{NL}	5.0	1.5	–	1.5	2.25	–	1.4	–	1.5	–	1.5	2.25	–	1.4	–	
($V_{out} \geq 7.0$ Vdc)			10	3.0	–	3.0	4.5	–	2.9	–	3.0	–	3.0	4.5	–	2.9	–	
($V_{out} \geq 10.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
($V_{out} \leq 1.5$ Vdc)		V_{NH}	5.0	1.4	–	1.5	2.25	–	1.5	–	1.4	–	1.5	2.25	–	1.5	–	Vdc
($V_{out} \leq 3.0$ Vdc)			10	2.9	–	3.0	4.5	–	3.0	–	2.9	–	3.0	4.5	–	3.0	–	
($V_{out} \leq 4.5$ Vdc)			15	–	–	–	6.75	–	–	–	–	–	–	6.75	–	–	–	
Output Drive Current																		mAdc
(V_{OH} = 2.5 Vdc) Source		I_{OH}	5.0	-0.62	–	-0.5	-1.2	–	-0.35	–	-0.23	–	-0.2	-1.2	–	-0.16	–	
(V_{OH} = 9.5 Vdc)			10	-0.50	–	-0.4	-0.75	–	-0.30	–	-0.19	–	-0.16	-0.75	–	-0.13	–	
(V_{OH} = 14 Vdc)			15	–	–	–	-2.0	–	–	–	–	–	–	-2.0	–	–	–	
(V_{OL} = 0.3 Vdc) Sink		I_{OL}	5.0	0.30	–	0.25	0.35	–	0.18	–	–	–	0.15	0.35	–	0.10	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.90	–	0.75	1.2	–	0.50	–	0.6	–	0.5	1.2	–	0.4	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	4.5	–	–	–	–	–	–	4.5	–	–	–	
Input Current	–	I_{in}	–	–	–	–	0.01	100	–	–	–	–	–	0.01	100	–	–	nAdc
Input Capacitance Address, Data Input, Strobe CE1	–	C_{in}	–	–	–	–	4.0	–	–	–	–	–	–	4.0	–	–	–	pF
(V_{in} = 0) Read/Write Input, CE2, V_{out}			–	–	–	–	6.0	–	–	–	–	–	–	6.0	–	–	–	
Quiescent Dissipation	–	P_D	5.0	–	0.025	–	0.00015	0.025	–	1.5	–	0.25	–	0.00015	0.25	–	7.5	mW
			10	–	0.8	–	0.0003	0.10	–	6.0	–	–	–	0.0003	1.0	–	30	
			15	–	0.001	–	–	–	–	–	–	–	–	0.001	–	–	–	

SWITCHING TIMES (C_L = 15 pF, t_r, t_f = 20 ns)

Min Strobe Down Time	1,2	t_{STL}	5.0	–	–	400	100	–	–	–	–	–	500	100	–	–	–	ns
			10	–	–	100	50	–	–	–	–	–	125	50	–	–	–	
			15	–	–	–	75	–	–	–	–	–	–	75	–	–	–	
Address Setup Time	1,2	$t_{setup(A)}$	5.0	–	–	–	-100	0	–	–	–	–	–	-100	0	–	–	ns
			10	–	–	–	-40	0	–	–	–	–	–	-40	0	–	–	
			15	–	–	–	-25	–	–	–	–	–	–	-25	–	–	–	
Data Setup Time	2	$t_{setup(D)}$	5.0	–	–	–	-75	0	–	–	–	–	–	-75	0	–	–	ns
			10	–	–	–	-15	0	–	–	–	–	–	-15	0	–	–	
			15	–	–	–	-5.0	–	–	–	–	–	–	-5.0	–	–	–	
Read Setup Time	1	$t_{setup(R)}$	5.0	–	–	–	-175	0	–	–	–	–	–	-175	0	–	–	ns
			10	–	–	–	-60	0	–	–	–	–	–	-60	0	–	–	
			15	–	–	–	-40	–	–	–	–	–	–	-40	–	–	–	
Write Setup Time	2	$t_{setup(W)}$	5.0	–	–	–	80	275	–	–	–	–	–	80	400	–	–	ns
			10	–	–	–	25	75	–	–	–	–	–	25	100	–	–	
			15	–	–	–	11	–	–	–	–	–	–	11	–	–	–	
Address Release Time	1,2	$t_{rel(A)}$	5.0	–	–	–	15	50	–	–	–	–	–	15	75	–	–	ns
			10	–	–	–	10	15	–	–	–	–	–	10	25	–	–	
			15	–	–	–	5.0	–	–	–	–	–	–	5.0	–	–	–	
Data Hold Time	2	$t_{hold(D)}$	5.0	–	–	–	10	35	–	–	–	–	–	10	50	–	–	ns
			10	–	–	–	5.0	10	–	–	–	–	–	5.0	15	–	–	
			15	–	–	–	2.5	–	–	–	–	–	–	2.5	–	–	–	
Read Release Time	1	$t_{rel(R)}$	5.0	–	–	–	-90	0	–	–	–	–	–	-90	0	–	–	ns
			10	–	–	–	-25	0	–	–	–	–	–	-25	0	–	–	
			15	–	–	–	-10	–	–	–	–	–	–	-10	–	–	–	
Write Release Time	2	$t_{rel(W)}$	5.0	–	–	–	5.0	0	–	–	–	–	–	5.0	0	–	–	ns
			10	–	–	–	10	0	–	–	–	–	–	10	0	–	–	
			15	–	–	–	30	–	–	–	–	–	–	30	–	–	–	
Read Cycle Time	1	$t_{cyc(R)}$	5.0	–	–	–	500	650	–	–	–	–	–	500	750	–	–	ns
			10	–	–	–	200	300	–	–	–	–	–	200	400	–	–	
			15	–	–	–	150	–	–	–	–	–	–	150	–	–	–	
Write Cycle Time	2	$t_{cyc(W)}$	5.0	–	–	–	440	600	–	–	–	–	–	440	700	–	–	ns
			10	–	–	–	275	400	–	–	–	–	–	275	550	–	–	
			15	–	–	–	200	–	–	–	–	–	–	200	–	–	–	
Read Access Time	1,4	$t_{acc(R)}$	5.0	–	–	–	400	550	–	–	–	–	–	400	650	–	–	ns
			10	–	–	–	180	270	–	–	–	–	–	180	350	–	–	
			15	–	–	–	110	–	–	–	–	–	–	110	–	–	–	
Output Disable Delay (10% Output Change Into 1.0 k ohm Load)	1	t_{dis}	5.0	–	–	–	200	400	–	–	–	–	–	200	600	–	–	ns
			10	–	–	–	80	160	–	–	–	–	–	80	200	–	–	
			15	–	–	–	60	–	–	–	–	–	–	60	–	–	–	

*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change. that the circuit will withstand before producing an output state change.

FIGURE 1 – READ CYCLE TIMING DIAGRAM

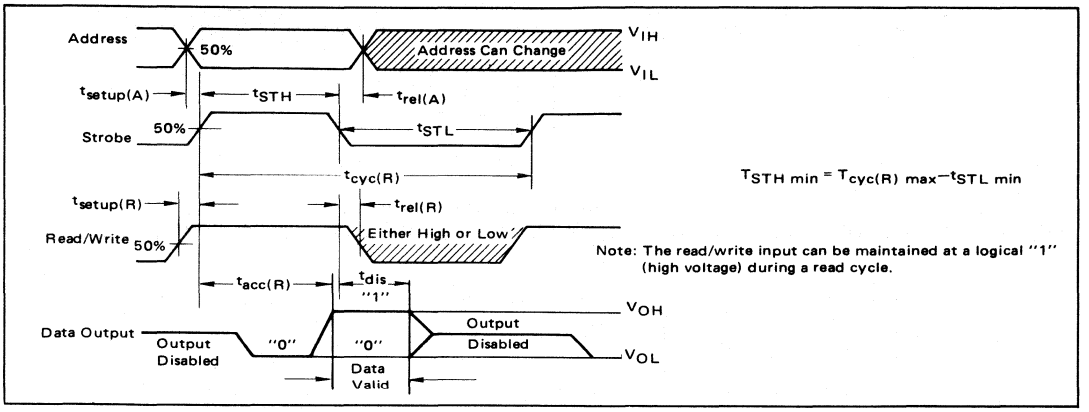

FIGURE 2 – WRITE CYCLE TIMING DIAGRAM

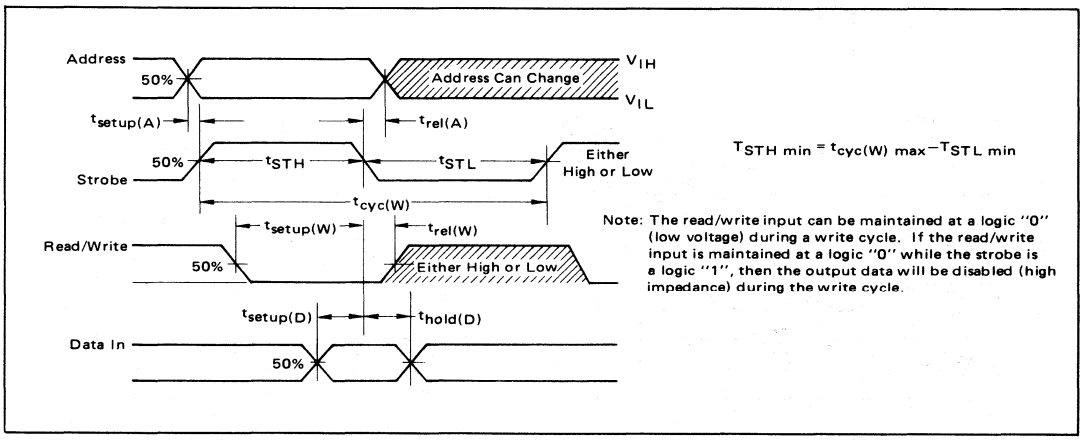

FIGURE 3 – MAXIMUM STROBE PULSE WIDTH versus TEMPERATURE

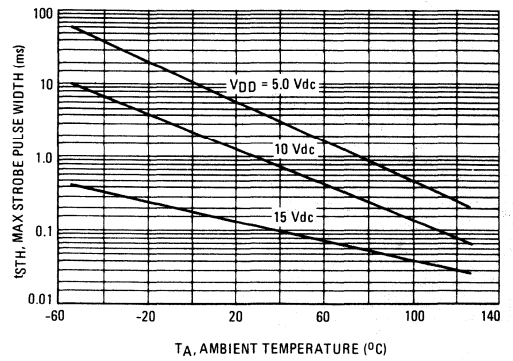

FIGURE 4 – TYPICAL READ ACCESS TIME versus LOAD CAPACITANCE

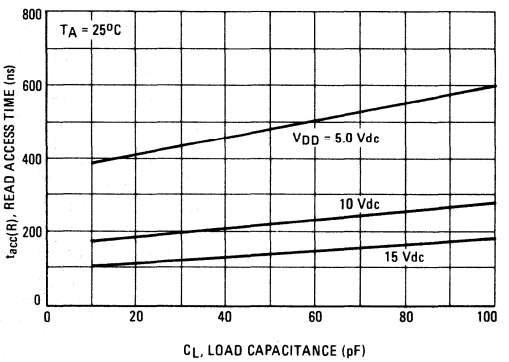

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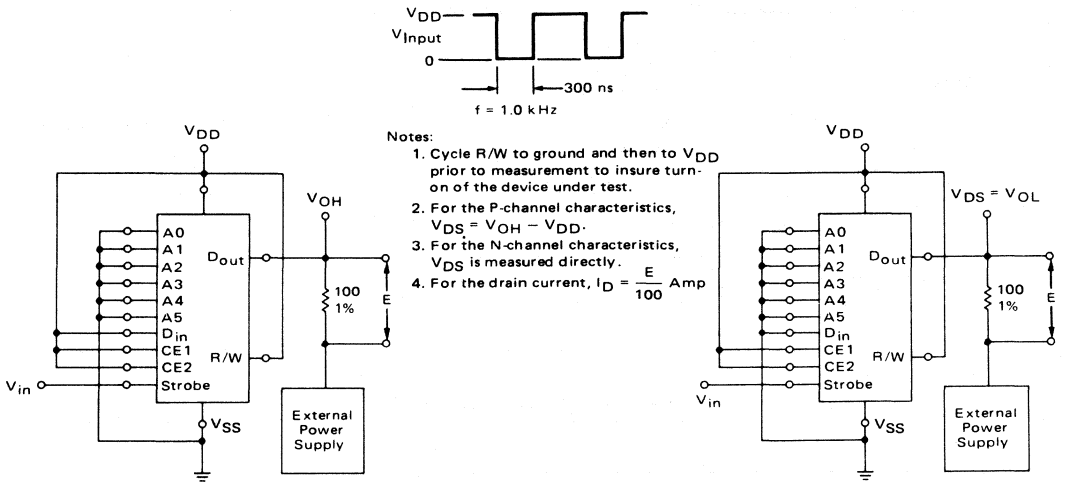
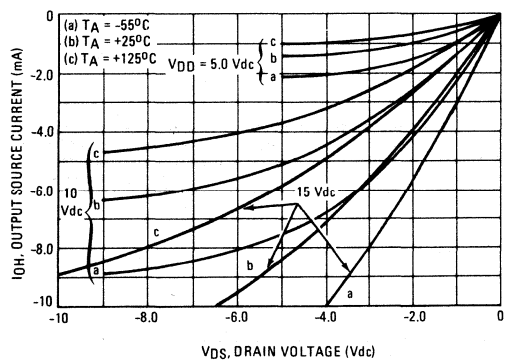
FIGURE 5 – TYPICAL OUTPUT SOURCE CAPABILITY versus TEMPERATURE

FIGURE 6 – TYPICAL OUTPUT SINK CAPABILITY versus TEMPERATURE





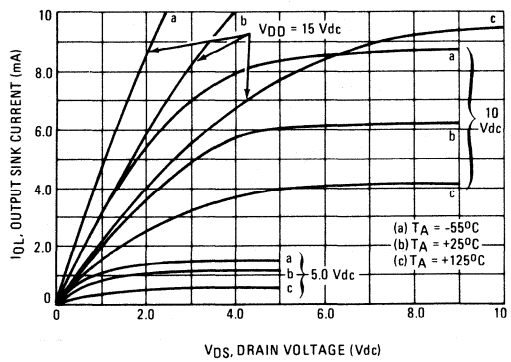


FIGURE 7 – TYPICAL POWER DISSIPATION CHARACTERISTICS

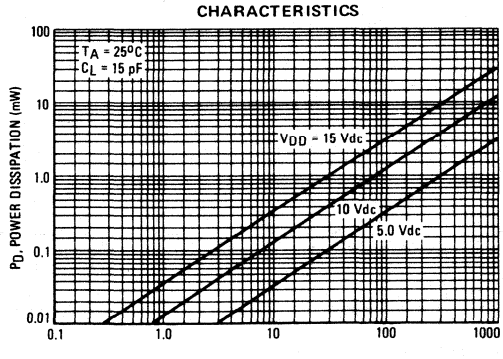
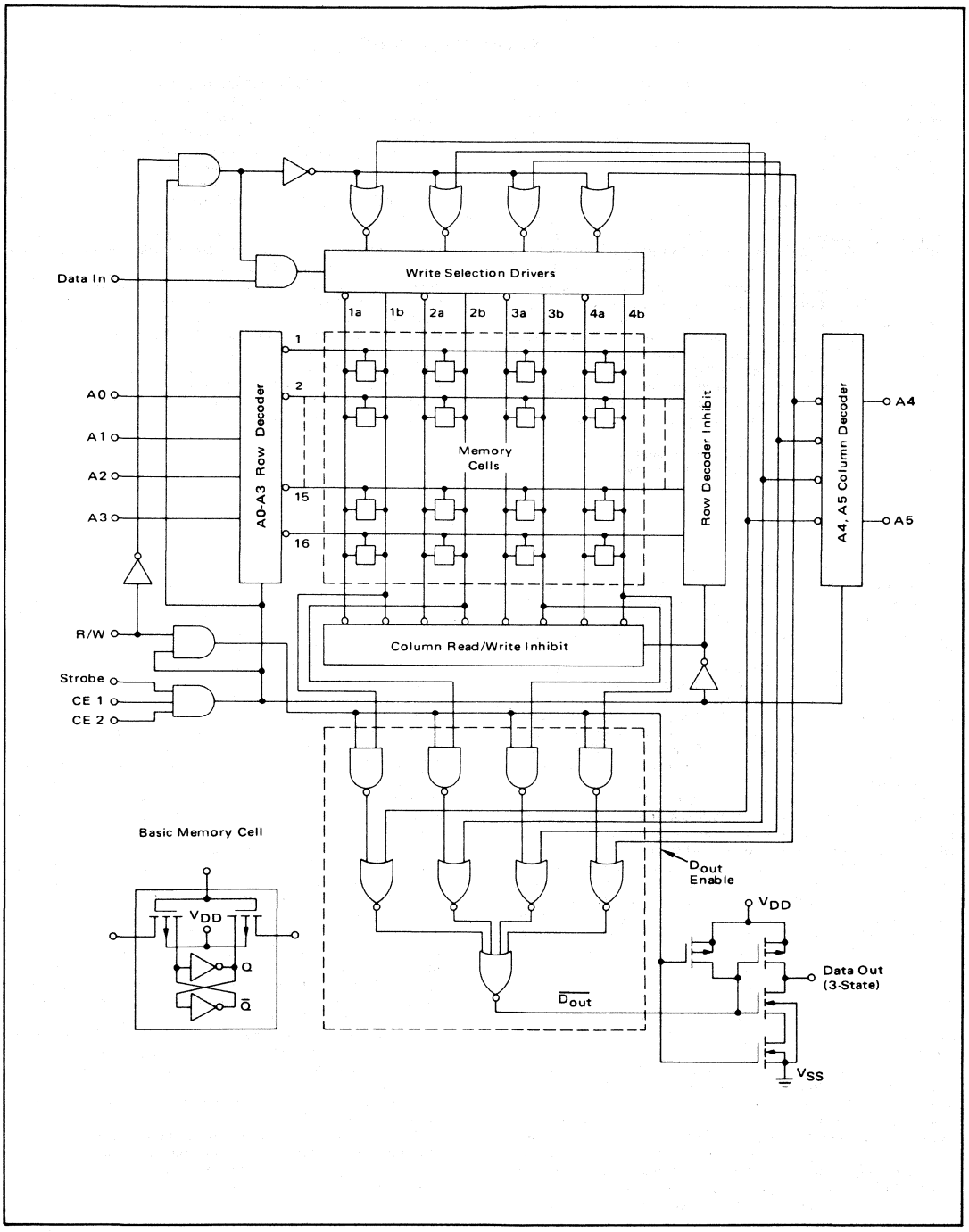


FIGURE 8 – FUNCTIONAL CIRCUIT DIAGRAM



OPERATING CHARACTERISTICS

In considering the operation of the MCM14505 CMOS memory, refer to the functional circuit diagram of Figure 8 and timing diagrams shown in Figures 1 and 2. The basic memory cell is a cross-coupled flip-flop consisting of two inverter gates and two P-channel devices for read/write control. The push-pull cell provides high speed as well as low power.

During a read cycle, when the strobe line is high the write selection drivers are disabled and the data from the selected row is available on columns 1b, 2b, 3b, and 4b. The A4 and A5 address bits are decoded to select output data from one of the four columns. The output data is available on the data output pin only when the strobe and read/write lines are high simultaneously and after the read access time, $t_{acc(R)}$, has occurred (see Figure 1). Note that the output is initially disabled and always goes to the logic "0" state (low voltage) before data is valid. The output is in the high-impedance state (disabled) when the strobe line or the R/W line is in the low state. The memory is strobed for reading or writing only when the strobe, CE1, and CE2 are high simultaneously. The R/W line can be a dc voltage during a read or write cycle and need not be pulsed, as shown in the timing diagrams. For this case the R/W line should be a logic "1" (high) for reading and a logic "0" for writing.

When the strobe line is high, the column read/write inhibit gates and the row decoder inhibit gates are disabled, the selected row is in the low state, and the unselected 15 rows retain their logic "1" level due to the row capacitance that exists when the row decoder inhibit gates are disabled. This capacitive storage mechanism requires a maximum strobe width (see Figure 3) equal to the junction reverse bias RC time constant. When the strobe is returned to a logic "0" the rows are forced to V_{DD} by the row decoder inhibit gates (pullup devices). Similarly the column read/write inhibit gates (pulldown devices) force the column lines to a logic "0" state.

Two column lines are associated with each memory cell in order to write into the cell. The write selection drivers are enabled when the R/W line is a logic "0" and the strobe line is a logic "1". The input data is written into the column selected by the column decoder. For instance, if a "1" is to be written in the memory cell associated with row 1 and column 1, then row 1 would be enabled (logic "0") while column 1b is forced high and column 1a is forced low by the write selection drivers. If a logic "0" is to be written into the cell, then column 1a is forced high and 1b is forced low. The data that is retained in the memory cell is the data that was present on the data input pin at the moment the strobe goes low when R/W is low, or when R/W goes high when the strobe is high.

APPLICATIONS INFORMATION

Figure 9 shows a 256-word by n-bit static RAM memory system. The outputs of four MCM14505 devices are tied together to form 256 words by 1 bit. Additional bits are attained by paralleling the inputs in groups of four. Memories of larger words can be attained by decoding the most significant bits of the address and ANDing them with the strobe input.

Fan-in and fan-out of the memory is limited only by speed requirements. The extremely low input and output leakage current (100 nA maximum) keep the output voltage levels from changing significantly as more outputs are tied together. With the output levels independent of fan-out, most of the power supply range is available as logic swing, regardless of the number of units wired together. As a result, high noise immunity is maintained under all conditions.

Power dissipation is 0.1 μW per bit at a 1.0-kHz rate for a 5.0-volt power supply, while the static power dissipation is 2.0 nW per bit. This low power allows non-volatile information storage when the memory is powered by a small standby battery.

Figure 10 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the usual power fails, a battery is used to sustain operation or maintain stored information. While normal power supply voltage is present, the battery is trickle-charged through a resistor which sets the charging rate. V_B is the sustaining voltage, and V^+ is the ordinary voltage from a power supply. V_{DD} connects to the power pin on the memory. Low-leakage diodes are recommended to conserve battery power.

The memory system shown in Figure 9 can be interfaced directly with the other devices in the McMOS family. No external components are required.

At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate such as the MC7407 is used as shown in Figure 11. Driver circuits are not required since the input capacitance is low (4.0 to 6.0 pF). The address, data, and read/write inputs do not need to be fast since they can be changed for the duration when the strobe pulse is low, t_{STL} (see Figures 1 and 2). For high-speed operation, a push-pull driver should be used if more than five strobe inputs must be driven at one time. One circuit of the type shown in Figure 11 can be used for every ten strobe inputs.

Figures 12, 13, and 14 show methods of interfacing the memory output to TTL logic at various memory voltages. If a V_{DD} of 5.0 volts is used for slow-speed, low-power applications, one transistor and one resistor must be used (Figure 12). The MCM14505AL will drive one low-power TTL gate directly.

If a V_{DD} of 10 volts is used, the output of the memory device can fan out to two low-power TTL gates (Figure 13a) or to a discrete transistor (Figure 13b). The discrete transistor circuit provides higher speed and/or high fan-out. A pulldown resistor at the base of the transistor is not needed for fast turn-off because of the push-pull output of the memory. Turn-on time of the transistor is much faster in Figure 13b since the voltage rise is only 0.75 volt. The low output capacitance of the MCM14505 means that several outputs can be wire-ORed without significantly degrading performance. The read access time is increased by only 20 ns typically for 16 outputs tied together when Figure 13b is used.

Five low-power TTL gates can be driven from the memory output if a V_{DD} of 15 volts is used (Figure 14a). Figure 14b shows the interface if a discrete transistor is used. The 1.0 kilohm resistor in the base is required to insure that not more than 10 mA flows through the output as listed in the maximum ratings. If a 2.0 kilohm collector resistor is used (fan-out = 3), the turn-on time of the transistor is only slightly faster than in the circuit shown in Figure 13b due to the lower output impedance when V_{DD} = 15 volts. The voltage at the memory data output has to rise to only 1.3 volts to insure driving a fan-out of three TTL devices.

If a 510-ohm collector resistor is used, 20 TTL loads may be driven. The read access time is increased about 20 ns when four memory outputs are tied together since the output voltage must rise to 3.7 volts before the transistor can sink the full I_{OL} for a fan-out of 20 TTL devices. Almost any NPN transistor with a minimum beta of 15 can be used for the interface shown in Figures 12, 13, and 14.

The high source current from the push-pull output stage of the MCM14505 makes for a simpler interface circuit since a low source current memory requires a differential comparator to achieve high-speed operation.

FIGURE 9 – CMOS 256-WORD BY n-BIT STATIC READ/WRITE MEMORY

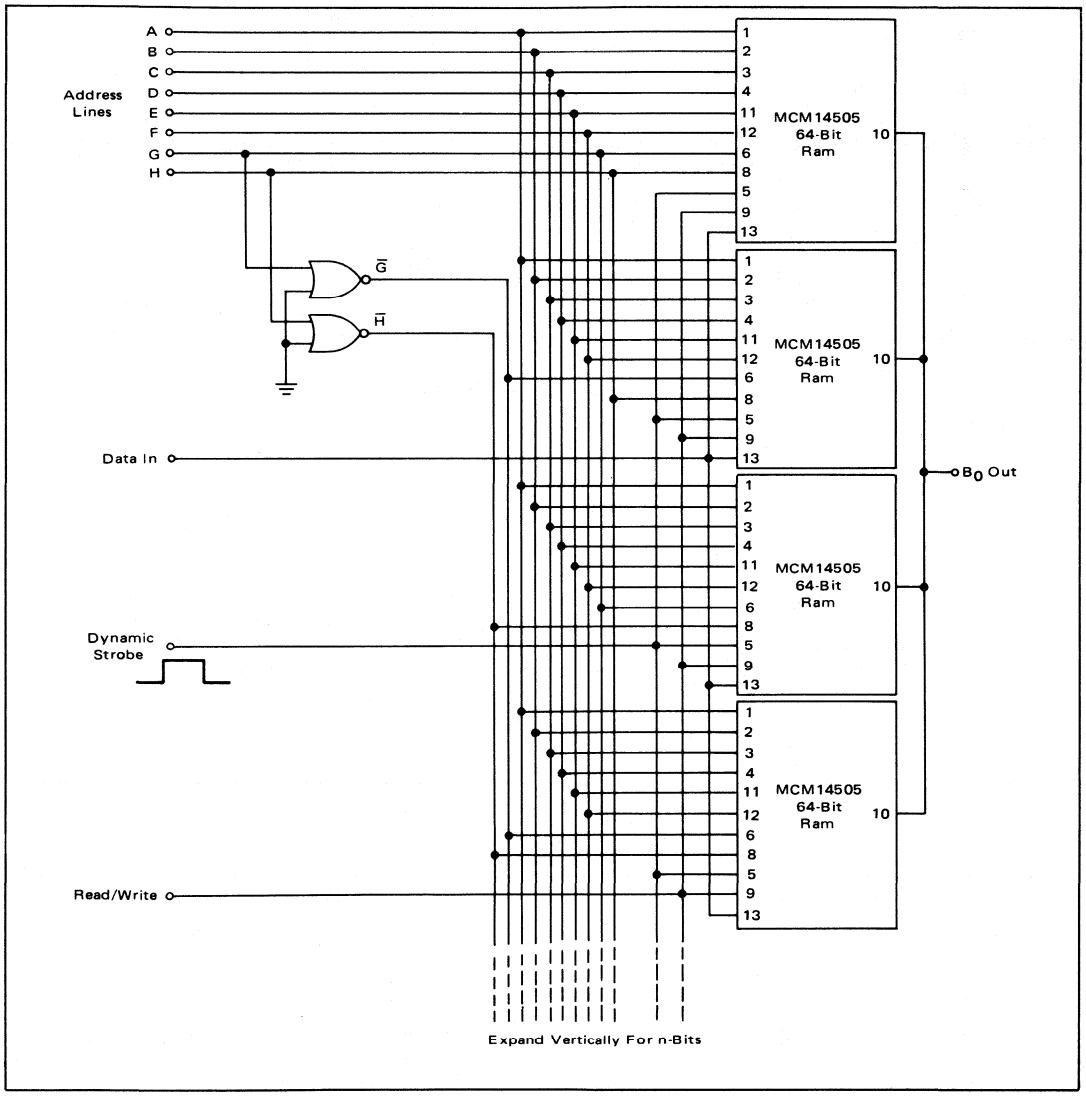


FIGURE 10 – STAND BY BATTERY CIRCUIT

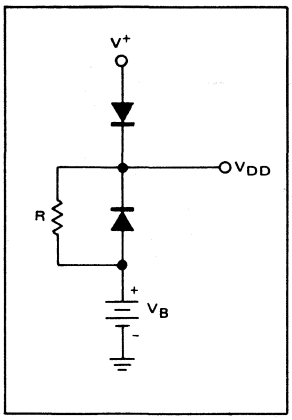


FIGURE 11 – TTL TO CMOS INTERFACE

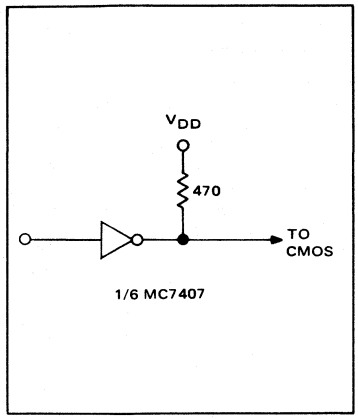


FIGURE 12 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 5.0 V

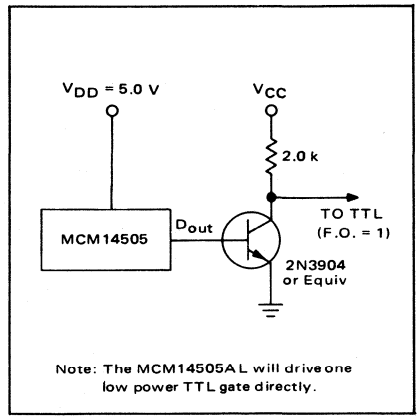


FIGURE 13 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 10 V

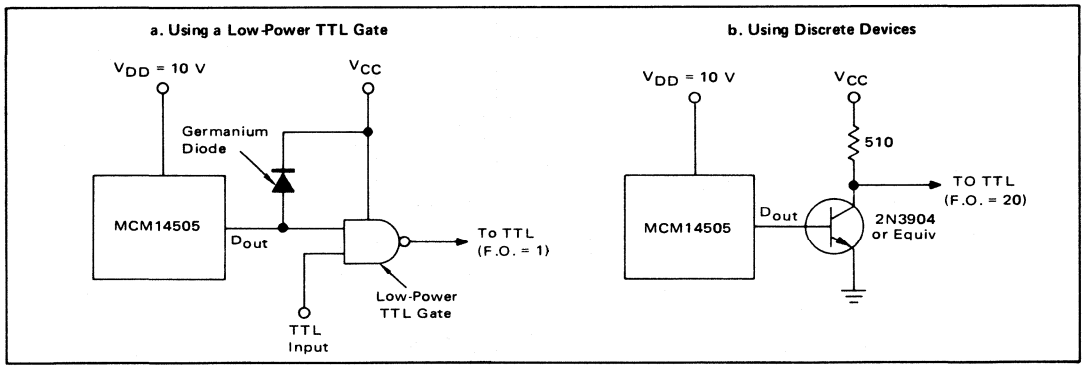
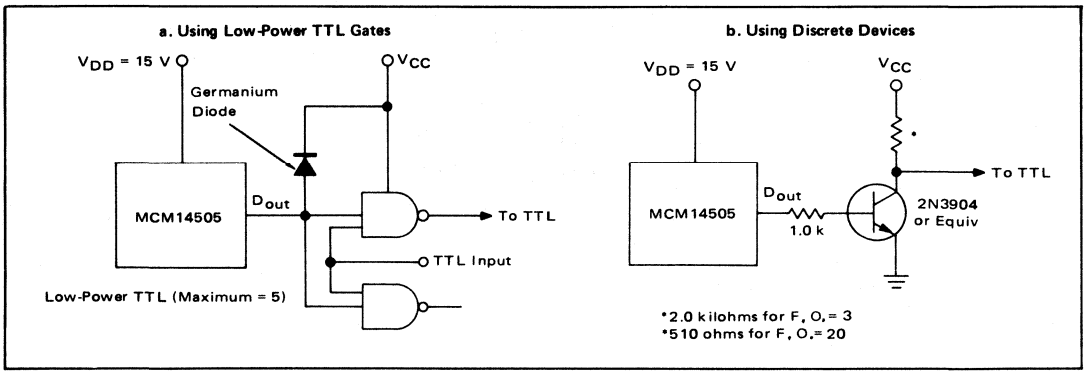


FIGURE 14 – CMOS-TO-TTL INTERFACE FOR V_{DD} = 15 V



7

MCM14524AL
MCM14524CL

Advance Information

1024-BIT READ ONLY MEMORY

The MCM14524 is a complementary MOS mask programmable Read Only Memory (ROM). This device is ordered as a factory special with its unique pattern specified by the user.

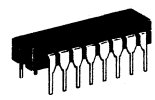
This ROM is organized in a 256 x 4-bit pattern. The contents of a specified address (< A0, A1, A2, A3, A4, A5, A6, A7 >) will appear at the four data outputs (B0, B1, B2, B3) following the negative going edge of the clock. When the clock goes high, the data present at the outputs will be latched. The memory Enable may be taken low asynchronously, forcing the data outputs low and resetting the output latches. This device finds application wherever low power or high noise immunity is a design consideration.

- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- Quiescent Power Dissipation — 11 nW/package typical
- Single Supply Operation — Either Positive or Negative
- Memory Enable Allows Expansion
- Output Latches Provide a Useful Storage Register

McMOS

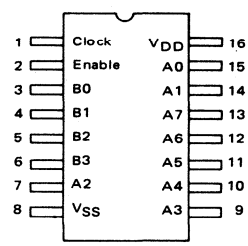
(LOW-POWER COMPLEMENTARY MOS)

1024-BIT READ ONLY MEMORY



CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage MCM14524AL MCM14524CL	V_{DD}	+18 to -0.5 +16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature — MCM14524AL Range — MCM14524CL	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

TRUTH TABLE

CLOCK	ENABLE	B0	B1	B2	B3
V_{DD} ⎍ V_{SS}	1	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*	⟨Address⟩*
V_{SS} ⎍ V_{DD}	1	OUTPUT DATA LATCHES			
X	0	0	0	0	0

X = Don't Care
*Indicates contents of specified Address will appear at outputs as stated above.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. A destructive high-current mode may occur if V_{in} or V_{out} is not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

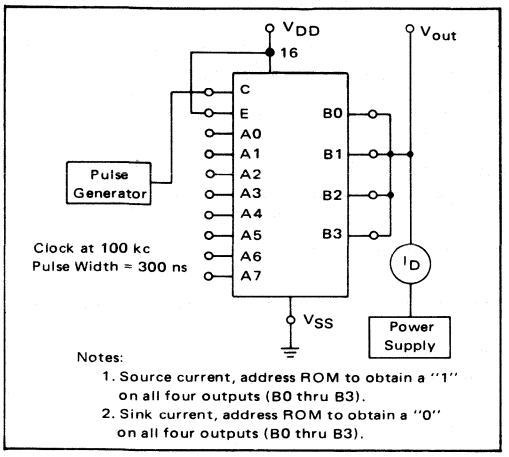
This is advance information and specifications are subject to change without notice.
See Mechanical Data Section for package dimensions.

ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	MCM14524AL/CL +25°C Min	Typ	Max	Unit
Output Voltage	"0" Level	V_{out}	5.0	–	0	0.01	Vdc
			10	–	0	0.01	
			15	–	0	0.01	
	"1" Level		5.0	4.99	5.0	–	
			10	9.99	10	–	
			15	14.99	15	–	
Noise Immunity*		V_{NL}					Vdc
(V_{out} ⩾3.5 Vdc)			5.0	1.5	2.25	–	
(V_{out} ⩾7.0 Vdc)			10	3.0	4.50	–	
(V_{out} ⩾10.5 Vdc)			15	4.5	6.75	–	
(V_{out} ⩽1.5 Vdc)		V_{NH}	5.0	1.5	2.25	–	Vdc
(V_{out} ⩽3.0 Vdc)			10	3.0	4.50	–	
(V_{out} ⩽4.5 Vdc)			15	4.5	6.75	–	
Output Drive Current	I_{Source}	I_{OH}					mAdc
(V_{OH} = 2.5 Vdc)			5.0	–	-0.6	–	
(V_{OH} = 9.5 Vdc)			10	–	-0.33	–	
(V_{OH} = 13.5 Vdc)			15	–	-1.5	–	
(V_{OL} = 0.4 Vdc)	I_{Sink}	I_{OL}	5.0	–	0.21	–	mAdc
(V_{OL} = 0.5 Vdc)			10	–	0.57	–	
(V_{OL} = 1.5 Vdc)			15	–	2.6	–	
Input Current		I_{in}	–	–	10	–	pAdc
Input Capacitance (All Inputs) (V_{in} = 0)		C_{in}	–	–	5.0	–	pF
Quiescent Dissipation		P_D					μW
			5.0	–	0.011	50	
			10	–	0.031	200	
			15	–	0.066	–	
Clock Read Access Delay (C_L = 15 pF)		t_{acc_C}					ns
			5.0	–	1800	–	
			10	–	825	–	
			15	–	530	–	
Enable Access Delay (C_L = 15 pF)		$t_{acc_{E_n}}$					ns
			5.0	–	265	–	
			10	–	100	–	
			15	–	70	–	
Output Rise and Fall Time (C_L = 15 pF)		t_r, t_f					ns
			5.0	–	170	–	
			10	–	75	–	
			15	–	55	–	
Minimum Clock Pulse Width**		PW_{CH}	5.0	–	130	–	ns
			10	–	60	–	
			15	–	60	–	
		PW_{CL}	5.0	–	1600	–	
			10	–	755	–	
			15	–	500	–	
Maximum Clock Pulse Width†		PW_{CL}	5.0		6.5	–	ms
			10		1.5	–	
			15		0.15	–	
Address Setup Time		t_{setup_A}	5.0	–	0	–	ns
			10	–	0	–	
			15	–	0	–	
Clock to Enable Setup Time		t_{setup_C}	5.0	–	1750	–	ns
			10	–	800	–	
			15	–	515	–	
Clock to Enable Hold Time		t_{hold_C}	5.0	–	0	–	ns
			10	–	0	–	
			15	–	0	–	
Address Hold Time		t_{hold_A}	5.0	–	0	–	ns
			10	–	0	–	
			15	–	0	–	
Typical Dynamic Power Dissipation (C_L = 15 pF, All Outputs)		P_D					mW
			5.0	P_D = (13.5 mW/MHz) f (MHz) + 0.000011 mW			
			10	P_D = (36 mW/MHz) f (MHz) + 0.000036 mW			
			15	P_D = (200 mW/MHz) f (MHz) + 0.000066 mW			

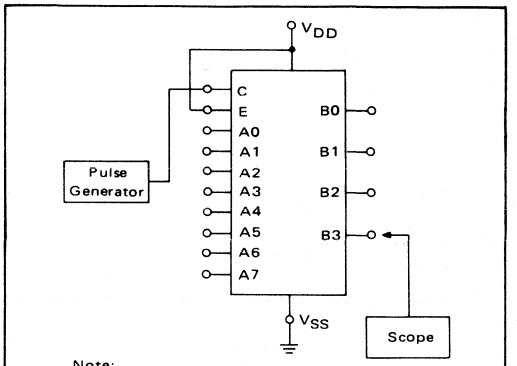
*DC Noise Margin (V_{NH}, V_{NL}) is defined as the maximum voltage change from an ideal "1" or "0" input level before producing an output state change.
**The clock can remain high indefinitely with the data remaining latched.
†If clock stays low too long, the dynamically stored data will leak off and will have to be recalled.

FIGURE 1 – OUTPUT DRIVE CURRENT TEST CIRCUIT



Notes:
1. Source current, address ROM to obtain a "1" on all four outputs (B0 thru B3).
2. Sink current, address ROM to obtain a "0" on all four outputs (B0 thru B3).

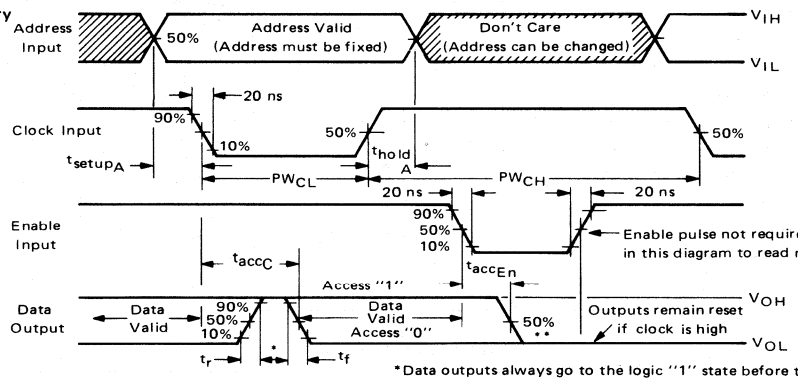
FIGURE 2 – SWITCHING TIME TEST CIRCUIT
(Refer to timing diagram)



Note:
Address ROM to obtain level change when clocking any one address line.

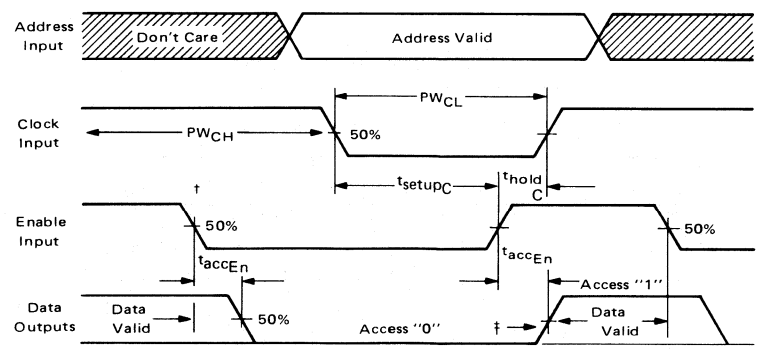
MEMORY READ CYCLE TIMING DIAGRAMS

a) Using Clock to Read Memory



*Data outputs always go to the logic "1" state before the data is valid between accessing successive "0's"
**Outputs forced to "0" by Enable.

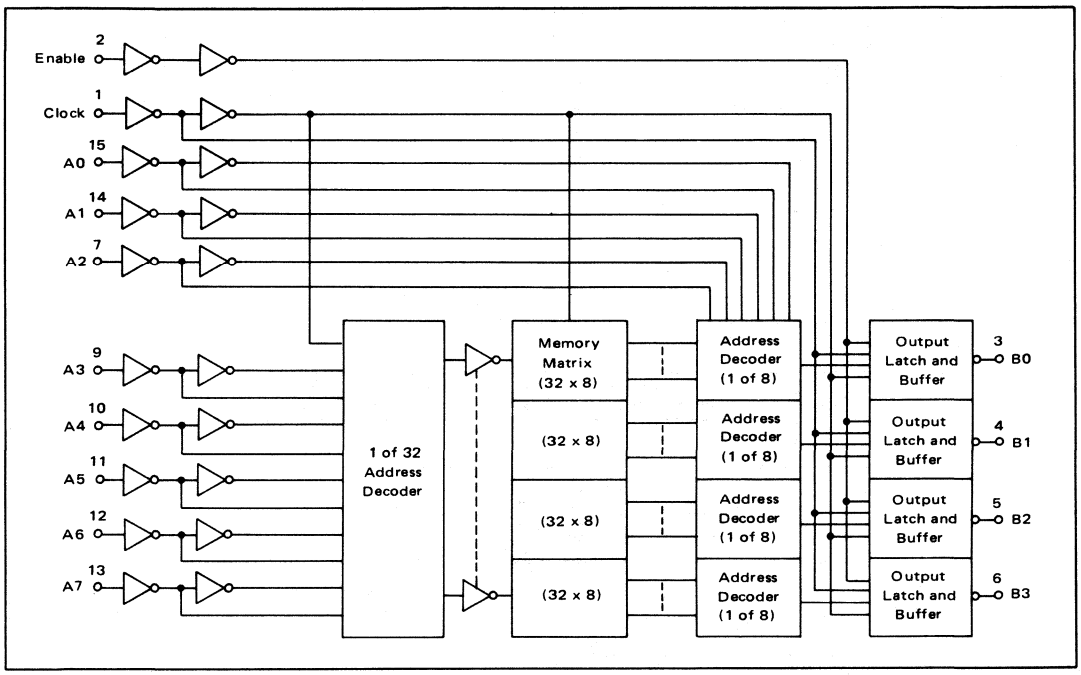
b) Using the Enable to Read Memory



† In this mode of operation, the negative going edge of Enable should occur on or before the clock negative edge.

‡The data outputs are valid without the logic "1" pulse occurring during the access cycle as shown in a) above.

BLOCK DIAGRAM



CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM14524, the customer may specify the content of the memory.

Address Inputs:

Words are numbered 0 through 255 and are addressed using sequential addressing of Address leads A0 through A7 with A0 as the least significant digit.

Logic "0" is defined as a "low" Address input (V_{IL}).
Logic "1" is defined as a "high" Address input (V_{IH}).

WORD \ ADDRESS		A7	A6	A5	A4	A3	A2	A1	A0
Word	0	0	0	0	0	0	0	0	0
Word	1	0	0	0	0	0	0	0	1
Word	2	0	0	0	0	0	0	1	0
Word	3	0	0	0	0	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
Word	255	1	1	1	1	1	1	1	1

Two methods may be used to transmit the custom memory pattern to Motorola.

METHOD A: PUNCHED COMPUTER CARDS

A binary coded decimal equivalent of each desired output may be punched in standard computer cards (four cards are required for all 256 words) in numerical (word number) order. 64 words per card are punched in columns 12 thru 75 using the Binary to Hexadecimal conversion table below. Columns 77 and 78 are used to number the cards, which must be in numerical order. Please use characters as shown in the table when punching computer cards.

BINARY TO HEXA-DECIMAL CON-VERSION TABLE

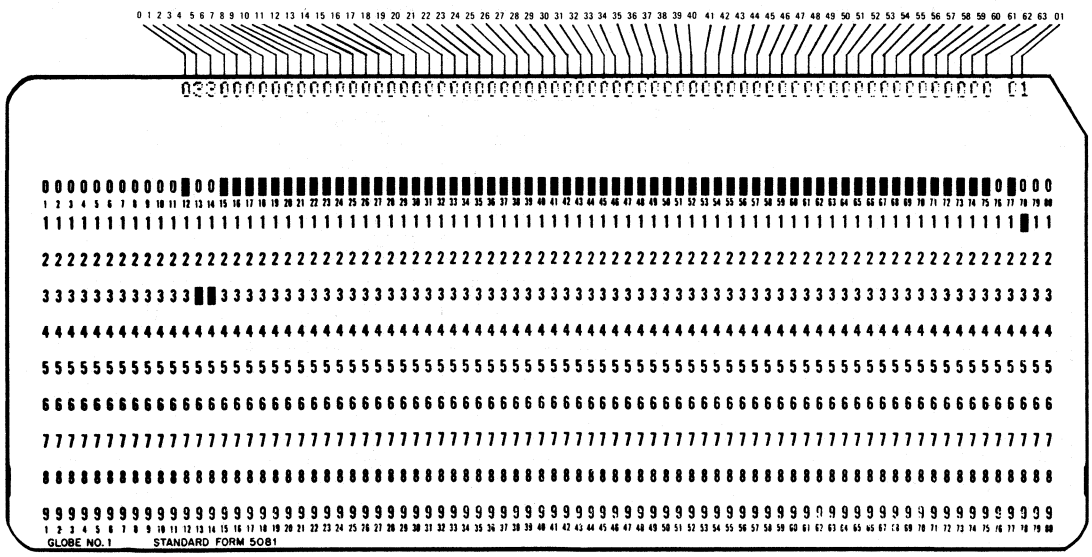
BINARY WORD DESIRED	CARD CHARACTER
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	A
1 0 1 1	B
1 1 0 0	C
1 1 0 1	D
1 1 1 0	E
1 1 1 1	F

ROM SAMPLE WORD PROGRAMMING FOR PUNCHED CARD

WORD NUMBER	ADDRESS INPUTS								SAMPLE WORD OUTPUTS				CARD CHARACTER
	A7	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	1	1	3
2	0	0	0	0	0	0	1	0	0	0	1	1	3
3	0	0	0	0	0	0	1	1	0	0	0	0	0
I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I
I	I	I	I	I	I	I	I	I	I	I	I	I	I
255	1	1	1	1	1	1	1	1	1	0	1	0	A

Shown in columns 12 – 15 on card below

WORD NUMBER



METHOD B: TRUTH TABLE

Use of the truth table presents a simple and direct way to input the memory pattern desired to Motorola. When filling out the table please use a "1" for a high, and a "0" for a low.

CUSTOM PROGRAM for the MCM14524AL/CL Read Only Memory

WORD	BIT 3	2	1	0
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				
16				
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